Super Chip Integration Based on Chip-to-Wafer 3D Integration Technology

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Super-Chip Integration Based on Chip-to-Wafer 3D Integration Technology

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Outline

- Background
- 3D Integration Technology [Tohoku Univ.]
- Super-Chip Integration
- Conclusion

Future market of semiconductor industry expands into various fields.
【ICT・Nano-tech・Bio・Robot】

Qualitative change of semiconductor technology

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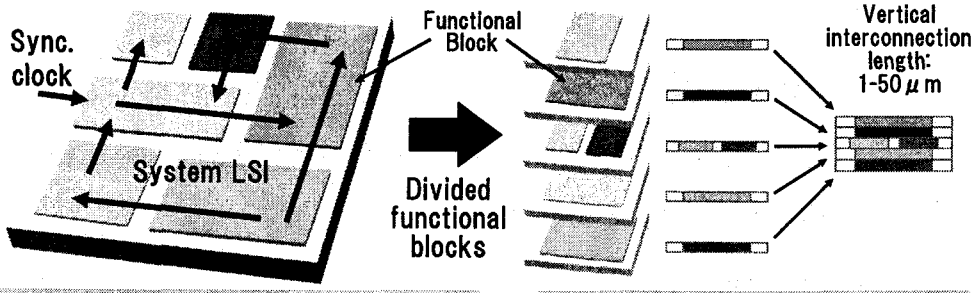
Fusion with different technologies

3-dimensional Integration
【Core technology for fusion】

Advantages of 3D LSI

■Conventional 2D LSI ■3D stacked LSI



Concern: Propagation delay due to long wiring

Short wiring due to vertical interconnection and thin chip

1. Short wiring length
2. High packing density
3. High-speed operation
4. Low power consumption
5. Low cost
6. Parallel processing
7. New function
8. New application

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- Background
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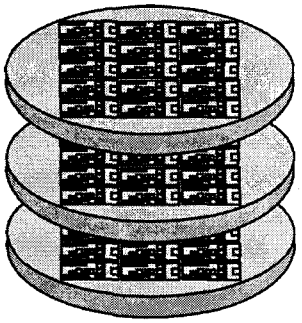
3D LSI Project at Tohoku University

3D integration: two approaches
- Jisso (Package) level
- LSI (Tr) level

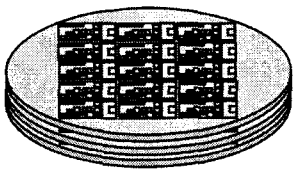
2D LSI wafers with vertical interconnection



Wafer thinning

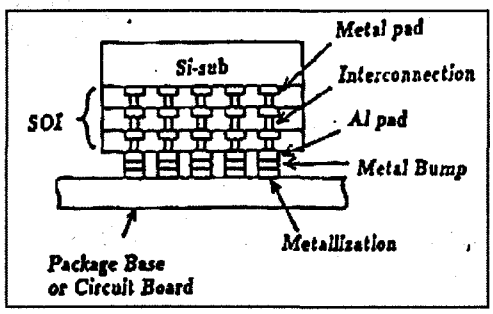
Wafer-to-wafer bonding

3D LSI



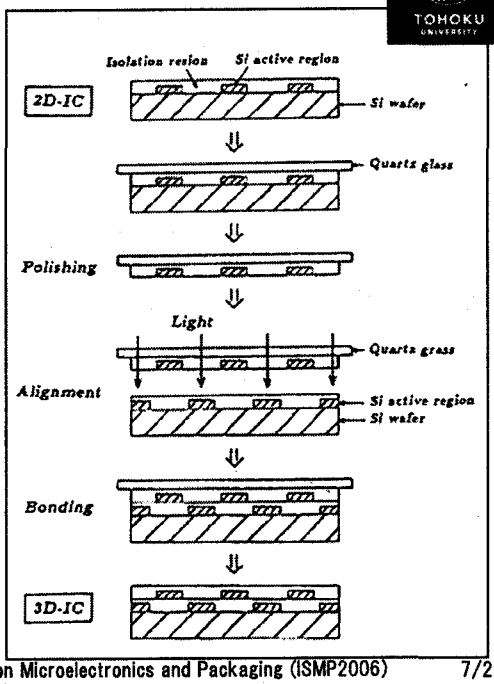
First proposal of 3D LSI using wafer-to-wafer bonding with buried interconnections and micro-bumps (1989)

3D Integration Technology Using Wafer Bonding and Thinning

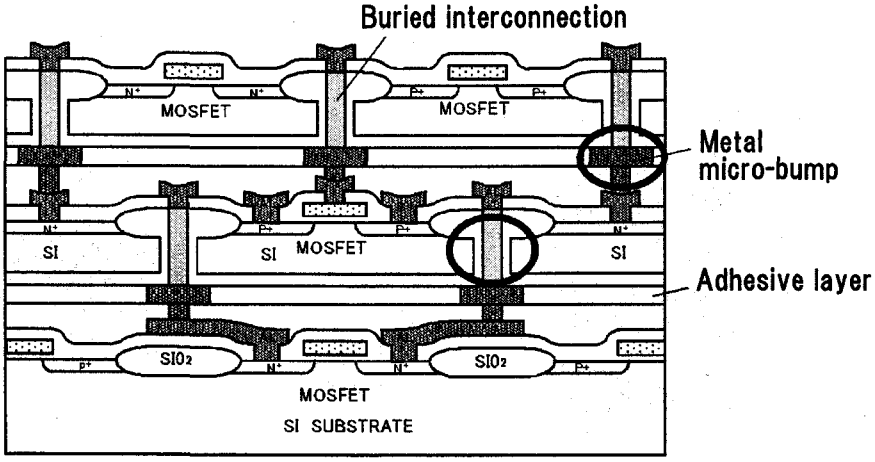


M. Koyanagi,
Proc. 8th Symposium on Future Electron Devices, pp.50-60
(Oct. 1989)

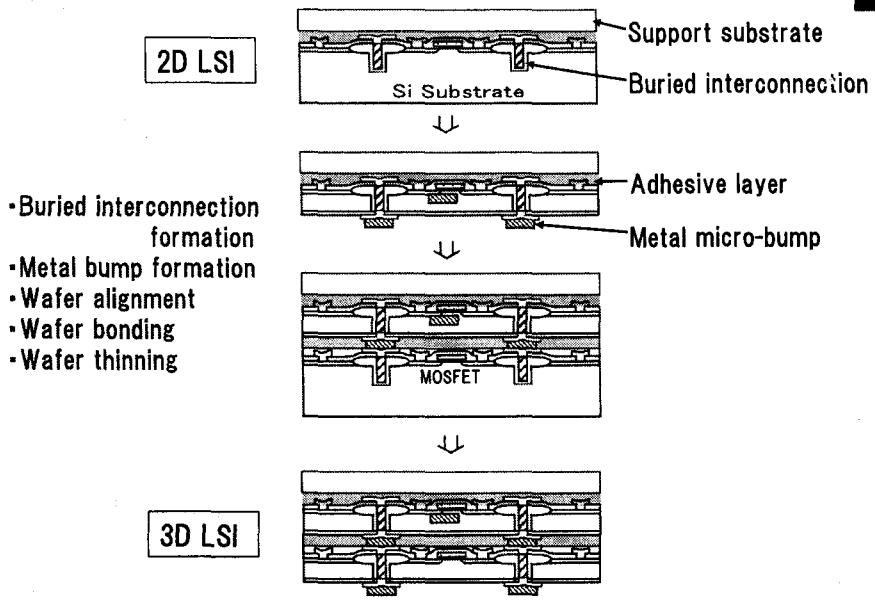
H. Takata, M. Koyanagi et. al.,
Proc. Intern. Semiconductor Device Research Symposium, pp.327-330
(Dec. 1991)



3D LSI Structure Using Tohoku Univ. Method

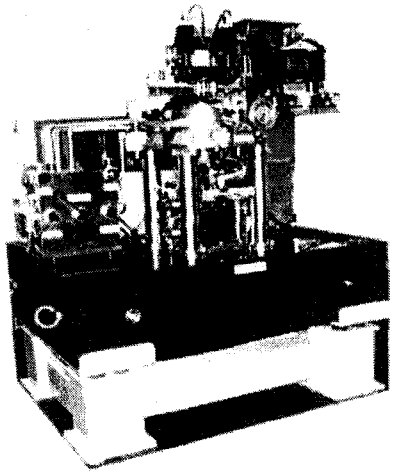


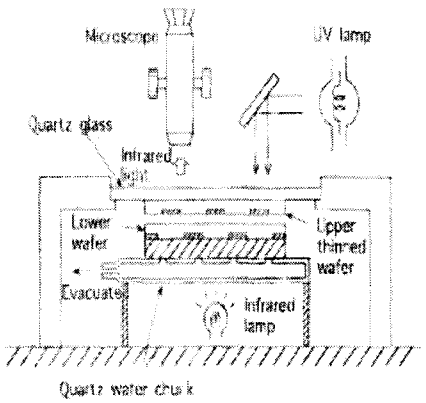
Key Technologies for 3D LSI Process



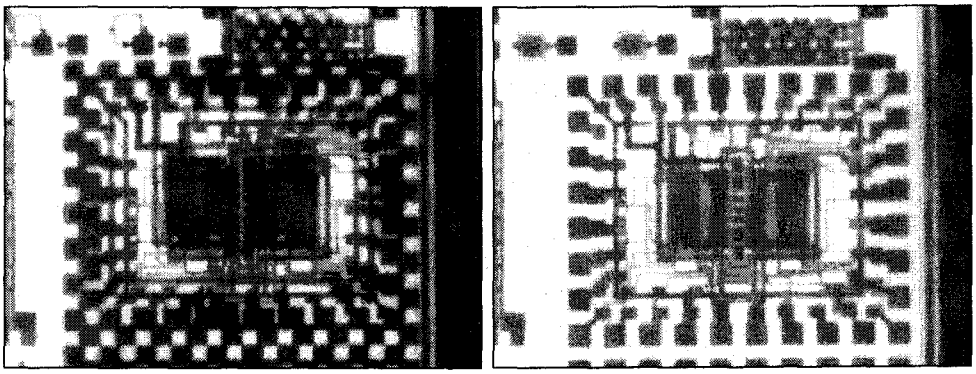
- Buried interconnection formation
- Metal bump formation
- Wafer alignment
- Wafer bonding
- Wafer thinning

Photograph of 3D Wafer Aligner





IR Images of 3D Test Chip



Before alignment

After alignment

3D LSI Chips Fabricated at Tohoku Univ.

3D image sensor chip

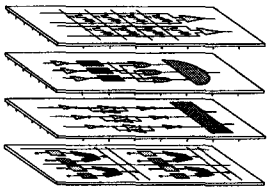
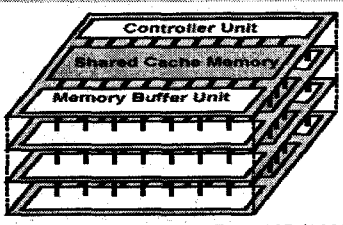


Image sensor
AMP & ADC
Resistor
Processor

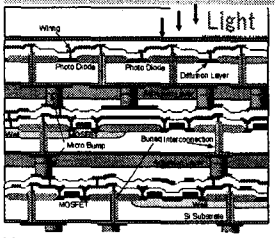
H. Kurino, M. Koyanagi *et al.*, IEDM, 879 (1999)

3D shared memory chip



K. W. Lee, M. Koyanagi *et al.*, IEDM, 165 (2000)

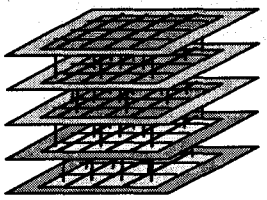
3D retinal prosthesis chip



Quartz glass
Photoreceptor layer
Horizontal/ Bipolar cell layer
Ganglion cell layer

M. Koyanagi *et al.*, ISSCC, 270 (2001)

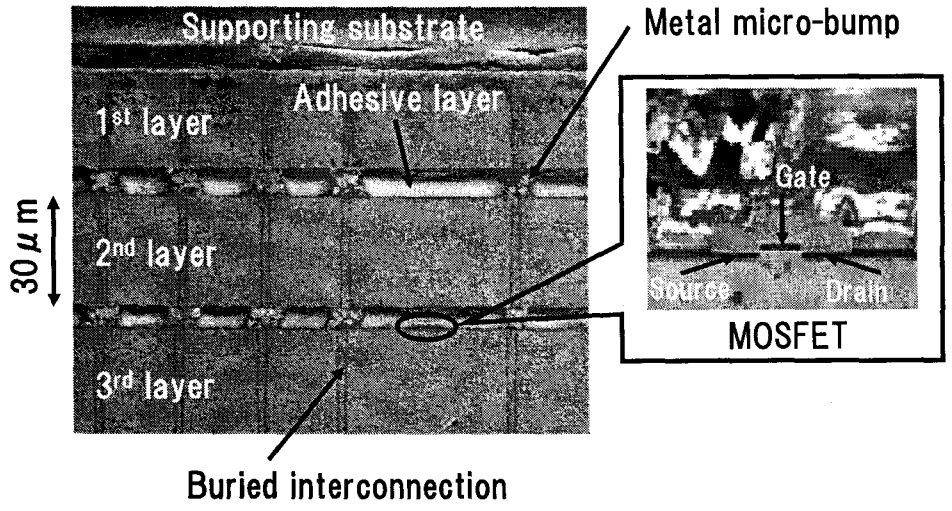
3D micro processor chip



DRAM
DRAM
DRAM
SRAM
Processor

T. Ono, M. Koyanagi *et al.*, IEEE COOL Chips, 186 (2002)

SEM Cross-Section of 3D Micro Processor Fabricated Using Wafer-to-Wafer Bonding



Publications of Fabricated 3D IC Chips

- 3-layer stacked image sensor chip(Mitsubishi) (IEDM, 1986)
  Laser recrystallization
- 3-layer stacked image sensor chip(*Tohoku Univ.*) (IEDM, 1999)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked memory chip(*Tohoku Univ.*) (IEDM, 2000)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 2-layer stacked image sensor chip (MIT) (ISSCC, 2001)
  SOI wafer bonding
- 3-layer stacked artificial retina chip(*Tohoku Univ.*) (ISSCC, 2001)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked microprocessor chip(*Tohoku Univ.*) (Cool Chips, 2002)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 2-layer stacked image sensor chip (MIT) (ISSCC, 2005)
  SOI wafer bonding

3D LSI Projects in the World

■USA (DARPA)
IBM, Freescale, Intel, Stanford, MIT, Rensselaer Polytechnic, etc.

■EC IMEC

■Germany
Fraunhofer, Infineon

■Japan
NEDO-project, ASET consortium

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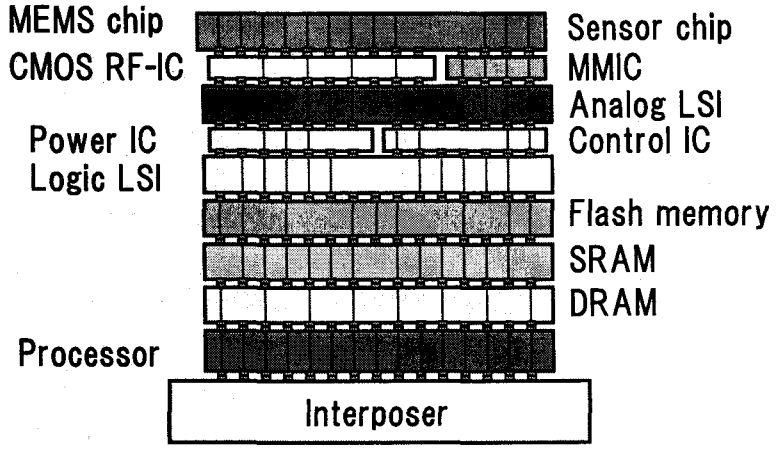
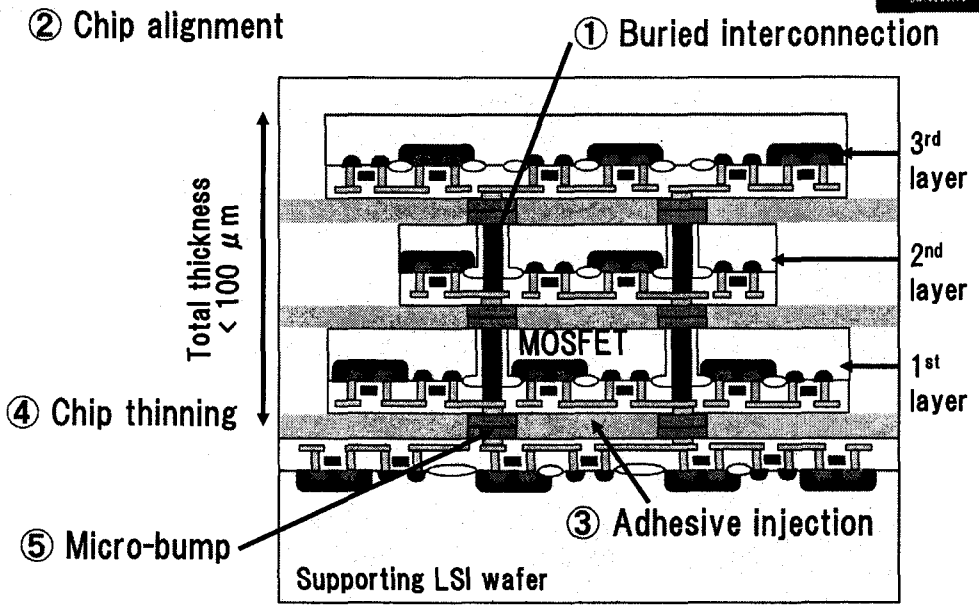
Conceptual Structure of 3D Super-Chip



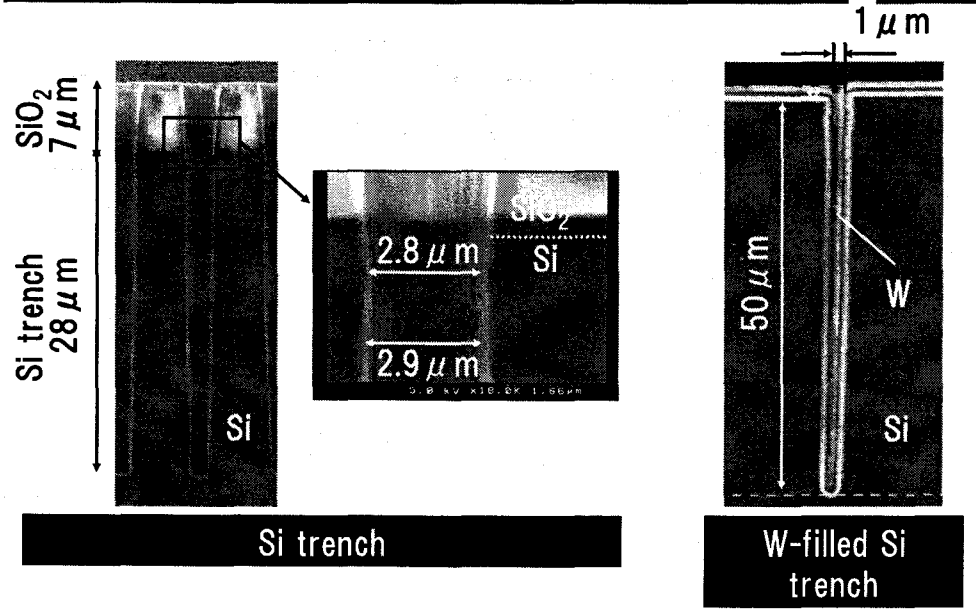
Comparison of 3D Integration Technology

Bonding	Wafer - Wafer	Chip - Wafer	Chip - Chip
Yield	Low	High	High
Availability of chip size	Low	High	High
Throughput	High	Low⇒High	Low

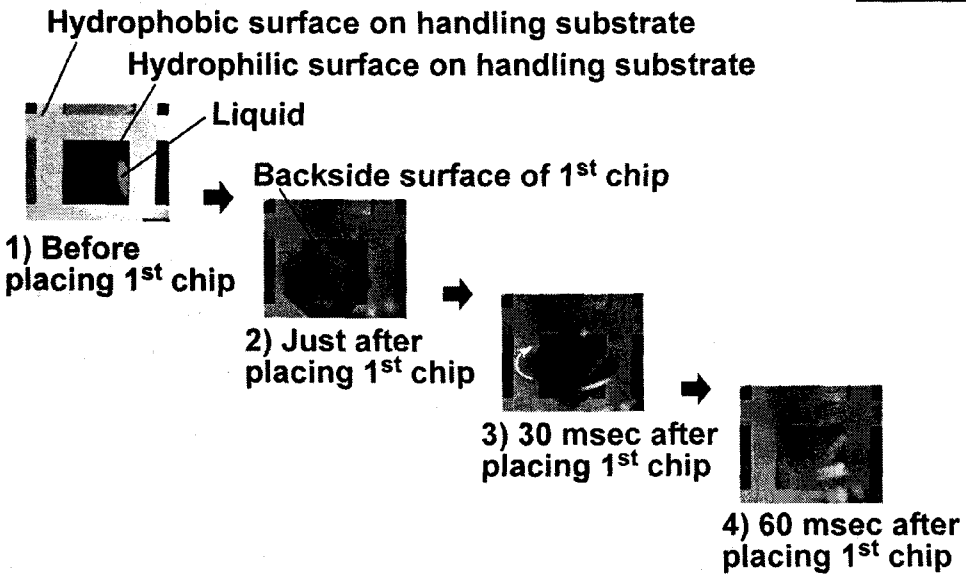
Key Technologies for 3D Super-Chip Integration



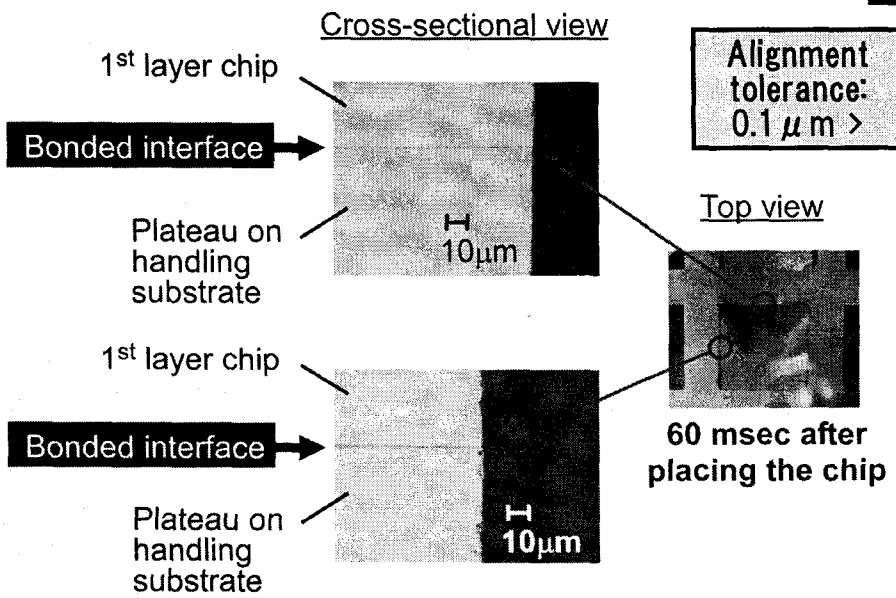
SEM Cross-Section of Si Trench Formed Through Thick SiO_2 and W-filled Si Trench



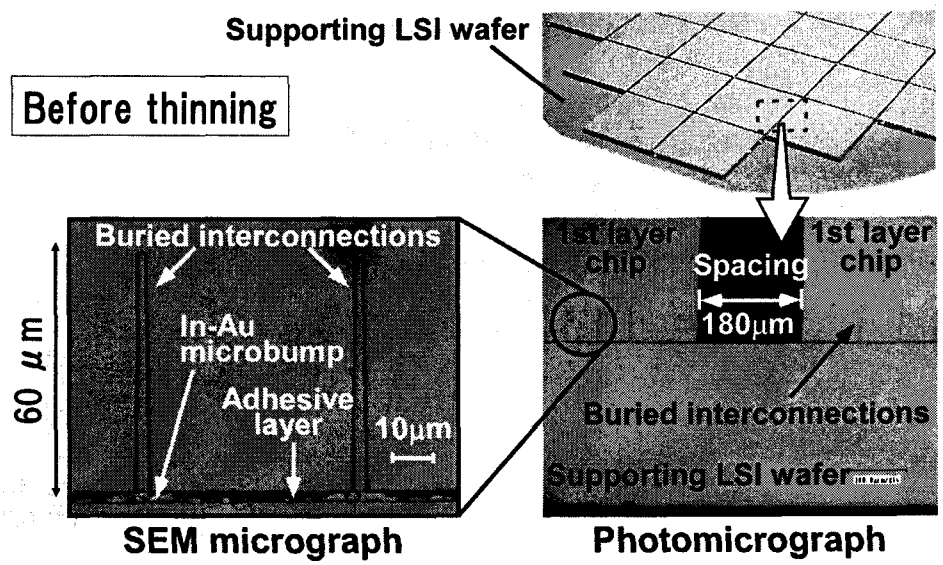
Chip Alignment by Self-Assembly Technique



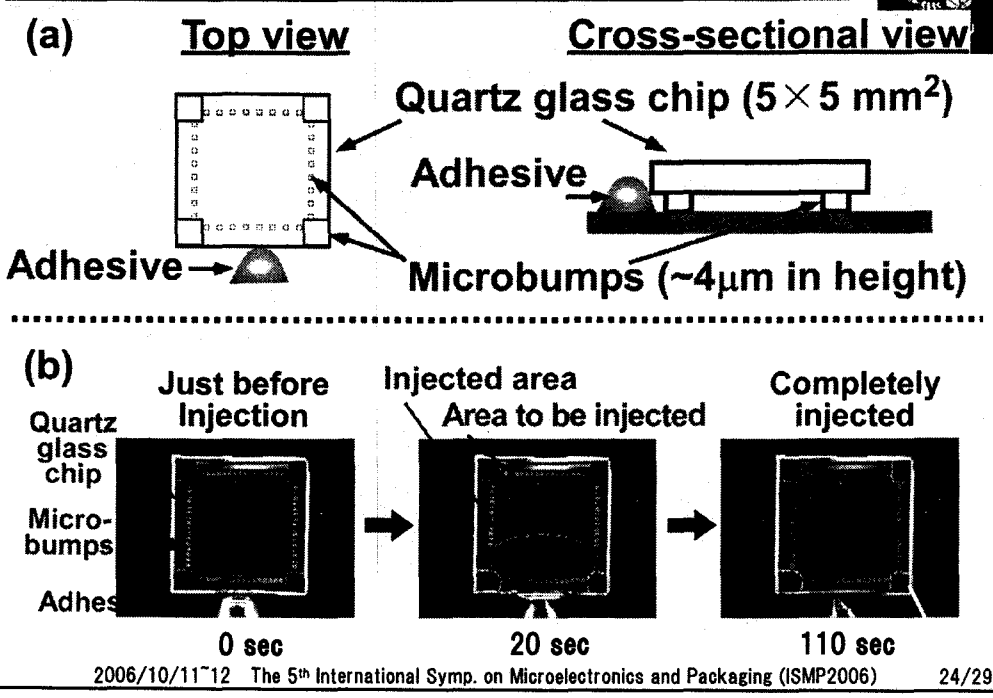
SEM Cross-Section of 1st Layer Chip Aligned to Plateau on Handling Substrate



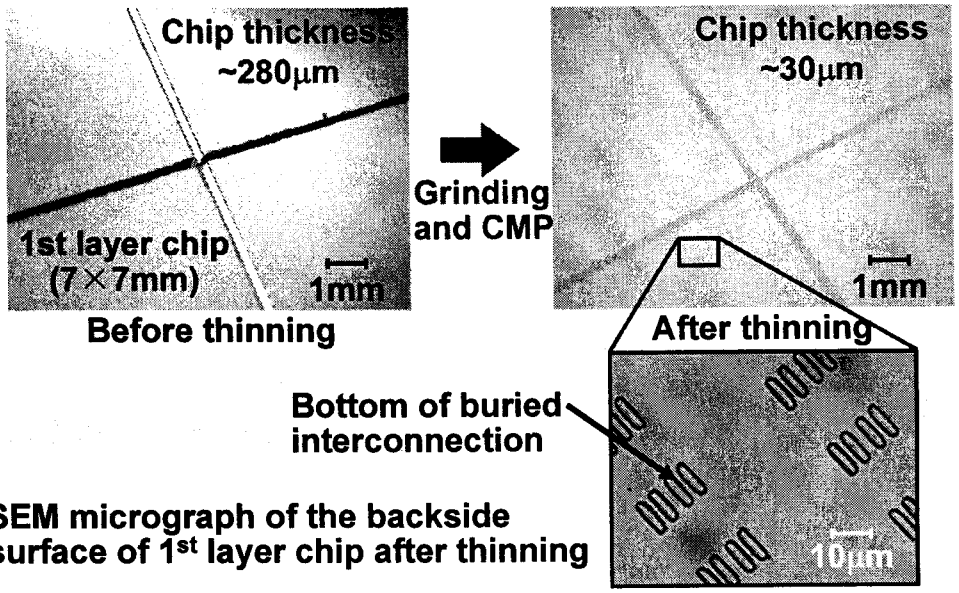
Cross-Section of 1st Layer Chips Bonded onto Supporting LSI Wafer Using Self-Assembly Technique



Adhesive Injection Test Using Quartz Glass Chip

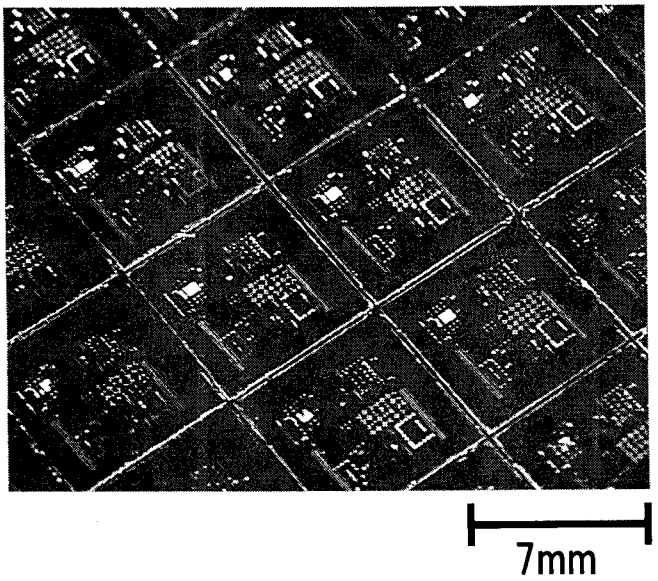


Photomicrograph of 1st Layer Chips Before and After Thinning

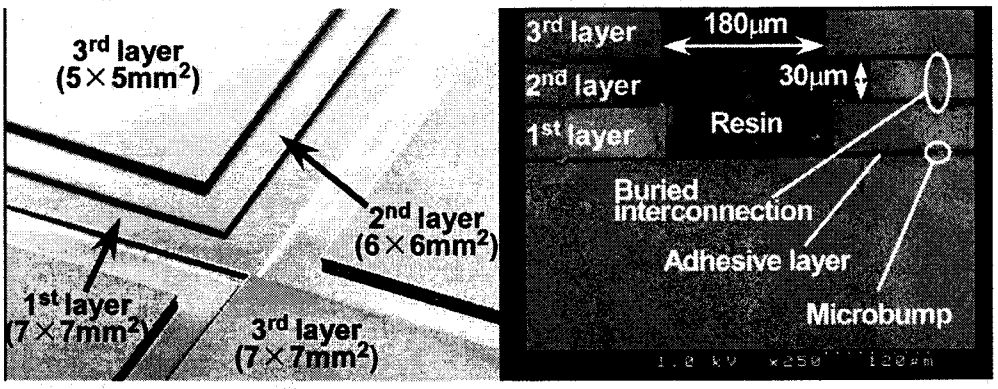


SEM micrograph of the backside surface of 1st layer chip after thinning

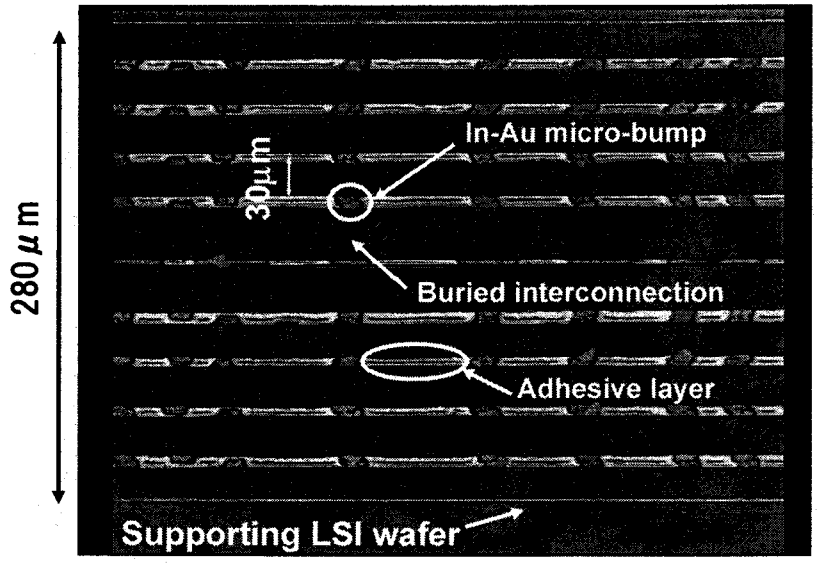
Photomicrograph of 1st Layer Chips After In-Au Micro-bumps Formation



Photomicrograph of Three-Layer Stacked Chips with Different Chip Size



SEM Cross-Sectional View of 3D Memory Super-Chip (10 Memory Layers)



Application of 3D LSI Technology