

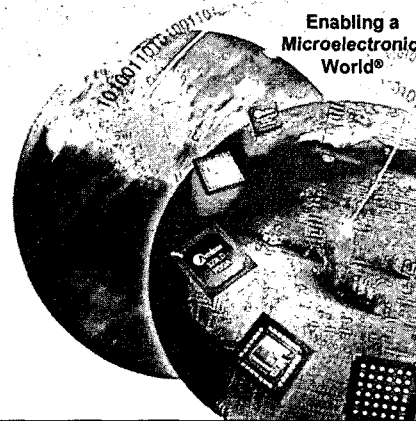
Reliability Study of Package on Package

은 영 호 책임연구원
(앰코코리아)

Reliability Study of Package on Package

Feb. 15, 2006
YoungHyo Eun

Enabling a
Microelectronic
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Package on Package (PoP) Introduction



- **PoP technology and infrastructure has been in development at Amkor > 5 years and production > 2 years.**
 - CSP structure was developed from 2003, released to production in Q4 of 2004
 - Flip chip structure was developed from 2004, scheduled to go to production line in Q3, this year
- **Amkor CSP package is qualified**
- **Commitment to Standardization work for broad industry benefit**
- **PoP applications include:**
 - Mobile phones (base band or applications processor + combo memory)
 - Digital cameras (image processor + memory)
 - Portable gaming (graphics processor + memory)



Package on Package (PoP) Introduction



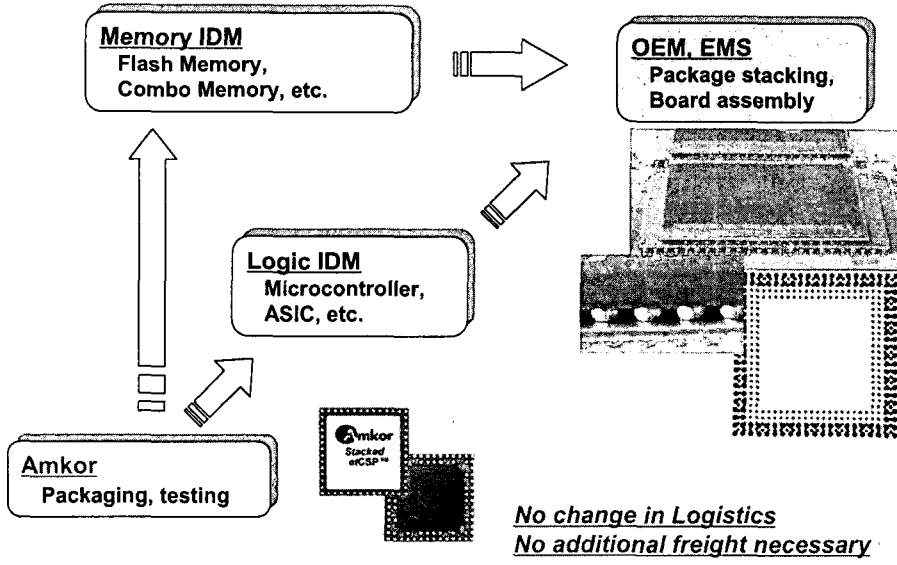
- Amkor has full commitment to PoP technology for both bottom and top packages.
- Initial applications in HVM and pre-production w/out underfill
- BLR data gathering on going with underfill
- Applied CSP platform technologies to quickly develop Base Pkg platform
- Have full suite of turnkey FC capabilities - internal bumping, probe, design, assembly and final test enable device transition to fine pitch FC PoP applications which the market is driving towards for next generation devices.

Stacked Die vs. PoP – Trade offs



Stacked Die 	PoP 
<p><u>Prospects</u></p> <ul style="list-style-type: none"> • IDM ownership • Smaller body size and lower package profile • Standard SMT assembly • Broad infrastructure 	<p><u>Prospects</u></p> <ul style="list-style-type: none"> • OEM Ownership • Flexible sourcing: • Tested at individual package level for Known-Good Device
<p><u>Concerns</u></p> <ul style="list-style-type: none"> • KGD required for high product yield • Single-sourced product for logic + memory • New development needed to change a device or handle die shrink • Sourcing, compound yield and multi test: <ul style="list-style-type: none"> - Can lead to higher total cost 	<p><u>Concerns</u></p> <ul style="list-style-type: none"> • Slightly larger / thicker Package stack • Coordinated business model covering: <ul style="list-style-type: none"> - Co-design for bottom and top packages - Electrical and BLR validation • Infrastructure for package stacking

PoP Logistics

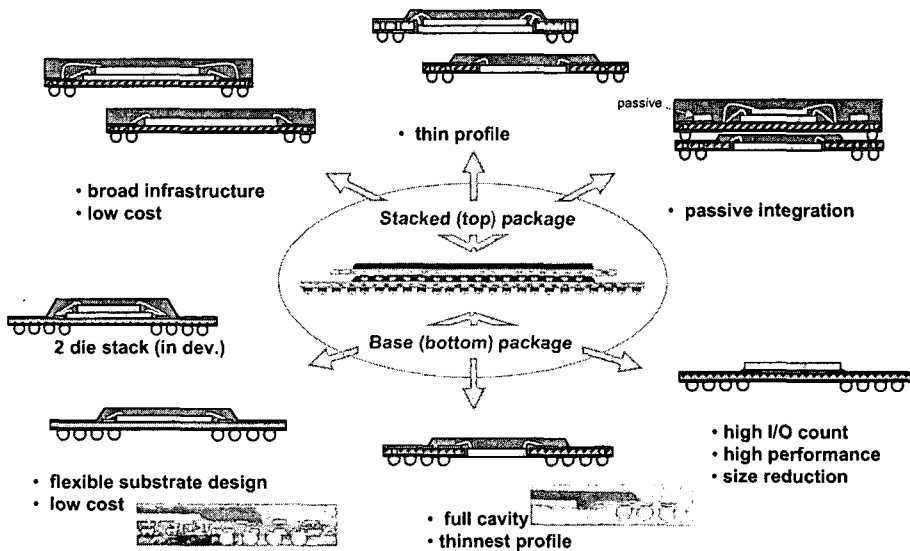


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PoP Options – Ready for Deployment



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PoP Features (bottom package options)



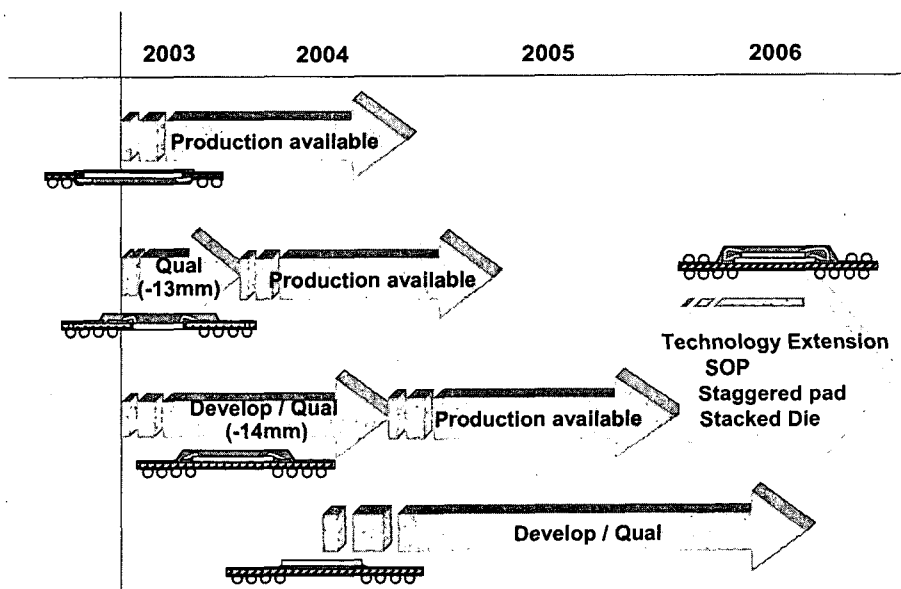
Items			
Substrate	2 / 4 layer	2 layer	4 layer or more
Cavity	No cavity	Full cavity	No cavity
Mold thickness	0.27 mold	0.2 mold	
Die thickness	0.10 die	0.15 die	0.15 – 0.20 die
Die pad count	- 400 I/Os	- 350 I/Os	400+ I/Os
Routing	Flexible	Limited	Flexible
Thermal ball	Available	Not available	Available
Bottom footprint	0.5 – 0.8 mm pitch flexible	0.5 mm pitch only	0.5 – 0.8 mm pitch flexible
Top package	0.65 mm pitch	0.5 mm pitch available	0.5 mm pitch potential
Module height after stacked	High	Low profile	Middle
Stacked die	Potential with thick mold	Potential with thick substrate	Potential with mold
Status	Qualified (14mm)	Qualified (13mm)	Development

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PoP Family Roadmap







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Base Package Development Roadmap



		Available	2006	2007	
Design Rules		Substrate Thickness (1+2+1)	0.3 mm	0.26 mm	0.22 mm
		Body Size	12mm – 14mm	10mm – 14mm	8mm – 16mm
		Memory package interface			
		BGA pitch	0.65mm	0.50 mm	0.45 mm
		Rows	2	2	2
		Mold cap thickness			
New Package Features		Solder on top BGA pad	Development	Production	Production
		Multi-tier wire bonding	Development	Production	Production
		Stacked die	Development	Production	Production
			PSvfBGA Extensions		
			FC-CSP base package		
		Die thickness	200µm	150µm	125µm
		Solder bump array pitch	225µm	200µm	180µm
		Au stud peripheral pitch	N/A	60µm	50µm
		Body Size			

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PSfcCSP - Base



Description	unit : mm		
	Min	Normal	Max
Bump height (H)*	0.060	0.070	0.080
Chip Thickness(C1)	0.187	0.200	0.213
Substrate Thickness(B1)	0.230	0.270	0.310
Ball height (D1)	0.170	0.210	0.250
Package Overall Height (A1=C1+H+B1+D1) **	0.691	0.750	0.809
SM to FC surface	0.254	0.270	0.286

Note) * Empirical

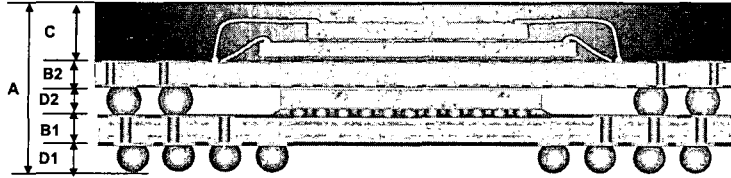
** : Values for min/max shown are calculated using Root Mean Square (RMS) deviation

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PSfcCSP - Top Package Stacked

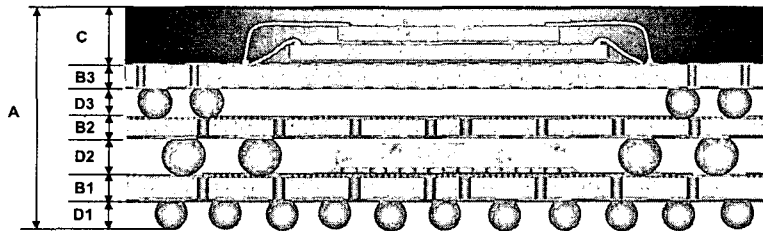


unit : mm

Description	Min	Nominal	Max	Remarks
Ball height (D1)	0.170	0.210	0.250	
Substrate Thickness(B1)	0.230	0.270	0.310	
Ball height (D2)	0.260	0.290	0.320	0.42 mm SB, 0.32mm SMO
Substrate Thickness(B2)	0.180	0.210	0.240	
Mold Cap Thickness(C)	0.380	0.400	0.420	
POP Overall Height *	1.307	1.380	1.453	$A=D1+B1+D2+B2+C$

Note) * : Values for min/max shown are calculated using Root Mean Square (RMS) deviation

PSfcCSP – Interposer & Top Package Stacked

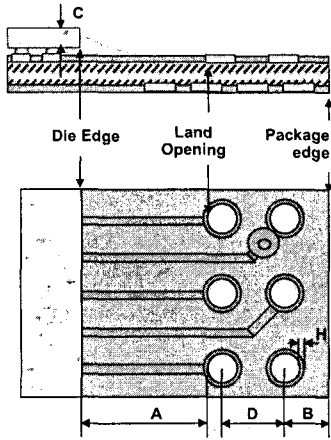


unit : mm

Description	Min	Nominal	Max	Remarks
Ball height (D1)	0.170	0.210	0.250	0.3 mm SB, 0.28mm SMO
Substrate Thickness(B1)	0.230	0.270	0.310	
Ball height (D2)	0.290	0.320	0.350	0.4 mm SB, 0.28mm SMO
Substrate Thickness(B2)	0.180	0.210	0.240	
Ball height (D3)	0.180	0.210	0.240	0.3 mm SB, 0.2mm SMO
Substrate Thickness(B3)	0.180	0.210	0.240	
Mold Cap Thickness(C)	0.380	0.400	0.420	
POP Overall Height *	1.757	1.830	1.903	$A=D1+B1+D2+B2+D3+B3+C$

Note) * : Values for min/max shown are calculated using Root Mean Square (RMS) deviation

PSfcCSP - Design Guideline



Design Rules

Die Edge to Land Opening: A (min)*

- Die size < 5.0mm

dispensing side

1700

1500

exit side

1000

800

- 5.0mm ≤ Die size < 8.0mm

dispensing side

2500

2000

exit side

1500

1300

- 8.0mm < Die size

dispensing side

3000

2500

exit side

1500

1300

Package Edge to Ball Center: B (min)

500

475

Top Land pitch (mm): D (min)

0.65

0.5**

S/M Registration: H (min)

50

40

Die Thickness : C (nom)

200

150

Bump Height after FC attach reflow

* Dimensions are in microns, if not specified.

** For 0.5 mm pitch memory interface, thin FC and/or SOP shall be applied.

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PSfcCSP – 2 Stack vs 3 Stack



• BOM

– Substrate

- PSfcCSP: 13BD, 361/136LD(Btm/Top), 0.06 core, 4L, 0.26T

- Interposer: 13BD, 136LD, 0.1 core, 2L, 0.16T

- SCSP: 8x12BD, 67LD, 0.1 core, 2L, 0.21T

– Flux for Flip Chip: INF-1

– Underfilling: NAU-8, ALU-3

– Solder ball

- Lead free, Sn95.5 / Ag4.0 / Cu0.5

- PS-fcCSP : 0.3 dia.

- Interposer : 0.4 dia.

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PSfcCSP – 2 Stack vs 3 Stack



- The prestacking yield of 2 stack was better than that of 3 stack, because thin interposer (0.16mm thk) has severe crying warpage
 - 2 stack : about 80%
 - 3 stack : about 30%
- Severe warpage was induced after underfill material cure, and it affected interposer attach
- TC Reliability Test Result
 - Condition (-55/125), w/o precon

UF	2 Stack		3 Stack	
	500X	1000X	500X	1000X
NAU-8	PASS	PASS	PASS	FAIL
ALU-3	PASS	PASS	PASS	PASS

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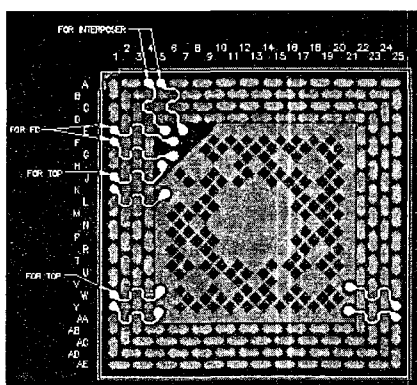
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PSfcCSP – 2 Stack vs 3 Stack

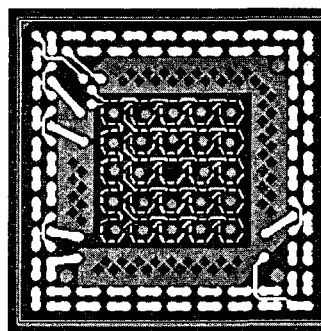


- DC Net_Bottom package, PSfcCSP

Green : FC bumping net
 Yellow : Interposer + btm pkg net
 Cyan : Interposer + top pkg net



Bottom view



Top view

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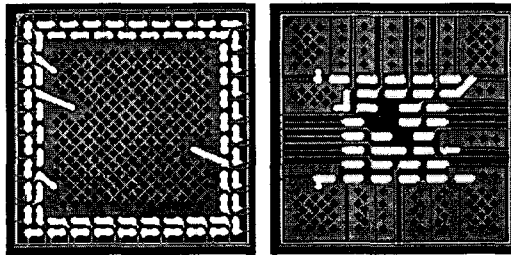
PSfcCSP – 2 Stack vs 3 Stack



- DC Net_Interposer & Top Package, SCSP

Green : FC bumping net
 Yellow : Interposer + btm pkg net
 Cyan : Interposer + top pkg net

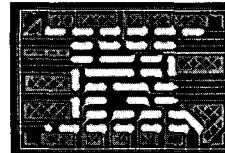
Interposer



Bottom view

Top view

SCSP



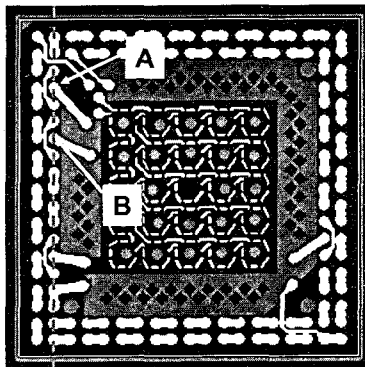
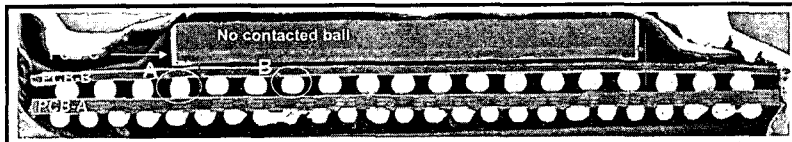
Bottom view

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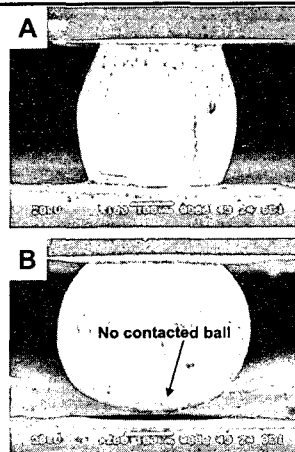
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SEM Analysis_3 Stack NAU-8



X-section 1



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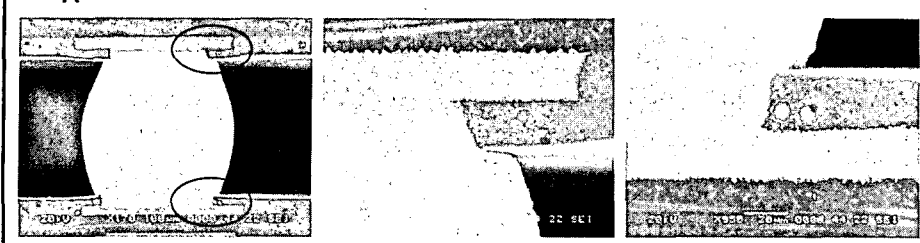
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SEM Analysis_3 Stack NAU-8

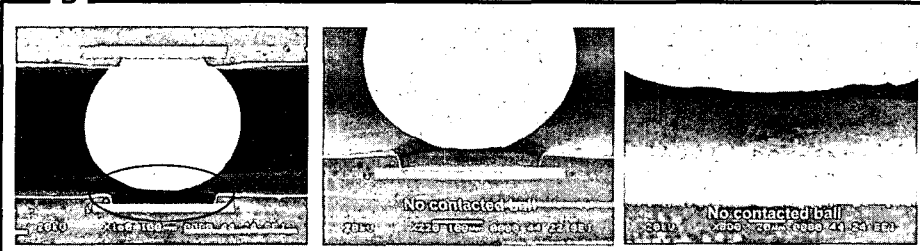


X-section 1

A



B

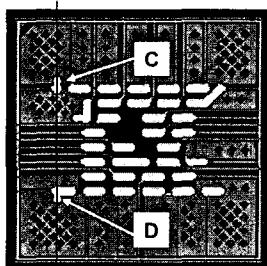


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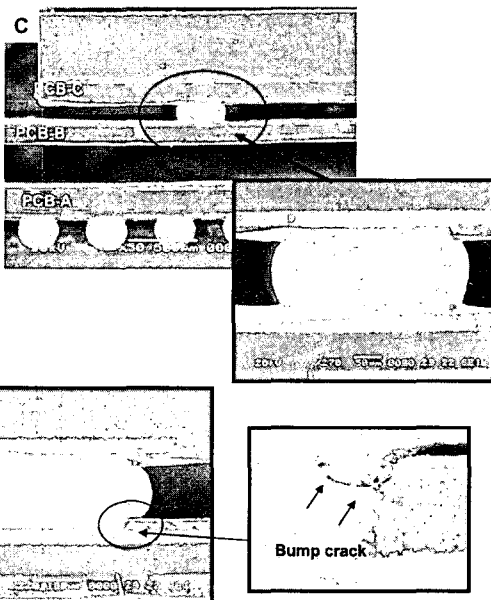
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SEM Analysis_3 Stack NAU-8



X-section 2



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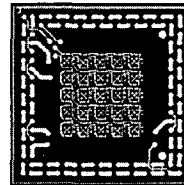
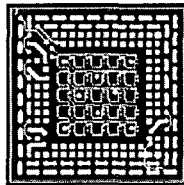
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Design Modifications_PSfcCSP

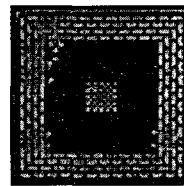
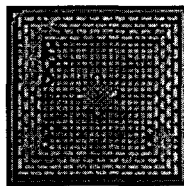


	1st	2nd
sub. thk.	0.26mm	0.26mm
core mat'l	HL-832-HS	HL-832-NB
core thk.	0.06mm	0.06mm

Top



Bottom



Design I
Spot dummy

Design II
No dummy

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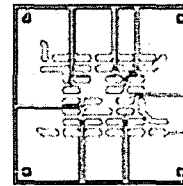
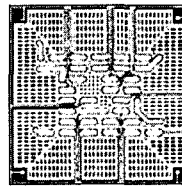
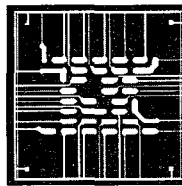
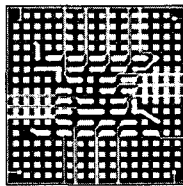
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Design Modifications_Interposer

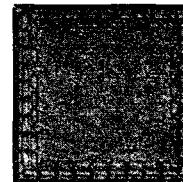
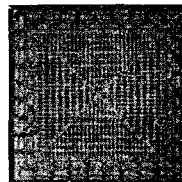
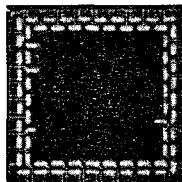
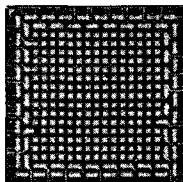


	1st	2nd
sub. thk.	0.16mm	0.21mm
core mat'l	HL-832-HS	HL-832-NB
core thk.	0.06mm	0.1mm

Top



Bottom



Design A
Spot dummy

Design B
No dummy

Design C
Line type dummy

Design D
Solid dummy

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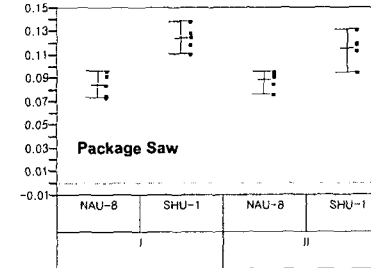
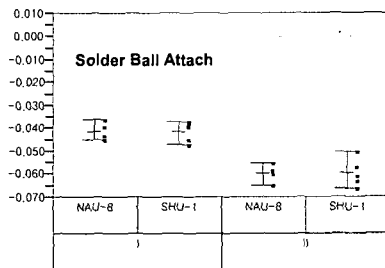
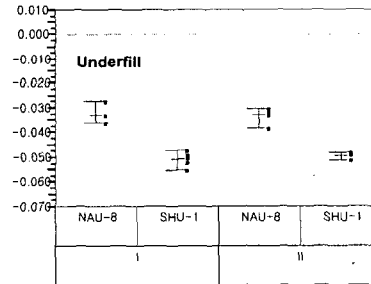
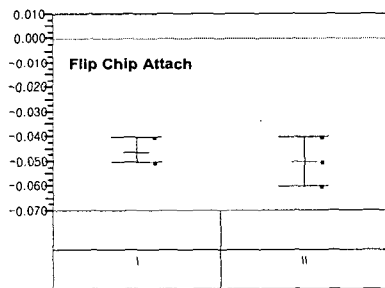
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Evaluation Legs

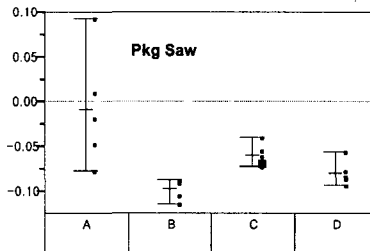
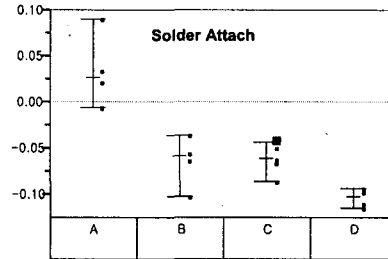
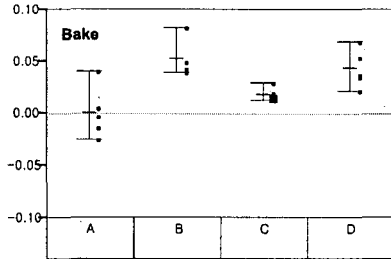


Leg	PSfcCSP	Underfill	Interposer
1	I	NAU-8	A
2	I	NAU-8	B
3	I	NAU-8	C
4	I	NAU-8	D
5	I	SHU-1	A
6	I	SHU-1	B
7	I	SHU-1	C
8	I	SHU-1	D
9	II	NAU-8	A
10	II	NAU-8	B
11	II	NAU-8	C
12	II	NAU-8	D
13	II	SHU-1	A
14	II	SHU-1	B
15	II	SHU-1	C
16	II	SHU-1	D

Warpage_PSfcCSP



Warpage_Interposer

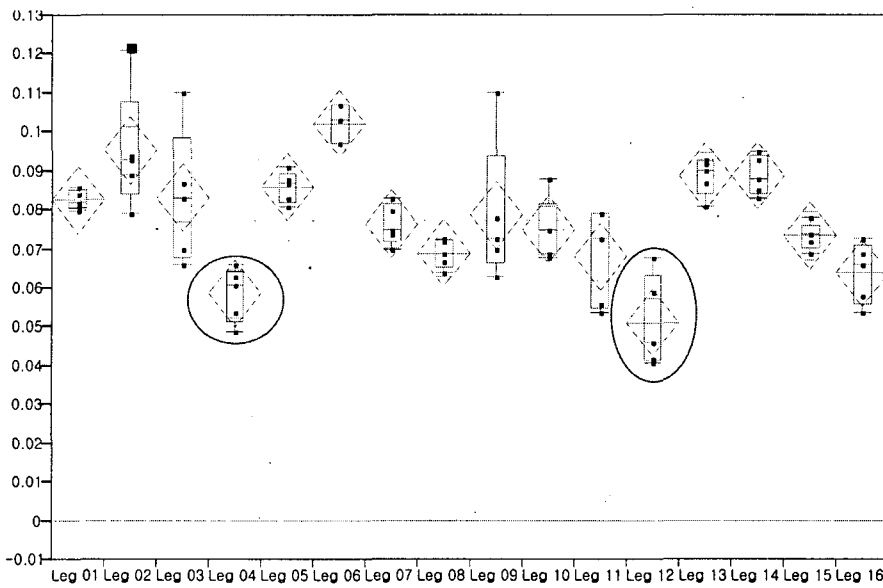


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Warpage After Stacking

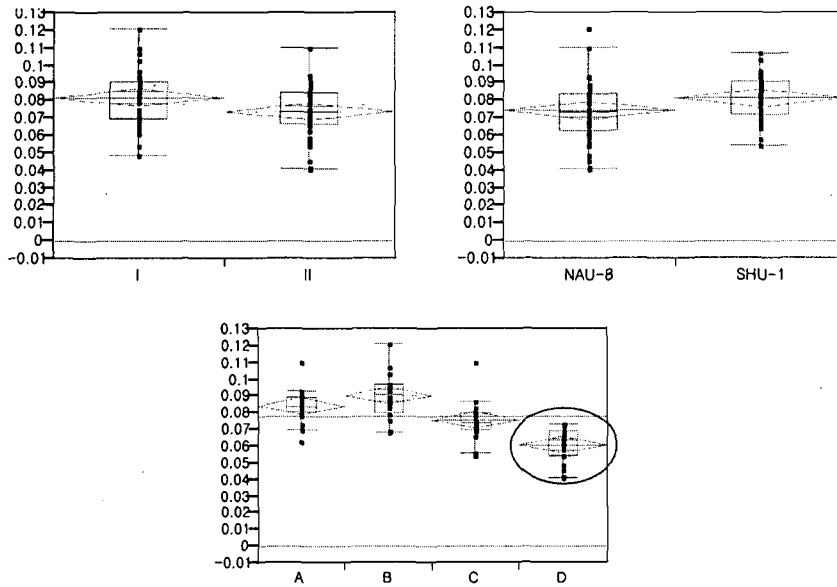


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Warpage After Stacking



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Summary_PSfcCSP Warpage



- Before stacking

	Warpage		
	PSfcCSP	Interposer	Underfill
Bake	-	C	-
Flip Chip Attach	I >= II	-	-
Underfill	I or II	-	NAU-8
Solder Attach	I	C	NAU-8 or SHU-1
Package Saw	I or II	C	NAU-8
Selection	I	C	NAU-8

- After stacking

Best	Hisomet	Coplanarity
Leg #	leg 4 or 12	leg 4 or 12
PSfcCSP	I or II	I or II
Interposer	D	D
Underfill	NAU-8	NAU-8

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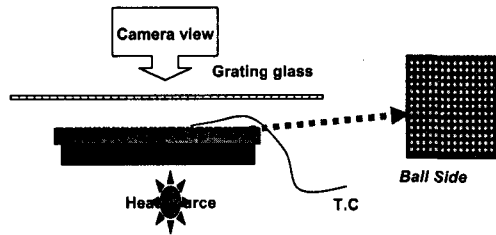
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PSfcCSP Warpage By Shadow Moire



- Equipment : TheirMoire PS88
- Reading Points : RT-150°C-200°C-230°C-245°C-260°C



Temperature Profile Test Setup

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PSfcCSP Warpage By Shadow Moire



- PSfcCSP behavior by reflow temp



- Interposer behavior by reflow temp



- PSfcCSP + Interposer behavior by reflow temp

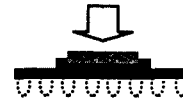
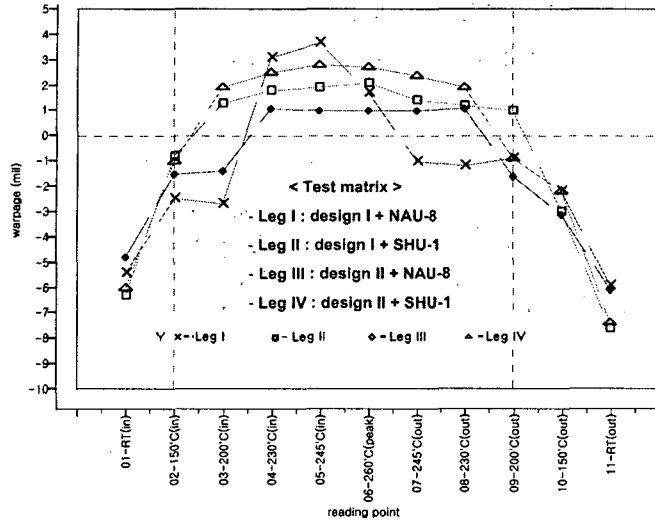


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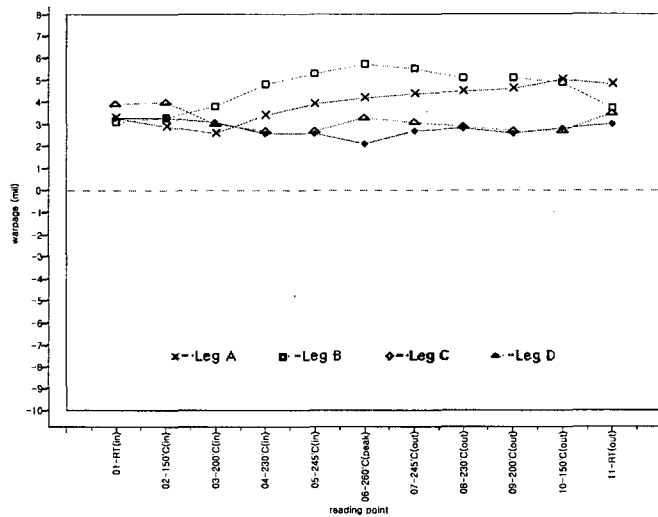
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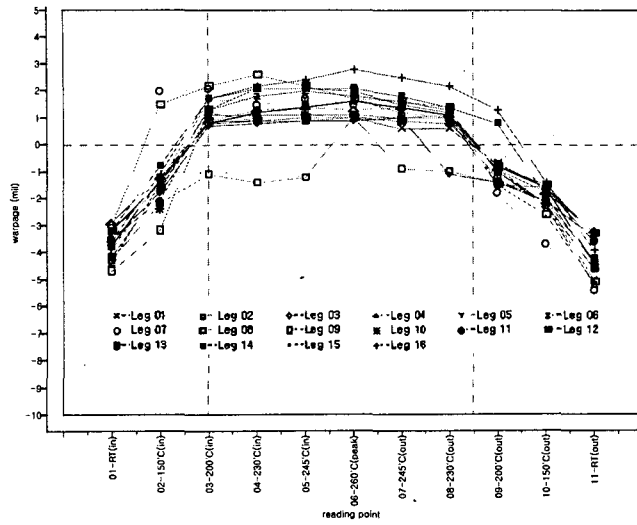
Warpage Behavior by Reflow Temp - PSfcCSP



Warpage Behavior by Reflow Temp - Interposer



Warpage Behavior by Reflow Temp- PSfcCSP + Interposer

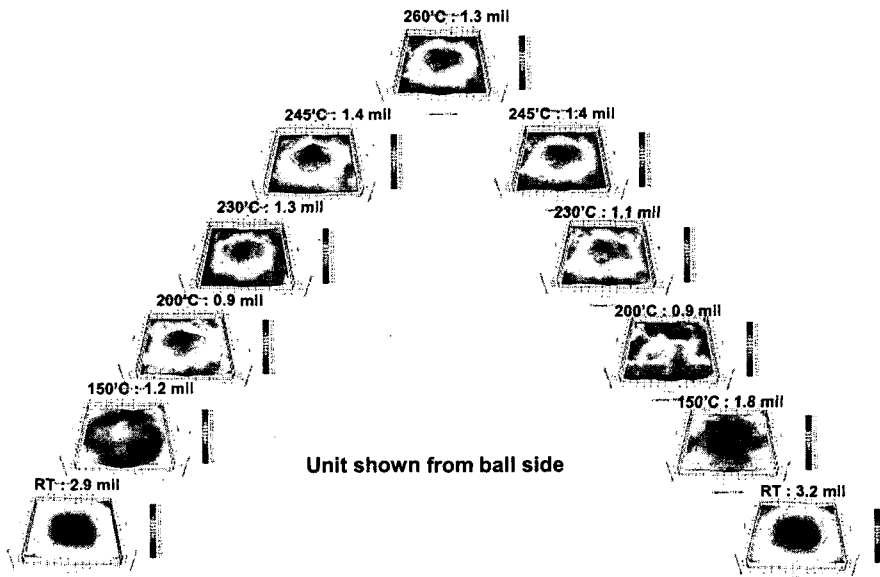


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Reference - Leg 4

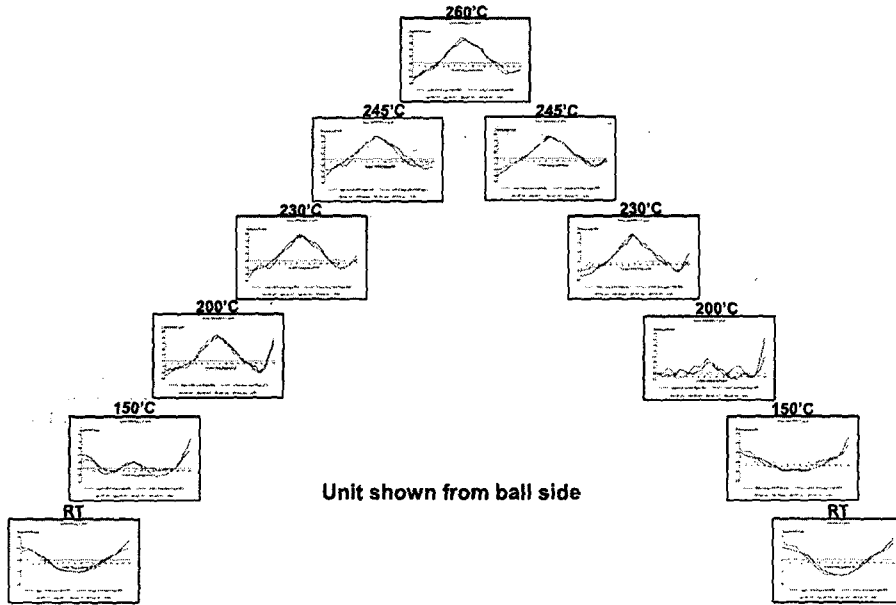


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Reference - Leg 4

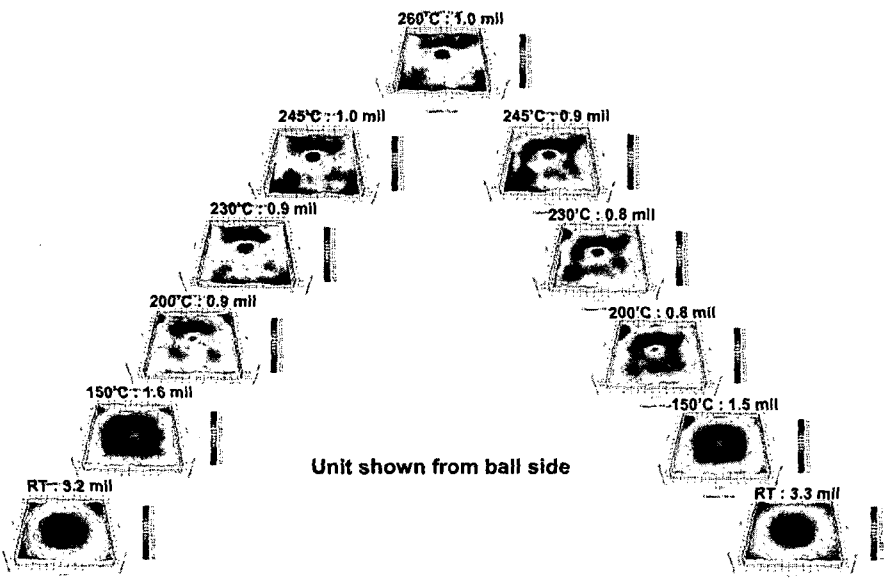


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Reference - Leg 12

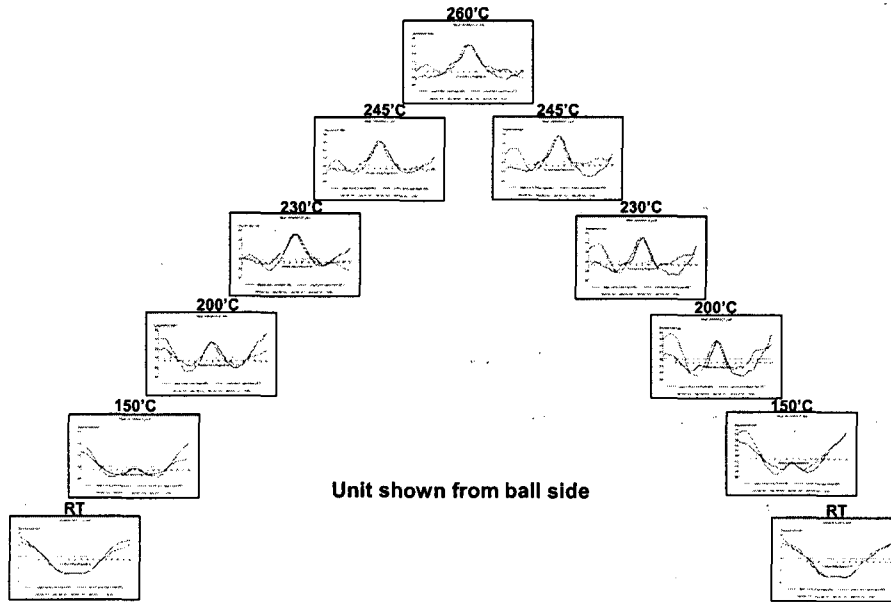


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Reference - Leg 12



Unit shown from ball side

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2L PSfcCSP



• BOM

- Substrate:
 - PSfcCSP: 0.1mm core, 2L, 0.21mm T
 - Interposer: 0.1mm core, 2L, 0.21mm T
- Flux for Flip Chip: INF-1
- Underfill: NAU-8, SHU1
- Solder ball
 - Lead free LF35 (Sn/Ag1.2/Cu0.5/Ni0.05)
 - PSfcCSP : 0.3 mm dia.
 - Interposer : 0.4 mm dia.

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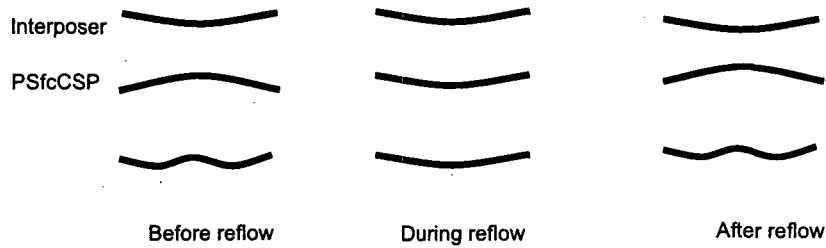
February 2008

2L PSfcCSP_Unit Warpage By Shadow Moire



• Warpage Findings

- Interposer integration with PS-fcCSP is in smile shape in general.
- But, in area of center ball, it is shown as crying shape. And it is not changed at high temperature

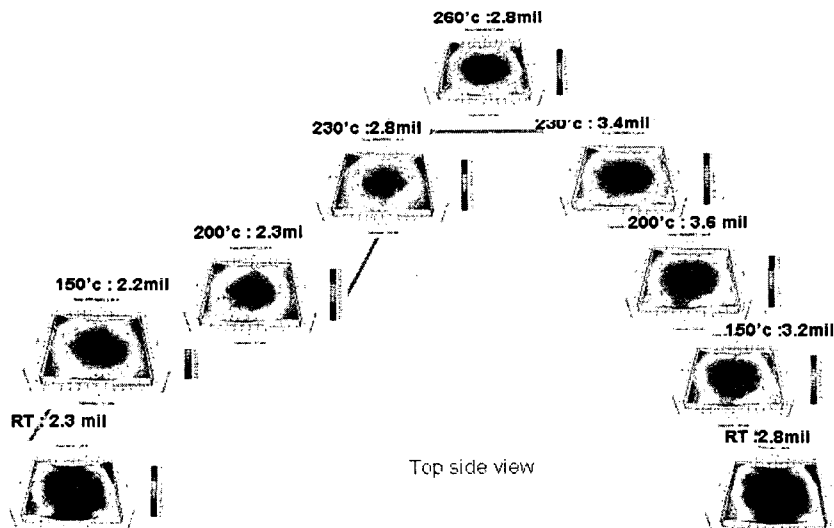


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Warpage of Integrated PSfcCSP – NAU8

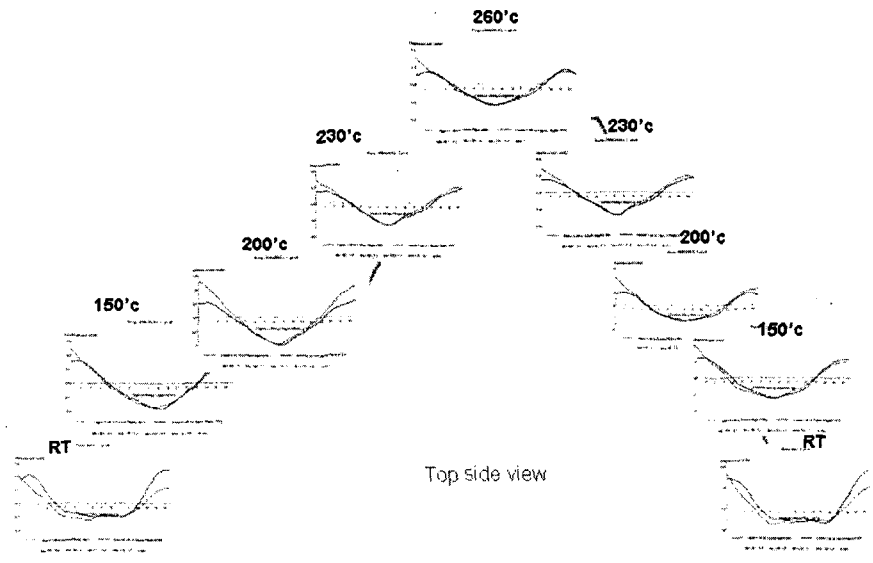


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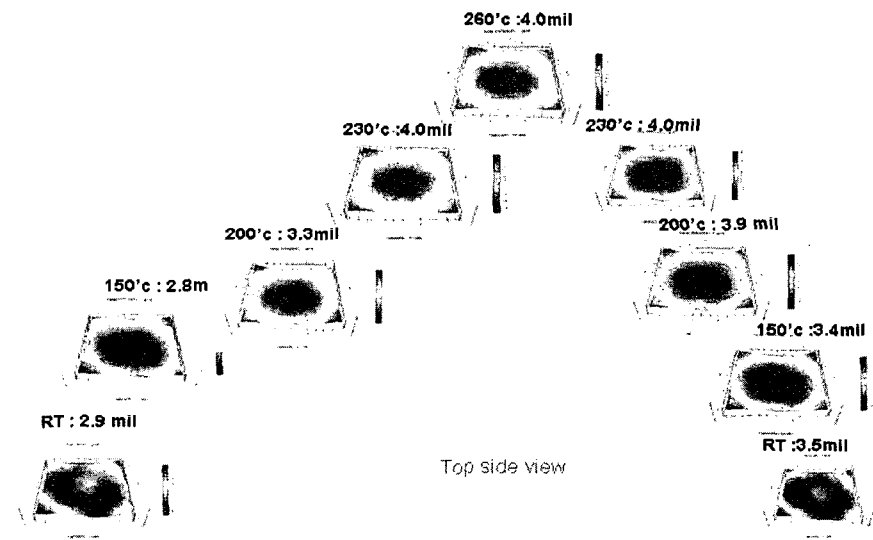
February 2006

Warpage of Integrated PSfcCSP – NAU8



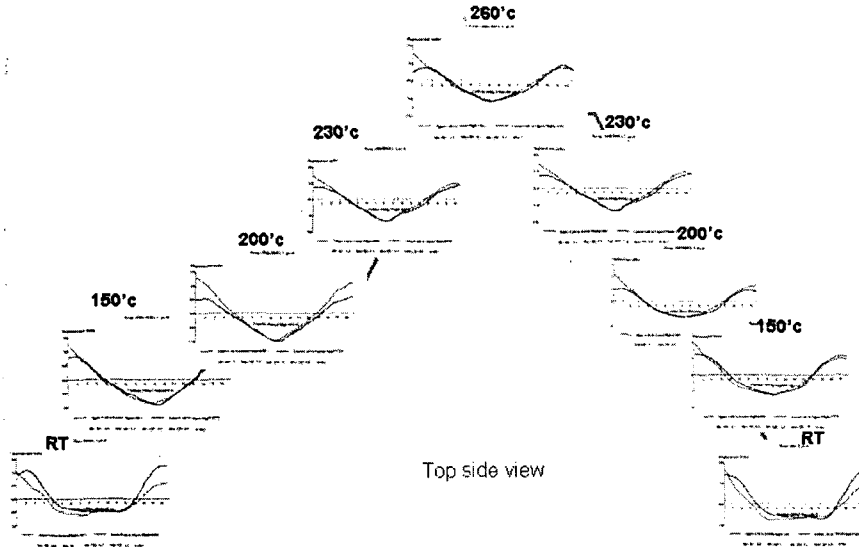
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Warpage of Integrated PSfcCSP – SHU1



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Warpage of Integrated PSfcCSP – NAU8

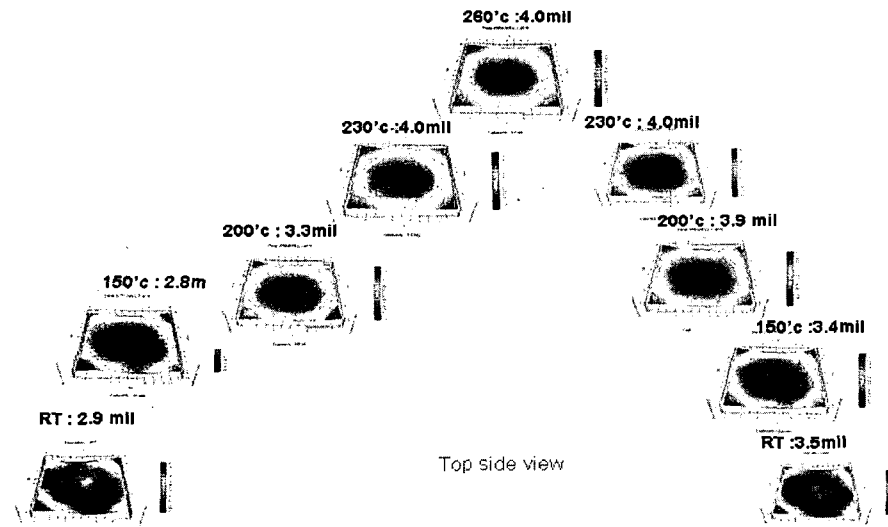


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Warpage of Integrated PSfcCSP – SHU1

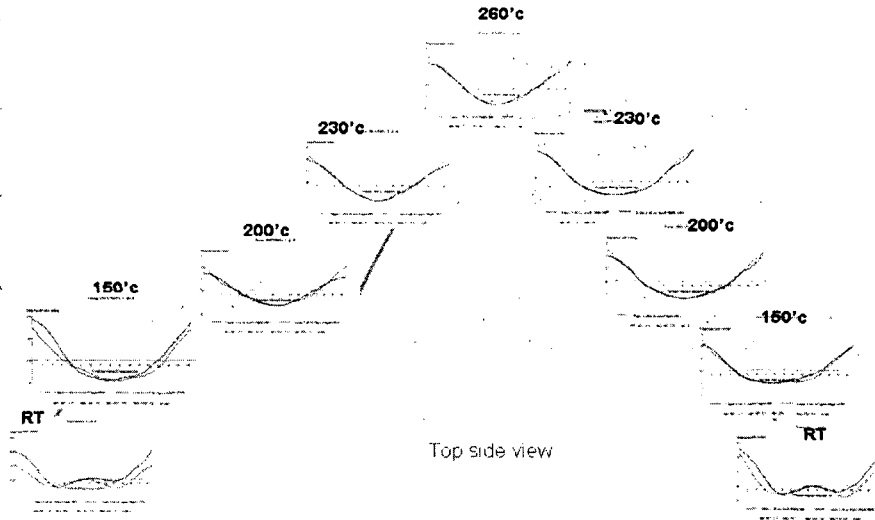


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Warpage of Integrated PSfcCSP – SHU1



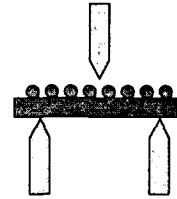
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PSfcCSP_Die Strength

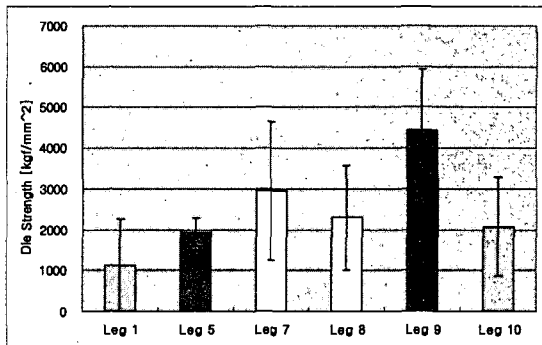


Matrix

	Polished	Wavelength	Making Type
Leg 1	Yes	1064nm	White
Leg 5	Yes	532nm	White
Leg 7	Yes	532nm	Black
Leg 8	No	532nm	Black
Leg 9	Yes	No marking	N/A
Leg 10	No	No marking	N/A



Result



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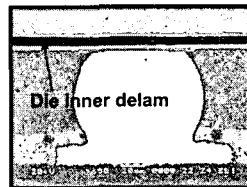
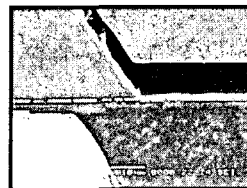
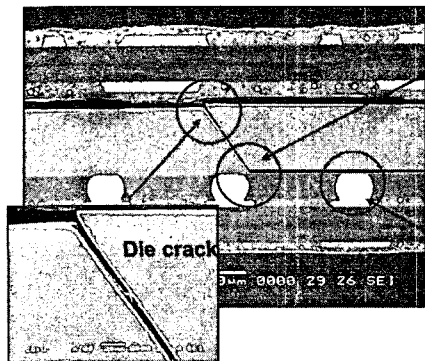
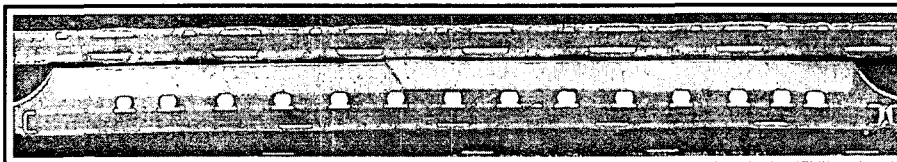
**PSfcCSP Reliability Performance
by Saw Method & Laser Mark**



- **MRT(30'C/60%RH, 192H)**
 - Leg B Failed
 - Leg C, D, E, F & G Passed
- **TC(-55'C/125'C, 500X&1000X)**
 - Leg D, E, F & G Passed
- **HAST(130'C/85%RH, 96&192H)**
 - Leg D, E, F & G Passed

Leg	Remark	UF
B	Face down saw + old laser mark (Nd-YAG 1064um wave)	NAU8
C	Face up saw + old laser mark (Nd-YAG 1064um wave)	NAU8
D	Face up saw + no laser mark	NAU8
E	"	SHU1
F	Face up saw + new laser mark (Nd-YAG 532um wave)	NAU8
G	"	SHU1

SEM Inspection_Leg B



PSfcCSP BLR Performance – Customer Data



		A	B	C	
Bend (3point)	First Failure	4850	2717	3650	
Drop	First Failure	296	226	191	
	N (10%)	443	292	263	
	N (63%)	658	378	369	
	Failure Location	Base to board	Major	Major	Major
		Top to base	N/A	Minor	N/A
		Top to interposer	N/A	N/A	Minor
		Interposer to base	N/A	N/A	Minor

Note

No chip crack

A Base only

B Base + Top

C Base + Interposer + Top