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$Pt/SrBi_2Nb_2O_9/Pt/Y_2O_3/Si$ 게이트 구조를 가지는 MFMISFET 의 제작 및 특성

Fabrication and characterization of MFMISFETs with $Pt/SrBi_2Nb_2O_9/Pt/Y_2O_3/Si$ gate structure.

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Ferroelectric memories have attracted considerable interest for future memory applications because of several advantages such as faster write speeds, lower operating voltages and a high level of integration by using a simple structure

The single transistor type ferroelectric random access memories (1T type FeRAMs) with MFMIS gate structures were fabricated and characterized in this work

To enhance the electrical properties of the single transistor type ferroelectric memory, MFMIS gate structures with different area ratios between ferroelectric capacitor and insulating capacitor were applied The 280nm-$SrBi_2Nb_2O_9$(SBN) film (crystallization process was done oxygen plasma RTA) was used as ferroelectric gate material, and 20nm-Y_2O_3 were used as insulator The memory window increased from 0 53 V for S_F/S_I = 1 1 and 1 97 V for the S_F/S_I = 1 7 with the gate applied voltage of 5 V The memory window was much improved comparing with the MFS and MFIS structures whose value was 0 61 and 0 93 V, respectively.

As a result, the MFMISFET [S_F/S_I ratio = 1 3] with $Pt/SBN/Pt/Y_2O_3/Si$ gate structure showed the good counter-clockwise hysteresis loops, and the threshold voltage differences of were 0 91 and 1 91 V for the applied gate voltage of 5 and 7 V The on/off ratio increased as the writing voltage increased and the maximum value of the on/off ratio was at the read voltage of 2 0 V The on/off ratio was 10, 280 and 4100 at the 3V, 5V and 7V operation, respectively