Design of Half-Bridge Piezo-Transformer Converters in the AC Adapter Applications

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ABSTRACT

As a viable alternative to magnetic transformers in the power supply for portable electronics, this paper presents a miniaturized off-line travel adapter or charger for cellular phones using the piezoelectric transformer. Various design considerations in the design of ac PT adapters are investigated before coming up with the proposed pseudo-resonant topology. A prototype hardware design is also presented and verified by simulations and experiments

I. Introduction

As the piezoelectric transformer(PT) technology develops, PTs may become a viable alternative to magnetic transformers in various applications. Power supplies that employ PTs, rather than the classical magnetic transformers[1,2], could be made smaller in size. This paper presents a miniaturized off-line travel battery charger for cellular phones using the piezoelectric transformer as a main energy transferring component in the ac-dc adapter[9].

The schematic diagram of a piezoelectric transformer adapter is presented in Fig. 1. An inverter is used to drive the PT whose driving frequency is determined by the PT's mechanical resonant frequency and the gain characteristic of the PT.

Figure. 1 was shown in [4,5] that by using specific characteristics of the PT with a half-bridge topology, ZVS could be achieved without any additional elements. This scheme may be useful when the load impedance is nearly fixed, as in the lamp ballast case. However, it utilizes avery narrow inductive region, which is highly dependent on the load impedance variations, and thus, this scheme cannot be applied to wide load range applications such as AC adapters. Therefore, some PT primary circuits adopt additional series inductors to achieve the ZVS condition and the waveform shaping (Ls-type)[11]. The resonance formed by the series inductor and the internal input capacitance of the PT. However, a bulky series inductor has to be designed to provide both the primary side current and the ZVS current. Thus, the PT advantages of small size were inadvertently lost. Some papers[8] have utilized half-bridge pseudo-resonant branches to provide the soft-switching characteristics. This scheme has been derived from the topological classification that has been referred to as the zero-voltage-switching clamped-voltage(ZVS-CV),partial-resonant, quasi-square wave, or the resonant transition topologies [7].

In this paper, the pseudo-resonant (Cs-Lp type) half-bridge converter is adopted. In this circuit, the capacitance, Cs, together with the parallel inductance, Lp, are considered to be the parameters to be optimally designed so as to provide a nearly sinusoidal waveform to the PT. By this design process, reduced switching losses and efficient PT energy conversion are obtained simultaneously in offline applications.

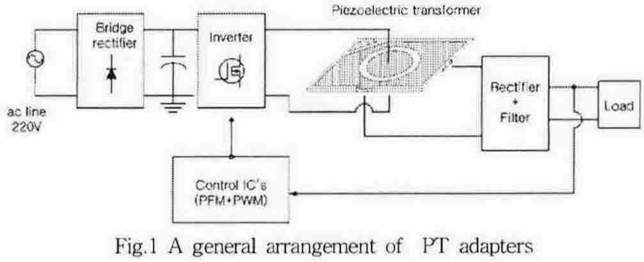

Fig.1 A general arrangement of PT adapters

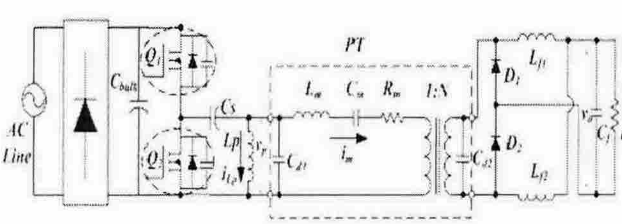

Fig.2 The Cs-Lp type half bridge ac adapter using PT

II. Principle of Operation and Design of the Half-Bridge PT Adapter

1.1 Analysis of the pseudo-resonant inverter

The mode of operations and their corresponding waveforms are illustrated in Fig.3. The gate drive waveform contains a sufficient deadtime for the ZVS condition. In this section, detailed analysis and the derivation of the design equation is performed.

1.1.1 During the switch ON/OFF

During the MOSFET switch on or off stage, the series capacitance, Cs, resonates with the parallel inductance, Lp, which provides a nearly sinusoidal voltage to the PT primary side.

When the high-side switch is turned on at t=t1, the primary voltage of the PT and the parallel inductor current are given by

$$v_P(t) = K\omega \cdot sin[\omega(t-t_1)] + V_{po} \cdot cos[\omega_O(t-t_1)] - [Z_O(I_{Lpo}+I_m) + K\omega] sin[\omega_O(t-t_1)]$$

$$i_{Lp}(t) = K\omega \cdot cos[\omega(t-t_1)] + [I_{Lpo}-K] \cdot cos[\omega_O(t-t_1)] + \frac{V_{po}}{Z_O} sin[\omega_O(t-t_1)] \quad (1)$$

$$A = \frac{I_m}{1-(\frac{\omega_o}{\omega})^2}, \omega_o = \frac{1}{\sqrt{L_p(C_s + C_{d1})}}, Z_o = \sqrt{\frac{L_p}{C_s + C_{d1}}}$$

Where ω is the switching frequency of the circuit.

1.1.2 During the Dead-time

The ZVS condition is achieved by using a parallel inductor, Lp. Thus the voltage waveform of the drain to source terminal is a quasi-square waveform.

Assuming that the current in the parallel inductor, i_{Lp}, is constant during the short transition time, there should be a sufficientcurrent to transit the voltage on the drain-to-source capacitor before the next gate pulse is applied. Thus, the minimum required current (Ireq) is given by,

$$I_{req} = C_{eq}\frac{V_{dc}}{Td}, \; C_{eq} \approx C_{ds1} + C_{ds2} + C_{d1} \quad (2)$$

where Vdc is the voltage rectified from the ac line, Td is the dead-time period, Cd1 is the PT primary electrode capacitance, and Cds1 and Cds2 are the parasitic capacitances of Q1 and Q2, respectively.

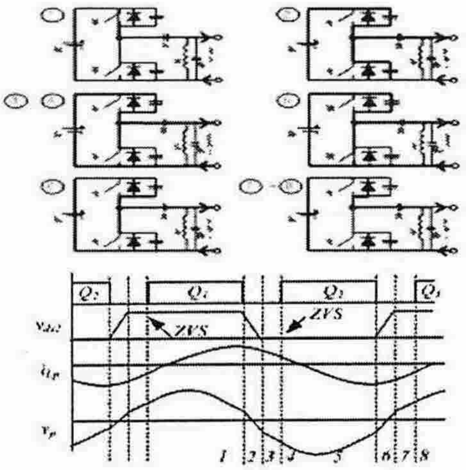

Fig.3 Waveforms and operation modes of the PT driving circuit

When Cs is relatively large, the resonant voltage, vp(t), can be approximated by the fundamental harmonic of magnitude of Vpm given by

$$V_{pm} \approx V_{dc} \cdot \left(\frac{2}{\pi}\right) \cdot \frac{\sin(\pi \frac{T_d}{T})}{\pi \frac{T_d}{T}} \quad (3)$$

Here it is assumed that the switching frequency of the converter is near theresonant frequency of the PT. The PT input current will cross zero during the dead-time. Therefore, the inductor current in the beginning of the dead-time region determines the ZVS operation, and can be approximated by

$$I_{Lpo} = (\frac{2}{\pi})\frac{sin(2\pi\frac{Td}{T})}{2\pi\frac{Td}{T}} \cdot \frac{V_{dc}}{2\pi \cdot f \cdot L} \quad (4)$$

where T=1/f is the switching period.

From (2) to (4),an inductance value for the ZVS is derived. The maximum Lp should be designed to be

$$L_p \le \left(\frac{2}{\pi}\right) \cdot \frac{\sin(2\pi\frac{T_d}{T})}{2\pi\frac{T_d}{T}} \cdot \frac{T_d \cdot T}{2\pi \cdot C_{eq}} \quad (5)$$

III. Hardware Implementation and Performance Analysis

The specifications of the target system are :

AC input voltage : 220 10 % [Vrms]

Regulated output voltage : 5 V

Maximum output current : 1 A

Power stage components are :

. Bulk capacitor : 400V 4.7uF Electrolytic

. MOSFET : FQD2N40/FQD2P40

Resonant tank :

. Cs=3.2nF(1kV ceramic), Lp=2.7mH(Axial 7)

. Piezo Transformer : PZT #4A-1 (Dong-il Tech.)

. Output inductor : 100uH/0.5A SMD (TDK)

. Output capacitor : 220uF/10V SMD Tantal

Control stage consists of :

. Controller : TL494 with external VCO circuit

. Frequency control range : 131kHz<f<140kHz

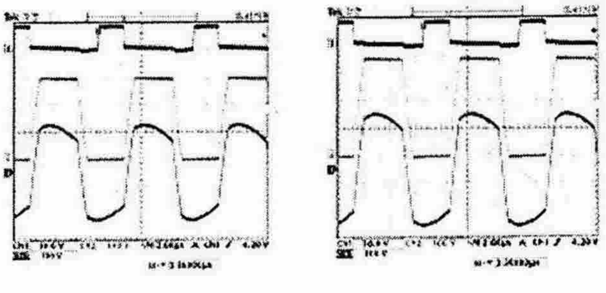

Figure.4 Hardware waveforms
(ch1: low side gate, ch2: drain-to-source voltage, ch3: PT primary voltage)

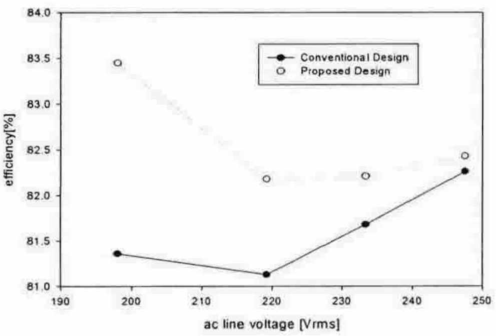

Fig.5 Efficiency of the PT vs line (Maximum load condition)

Figure 4 shows the PT driving circuit waveforms in the two extreme input conditions. As predicted from the analysis, Figure 5 shows the performance of the hardware system. With the proposed resonant driving method, increase of PT operating efficiency of 1~2% was obtained.

IV. Conclusion

This paper presents a pseudo-resonant topology which is suitable for the off-line piezo-adapter. The proposed topology provides a nearly sinusoidal voltage on the primary side of the PT to reduce the circulating energy utilizing a partial resonance during the dead-time. The resonance characteristics provide additional gain of the inverter which eases the PT voltage gain design. During the gate dead-time, the parallel inductor branch also provides a ZVS condition to both of the main switch pairs. A design of the ac piezo-adapter using the above topology is also presented and verified by simulations and experiments.

이 논문은 산업자원부 와 삼황양행의 연구비 지원에 의하여 연구되었슴

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