PDP 유지전원단을 위한 높은 효율을 갖는 새로운 페이지쉬프트 풀브릿지 컨버터

이우진, 김정은, 한상규, 문건우
한국과학기술원

A New High Efficiency Phase Shifted Full Bridge Converter for Sustaining Power Module of Plasma Display Panel

Woo-Jin Lee, Chong-Eun Kim, Sang-Kyoo Han, Gun-Woo Moon
Korea Advanced Institute of Science and Technology (KAIST)

요 약

PDP 유지전원단을 위한 고효율을 갖는 새로운 페이지 쉬프트 풀브릿지 컨버터를 제안한다. 제안된 컨버터는 Rectifier로 Voltage Doubler를 사용함으로서, 큰 사이즈의 Output Inductor가 없게 되어 간단한 구조를 가지게 되며 Rectifier Diodes의 전압 스트레스가 출력전압으로 클램핑되어서 스너버회로가 필요없다는 장점을 가지게 된다. 또한 넓은 영전압 스위칭 구간을 가지며, 트랜스포머의 기생성분인 Leakage 인덕터와 Voltage doubler의 캐패시터간의 공진을 이용함으로서 전류가 작은 RMS 값을 가지게 되어서 낮은 도통손실과 Rectifier Diode의 전류 스트레스 또한 낮다는 장점을 가지게 된다. 본 논문을 통해 제안된 컨버터의 동작원리와 해석, 실험을 수행하였다.

ABSTRACT

A new high efficiency phase shifted full bridge (PSFB) converter for sustaining power module of plasma display panel (PDP) is proposed in this paper. The proposed converter employs the rectifier of voltage doubler type without output inductor. Since it has no output inductor, the voltage stresses of the secondary rectifier diodes can be clamped at the level of the output voltage. Therefore, no dissipative resistor-capacitor (RC) snubber for rectifier diodes is needed and a high efficiency as well as low noise output voltage can be realized. In addition, due to elimination of the large output inductor, it features a simple structure, lower cost, less mass, and lighter weight. Furthermore, the proposed converter has wide zero voltage switching (ZVS) ranges with low current stresses of the primary switches. Also the resonance between the leakage inductor of the transformer and the capacitor of the voltage doubler cell makes the current stresses of the primary switches and rectifier diodes reduced. In this paper, the operational principles, analysis of the proposed converter, and the experimental results are presented.

1. INTRODUCTION

A plasma display panel(PDP) is getting popular for the large area wall-hanging color TVs, because it has advantages over conventional display devices by its large screen, wide view angle, lightness, thinness, long life time, and high contrast. Since the recent wall hanging PDP color TV tends to require the small size, lighter weight, and fan-less system for the lower acoustic noise and vibration, the high power density, high performance, and high efficiency become the hot issue of the PDP power module. The operation of the PDP can be divided into three periods such as resetting, addressing, and sustaining periods. The power modules for sustaining are expecially responsible for the overall system efficiency, since the most of the power driving the PDP is consumed during this sustaining period.[1-3] Therefore, among the various DC/DC converters developed, a full bridge converter suitable for the application like the PDP power module has been proposed to reduce the current/voltage stress of the semiconductor devices. However, it has several serious problems such as low system efficiency, serious parasitic ringing in the

secondary rectifier, considerable heating, bulky cooling system, and noisy output voltage. To resolve these problems, the proposed converter employs the rectifier of voltage doubler which has no output inductor. Due to eliminate the output inductor, the voltage stresses of the secondary rectifier diodes can be clamped at the level of the output voltage and the structure is even simpler. Therefore, no dissipative RC(resistor capacitor) snubber for rectifier diodes is needed and a high efficiency as well as low noise output voltage can be realized. Moreover ZCS turn off of the rectifier diode can be achieved. The ZVS turn on of the primary switches also can be easily achieved by using the magnetizing current regardless of the load condition. However, the current stresses of the rectifier diodes D1 and D2 are rather large because of the half bridge configuration, the resonance between Llkg and the capacitors of the transformer secondary side can reduce not only the current stresses of the secondary rectifiers but also the conduction loss of the primary side. Thus, the proposed converter, which is suitable for high voltage and low current application, can effectively overcome the above problems and realize the high power density, high performance, and high efficiency.

2. OPERATIONAL PRINCIPLES

Fig. 1 shows the circuit diagram and key waveforms of the proposed converter, respectively. As shown in Fig. 1, the proposed converter is the phase shifted full bridge converter with the voltage doubler type rectifier stage. The operation of the proposed converter can be divided into eight modes. One switching cycle of a proposed circuit is divided into two half cycles, t_0-t_4 and t_4-t_8. Since the operation principles of two half cycles are symmetric, only the first half cycle is explained.

Mode 1 (t_0~t_1): After the ZVS condition of M_4 is achieved (V_{DS4} = 0V), the primary current, I_{pri}, rises with resonance between the leakage inductor and rectifier capacitor. The magnetizing current, I_{Lm}, also rises linearly. These can be obtained by

$$I_{pri}(t) = I_{Lm}(t)\cos\omega_r(t) + \left(\frac{(V_{in} - nV_{o1})}{Z_o}\right)\sin\omega_r(t), \quad (1)$$

$$I_{Lm}(t) = I_{Lm}(t_0) + \frac{nV_{o1}}{L_m}(t), \quad (2)$$

where, $\omega_r = \frac{n}{\sqrt{L_{lkg}C_t}}$, $Z_o = \frac{1}{n}\sqrt{\frac{L_{lkg}}{C_t}}$, $n = \frac{N_p}{N_s}$, $C_t = C_{o1} // C_{o2}$.

Before M_4 is turned on, I_{pri} flows through the internal diode of M_4. Thus, the ZVS of M_4 is guaranteed. The current of the rectifier diode D_1, I_{D1}, flows through C_{o1}. Therefore the rectifier capacitor $C_{o1}$is charged, while C_{o2} is discharged.

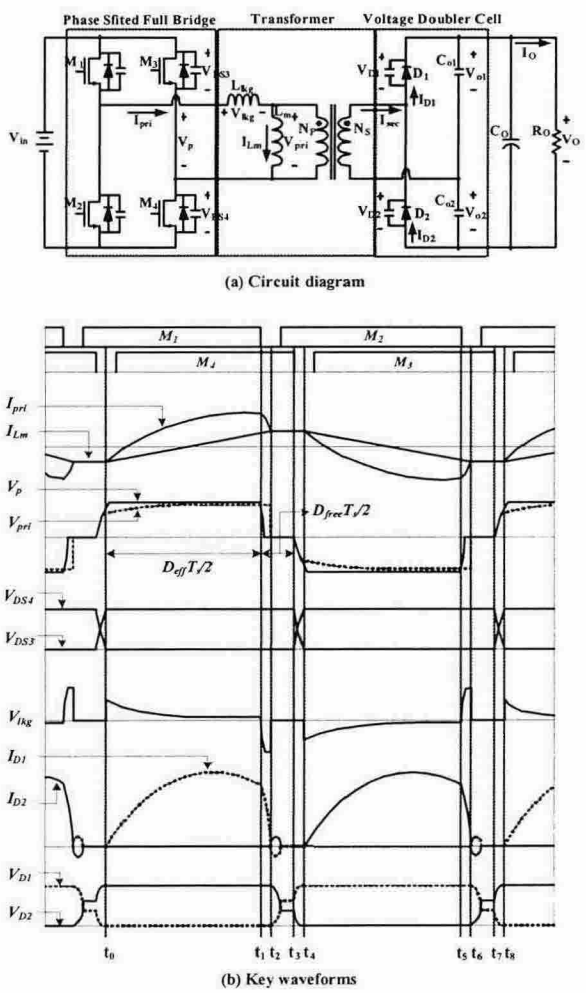


그림 1. 제안된 페이지쉬프트 풀브릿지 컨버터
Fig. 1 The proposed PSFB converter

Mode 2 (t_1~t_2): When M_1 is turned off at t_1, mode 2 begins. The primary current at t_1, $I_{pri}(t_1)$ start to

charge and discharge the output capacitors of M_1 and M_2 respectively. Therefore the voltage across the transformer primary side V_p, is decreased to 0V and the voltage across L_{lkg}, V_{lkg}, is also decreased. After V_{lkg} is the same as $nV_{o1}(=V_{pri})$, the primary current is decreased with the slope of nV_{o1}/L_{lkg}. At the same time, the secondary side of the transformer operates similarly to mode 1.

Mode3(t_2~t_3): When the primary current I_{pri} becomes equal to the magnetizing current I_{Lm}, mode 3 begins. Since the diode current, I_{D1}, is reduced to zero, ZCS turn-off of D_1 can be obtained. During this mode, D_1 and D_2 are off-state with voltages V_{o1} and V_{o2}, respectively. After $M_2$is turned on, the voltage across the primary of the transformer V_p is maintained to 0V. The primary current I_{pri} is still equal to $I_{Lm}(t_2)$.

Mode4(t_3~t_4): After $M_4$is turned off, the voltage across the primary of the transformer V_p is decreased to V_{in}. At t_4, the commutation between D_1 and D_2 is completed.

3. ANALYSIS

In order to the DC conversion ratio, it is assumed that the capacitors C_{o1}, C_{o2}, and output capacitor C_o are large enough to be considered as a constant voltage source V_{o1}, V_{o2}, and V_o repectively. Moreover, the magnetizing inductor L_m is so large that I_{Lm}=0, I_{pri} is increased linearly and the dead time is discarded. By averaging the current of secondary rectifier, the input-output voltage gain is expressed by

$$\frac{V_o}{V_{in}} = \frac{1}{\frac{4L_{lkg}}{nR_oT_sD_{eff}^2} + \frac{n}{2}} \tag{3}$$

where D_{eff} is the effective duty ration and T_s is a switching period.

To achieve the ZVS of switches, the energy E_{lkg_t1} stored in the leakage at t_1 must be greater than the energy required to charge and discharge the output capacitors (C_{oss}) of M_1 and M_2. Similarly the energy E_{Lm_t3} stored in the magnetizing inductor at t_3 must be large enough to fully charge and discharge C_{oss} of M_3 and M_4. Therefore, to assure the ZVS of switches M_1-M_4, the following equations must be satisfied.

$$E_{lkg\_t1} = \frac{1}{2}L_{lkg}I_{pri}(t_1)^2 \geq \frac{1}{2}2C_{oss}V_{in}^2 \tag{4}$$

$$E_{Lm\_t3} = \frac{1}{2}L_mI_{Lm}(t_3)^2 \geq \frac{1}{2}2C_{oss}V_{in}^2 \tag{5}$$

where the output capacitances of M_1-M_4 are assumed to be equal to C_{oss}.

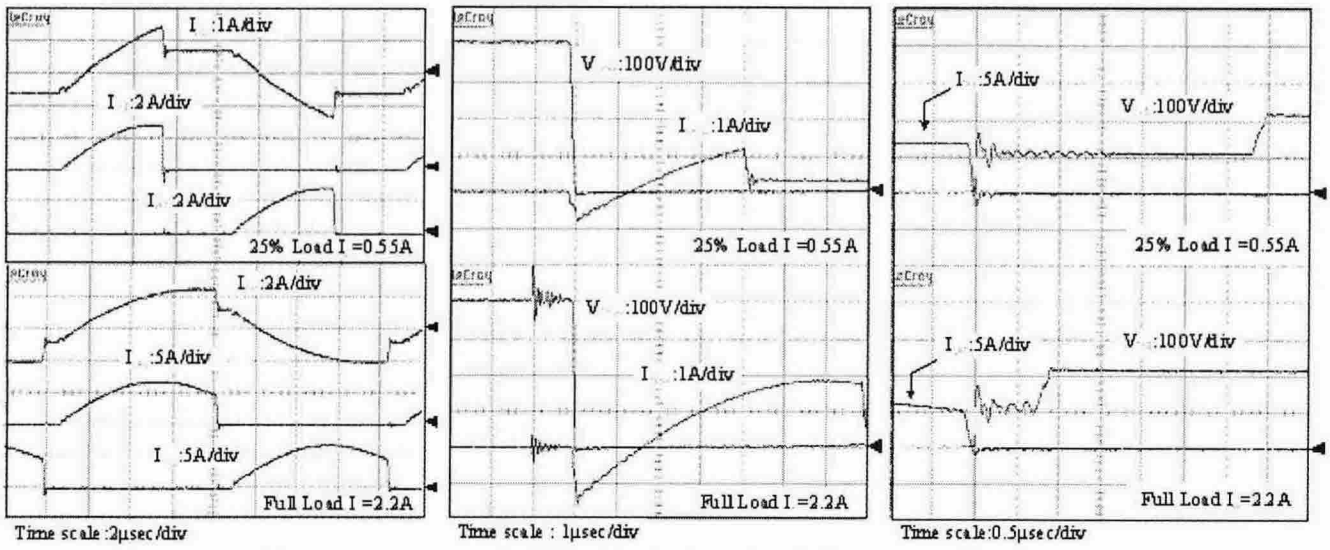
4. EXPERIMENTAL RESULTS

A prototype of a 205V, 450W converter operated at 60KHz with 400V input has been built with the following components; the switches M_1,M_2,M_3, and M_4=FQP12N60, output capacitor C_o=1000uF/250V, leakage inductance L_{lkg}=23uH, magnetizing inductance L_m=1.4mH, transformer turns N_p:N_s = 42:13, D_1 and D_2 = 15ETH03, C_{o1}=C_{o2}=2.2uF/630V.

Fig. 2 shows the experimental waveforms at 25% and full load. As can be seen in Fig. 2, the ZVS of the power switches can be easily achieved using the magnetizing current regardless of the load conditions. Since the voltages across D_1 and D_2 are always clamped at the output voltage V_o, there is no serious voltage ringing in rectifier diodes. Furthermore ZCS turn off can be achieved. The waveforms of I_{D1} and I_{D2} are not a triangular form but a quasi-sinusoidal one. This result in the low current stresses of D_1 and D_2 and also less conduction loss of the primary side. In addition, the DC offset of the transformer magnetizing current and magnetic flux are completely blocked. Therefore, the transformer magnetic core is fully utilized, and thus, its power density can be considerably increased and the heat generation of the transformer greatly reduced. Also the currents of I_{D1} and I_{D2} are balanced.

5. CONCLUSION

A new high efficiency phase shifted full bridge converter for PDP sustaining power module is proposed in this paper. The proposed converter employs the rectifier of voltage doubler type without output inductor to solve the problem related to voltage ringing of the secondary rectifier. In addition, since it



(a) I_{pri}, I_{D1}, and I_{D2} (b) ZVS of lagging leg switch (M_4) (c) ZCS of rectifier diode (D_1)

그림 2. 주요 실험 파형

Fig. 2. Kew experimental results

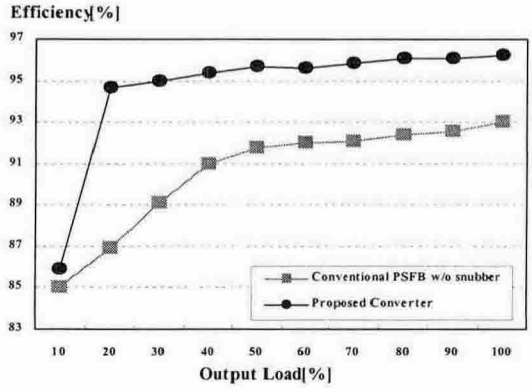


그림 3. 측정 효율

Fig. 3. Measured efficiency

has no large output inductor filter, it features a simpler

structure, lower cost, less mass, and lighter weight. Furthermore, the proposed converter has the wide ZVS ranges with low current stresses of the primary switches. Also the resonance between the leakage inductor of the transformer and the capacitor of voltage doubler rectifier can reduce the current stresses of the primary switches and the rectifier diodes. A prototype has been experimented to prove the validity of the proposed converter. Fig. 3 shows the measured efficiency. The high efficiency above 95% can be obtained along a wide load range. Therefore, it can be realized the improvement of the efficiency and also the proposed converter is expected to be suitable for the sustaining power module owing to the high reliability, low noise, low cost, and high efficiency.

This work was supported (in part) by the Ministry of information & Communications, Korea, under the Information Technology Research Center (ITRC) Support Program.

References

[1] S.K.Han, J.Y.Lee, G.W.Moon, M.J.Youn, C.B.Park, N.S.Jung, and J.P.Park, "A New Energy-Recovery Circuit for Plasma Display Panel", *Electronics Letters*, 18th July 2002, Vol. 38, No. 15, pp 790-792.

[2] S.K.Han, G.W.Moon, and M.J.Youn, "Current-fed Energy-Recovery Circuit for Plasma Display Panel", *Electronics Letters*, 10th July 2003, Vol. 39, No. 14, pp.1035-1036.

[3] C.W.Roh, H.J.Kim, S.H.Lee, and M.J.Youn, "Multilevel Voltage Wave-Shaping Display Driver for AC Plama Display Panel Application", *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 6, June 2003, pp. 935-947.