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Virtual Qualification을 통한 자동차용 전장부품의 수명 평가

Life Assessment of Automotive Electronic Part using Virtual Qualification

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Key Words : Reliability(신뢰성), Failure mechanism(고장메커니즘), Fatigue life(피로수명), Solder joint, Virtual Qualification

ABSTRACT

In modern automotive control modules, mechanical failures of surface mounted electronic components such as microprocessors, crystals, capacitors, transformers, inductors, and ball grid array packages, etc., are major roadblocks to design cycle time and product reliability. This paper presents a general methodology of failure analysis and fatigue prediction of these electronic components under automotive vibration environments. Mechanical performance of these packages is studied through finite element modeling approach for given vibration environments in automotive application. Using the results of vibration simulation, fatigue life is predicted based on cumulative damage analysis and material durability information. Detailed model of solder/lead joints is built to correlate the system level model and obtain solder strains/stresses. The primary focus in this paper is on surface-mount interconnect fatigue failures and the critical component selected for this analysis is 80 pin plastic leaded microprocessor.

1. Introduction

In the last 25 years, the use of electronics into automobiles has seen a phenomenal growth partly due to the rapid advancements in applicable technologies. The electronic systems in cars account for up to 30% of the manufacturing cost presently, a proportion that is set to rise. Reliability is difficult to achieve in automotive electronic products because of the long life cycles under harsh application environments. Automotive electronics has to be subjected to extensive and often conservative assurance methods to reduce the risk of failure and unsafe operation. Thus there is a need for accessing quantitative, proven design and validation tools for effective virtual qualification. Simulation has to be accepted as the in-thing for reduction in the design and development time and number of design iterations.

Virtual qualification is a failure prediction methodology based on the scientific determination of the dominant failure mechanisms and failure sites within the electronic component. The dominant failure mechanisms and failure sites are exposed by characterizing the stresses in the system using thermal or vibration analyses as inputs for analytical models derived from physical phenomena fundamental. Most of the time these physical processes from where the analytical models are developed are chemical, metallurgical, physical, or thermo-dynamical in nature.

The virtual qualification differs from more traditional reliability prediction or estimating techniques because the prediction can be made at the design stage; rater than based on field and test data. The objective of accelerated product qualification is to assess whether a product will meet the application life requirements. Historically, this objective has been achieved by physical tests, sometimes referred to as accelerated stress tests (AST). Unfortunately, the application of AST does not necessarily guarantee field reliability (Caruso and Dasgupta 1998). Of particular concern is the possibility that failures precipitated during the physical test may not occur in the field (Chan and Englert 2001). More important, even if relevant failures can be precipitated, a quantitative technique is needed to extrapolate results from test conditions to life conditions. Thus, validity and usefulness of AST is brought under scrutiny. To address this problem, the virtual life assessment is used as an accelerated product qualification method. The fundamental barriers to effective integration of the virtual life assessment into a reliability prediction plan are: the cultural change that requires some reliability analysis to be performed before/during the component placement phase, and the inability of current tools to provide all the needed data.

2. Virtual Qualification

2.1 Life cycle load

The life cycle loading for this assembly consist of combined vibration and temperature environments. In order to determine the life cycle loading, the ground test

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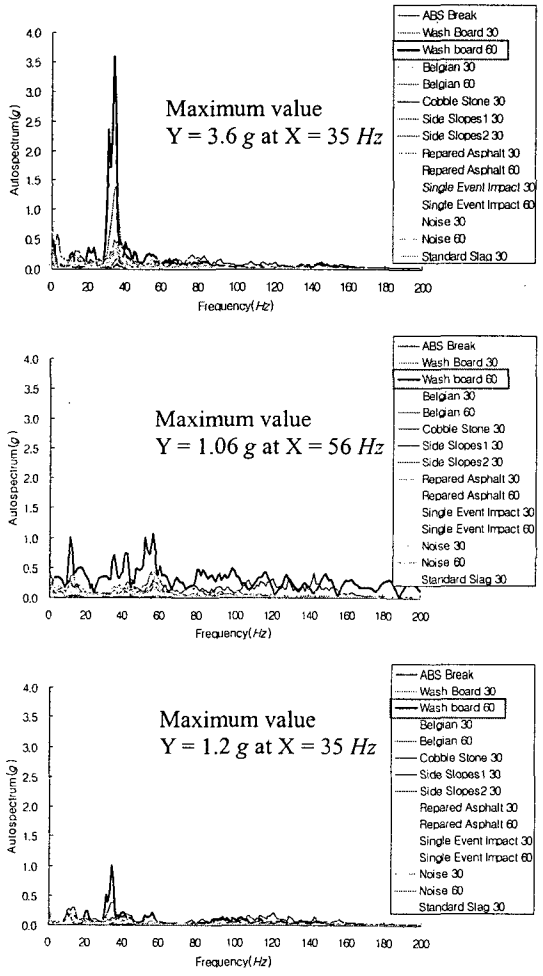
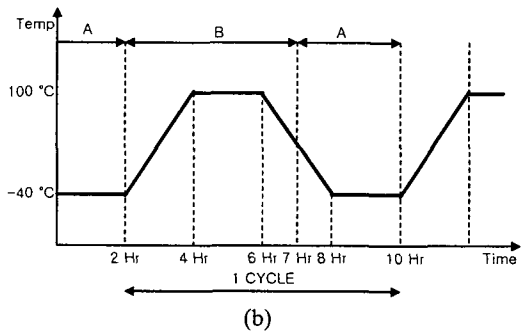
is performed. The tri-axial accelerometer is used to measure the vibration at each axis. Figure 1-(a) show the maximum value of the auto-spectrum obtained from the measurement in each direction of X(front and back), Y(up and down), Z(left and right) axis of the car.

It is apparent that the largest of vibration 3.6*g* amount is at 35 *Hz* in the X axis.



(a)



(b)

Fig. 1 Life cycle loads (a) Vibration (b) Thermal

2.2 Vibration analysis

Vibration analysis is performed to determine the location of maximum curvature for vibration loads in the board. Component located at this location is identified as critical component because the interconnects at this site is expected to be under the maximum stress due to vibration.

The modal testing and FEM modal analysis is performed to obtain the mode shapes and to identify the critical component locations. The component investigated in this study (microprocessor) is present at the location of maximum curvature in the first mode.

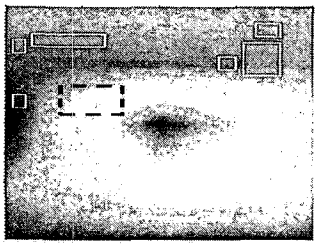


Fig. 2 First mode shape

Figure 3 shows the stress analysis results of the interconnects of microprocessor. The maximum stress occurs on the corner solder joint near the component body. The simulation results indicate that potential failure mechanism is fatigue failure of solder joint at the corner interconnect caused by vibration.

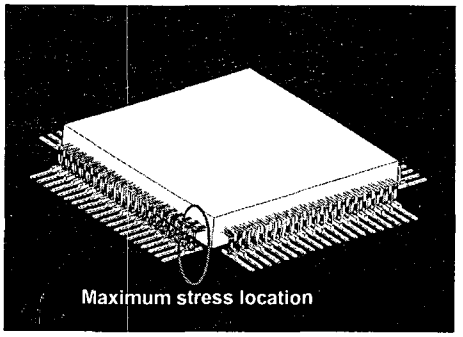


Fig. 3 Stresses of the critical component

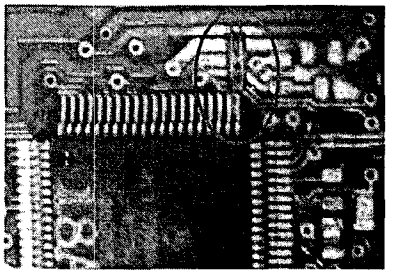


Fig. 4 Location of strain gage

2.3 Damage analysis

Damage analysis is performed on the interconnect identified as critical in the stress analysis to assess the fatigue life of this interconnect.

Thermo-mechanical interconnect stress analysis is performed at the critical location under the applied thermal loads shown in Figure 1-(b). The mean stress history due to the applied thermal cycling is determined. In this analysis the average mean stress is calculated and is used later in conjunction with the observed mechanical strains from vibration loads, to compute the interactive damage.

The deformation histories, collected using strain gage, Figure 5, are converted to range distribution functions (RDF) using cycle counting algorithms.

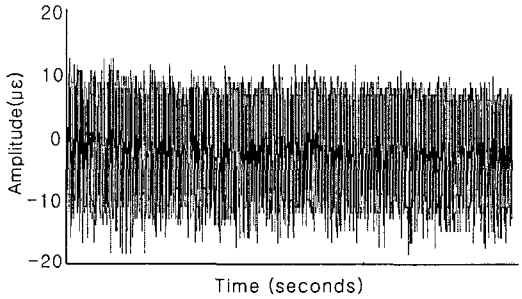


Fig. 5 Deformation history

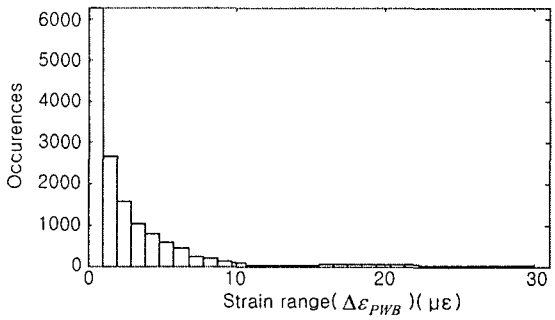


Fig. 6 Strain range distribution

The cycle counting algorithm systematically reduces the complex load history into a number of constant amplitude events and identifies hysteresis loops by range pair matching of local maxima and minima events in the load history. Figure 6 shows the RDF obtained for the deformation history under life-cycle loads.

The strain ranges are then converted to board curvatures with the help of the Equation (1)

$$\kappa_{PWB} = \varepsilon_{PWB} / (0.5 \times t) \qquad (1)$$

Using a local finite element model (Figure 7) of the critical component the strain in the critical solder joint is obtained for a measured board curvature. End rotations are applied in the FEM model to simulate the board curvature due to flexure. The rotation to be applied is calculated based on the Equation (2)

$$\theta = \kappa_{PWB} dx \qquad (2)$$

κ_{PWB} = *board curvature*

ε_{PWB} = *PWB strain*

t = *thickness of the board*

dx = *length of the PWB*

θ = *rotation applied at the end of the* model

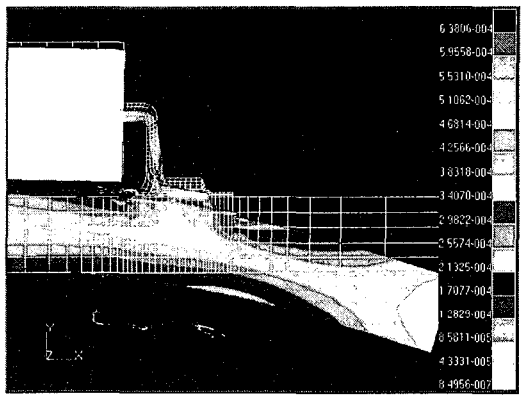


Fig. 7 Detailed model of the critical interconnect

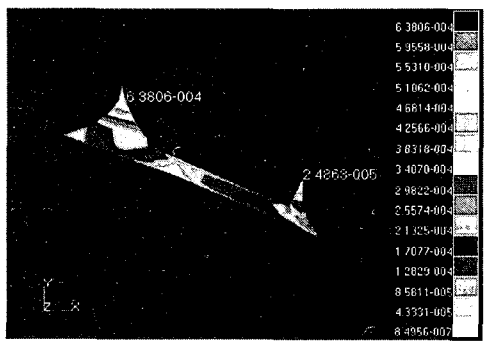


Fig. 8 Solder joint strains

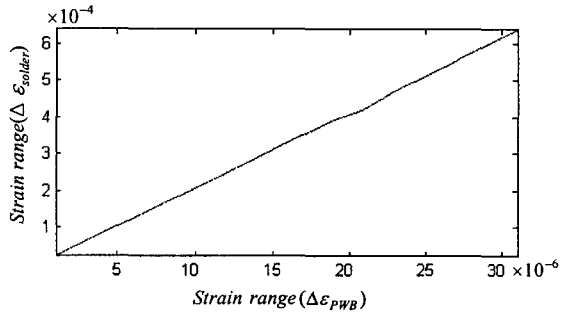


Fig. 9 Strain range of PWB vs. Strain range of solder

Finally RDF of the solder joint strains are then obtained. In the damage analysis, the Coffin-Manson damage model, Equation 3, is then used to calculate damage due to the individual bins.

$$\Delta\varepsilon/2 = ((\sigma_f'-\sigma_0)/E)(2N_f)^b + \varepsilon_f(2N_f)^c \quad (3)$$

$\Delta\epsilon$ = *Equivalent strain amplitude*
σ_f' = *Fatigue strength coefficient*
ϵ_f = *Fatigue ductility coefficient*
N_f = *Number of cycles to failure (life)*
σ_0 = *Mean stress (residual thermo-mechanical stress)*
E = *Modulus of elasticity*
b = *fatigue strength exponent*
c = *fatigue ductility exponent*

Miner's rule for damage superposition (Miner, 1945) is used to obtain the incremental damage due to all the bins.

$$(\Delta D_v)_j = (\sum_i (\frac{n_i}{N_i})_{T_j})\Delta t_j$$
$$\frac{1}{N_v} = \sum(\Delta D_v)_j \quad (4)$$

n_i = *number of occurrences from strain RDF*
T_j = *discretized temperature levels*
t_j = *fraction of total time spent at the discretized temperature level*
N_i = *Life predictions from generalized Coffin-Manson model for each increment*
$(D_v)_j$ = *accumulated vibrational damage in each increment* Δt_j
N_v = *accumulated solder joint fatigue life under vibrational loading*

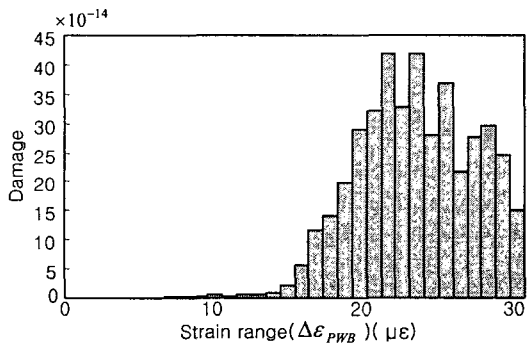


Fig. 10 Vibrational Damage in the solder joint

3. Conclusions

The methodology presented in this paper, fatigue life of automotive electronic packaging assemblies can be virtually tested through computer simulation.

Although described in terms of microprocessors, the proposed methodology is applicable to other design configurations and components. In the analysis of the microprocessor, potential failure mechanism under vibration is briefly mentioned.

The incremental damage superposition approach is applied for virtual qualification under combined thermal and vibration environment.

The ability to predict product reliability early in the conceptual design phase is one of the key factors in achieving design robustness within a shorter cycle time. Continuous proactive efforts are underway to enhance this ability. These efforts include comprehensive board level correlation test, material characterization, and component durability studies.

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