An embedded vision system based on an analog VLSI Optical Flow vision sensor

Vlatko Bečanović*, Takayuki Matsuo*, Alan A. Stocker**
*Dept. of Brain Science Engineering, Kyushu Institute of Technology,
vlatko@brain.kyutech.ac.jp,
matsuo-takayuki@edu.brain.kyutech.ac.jp
**Howard Hughes Medical Institute and Center for Neural Science, New York University,
alan@cns.nyu.edu

Abstract - We propose a novel programmable miniature vision module based on a custom designed analog VLSI (aVLSI) chip. The vision module consists of the optical flow vision sensor embedded with commercial off-the-shelves digital hardware; in our case is the Intel XScale PXA270 processor enforced with a programmable gate array device. The aVLSI sensor provides gray-scale imager data as well as smooth optical flow estimates, thus each pixel gives a triplet of information that can be continuously read out as three independent images. The particular computational architecture of the custom designed sensor, which is fully parallel and also analog, allows for efficient real-time estimations of the smooth optical flow. The Intel XScale PXA270 controls the sensor read-out and furthermore allows, together with the programmable gate array, for additional higher level processing of the intensity image and optical flow data. It also provides the necessary standard interface such that the module can be easily programmed and integrated into different vision systems, or even form a complete stand-alone vision system itself. The low power consumption, small size and flexible interface of the proposed vision module suggests that it could be particularly well suited as a vision system in an autonomous robotics platform and especially well suited for educational projects in the robotic sciences.

Keywords: optical flow, analog VLSI (aVLSI) sensor, embedded vision system, XScale architecture, robotics.

1 Introduction

Vision is crucial for many real-world applications. Yet, vision is expensive. The high bandwidth and the variable and ambiguous visual environment typically require large computational power - even to solve relatively simple low-level visual processing tasks. Particularly, this becomes a problem for smaller robots where size- and power-restrictions severely limit the available computational resources for visual processing. Some low-cost vision modules based on the traditional camera/microprocessor approach have been proposed (see [4], *e.g.*), yet because of above reasons, processing is either slow or limited to computationally not highly demanding tasks such as color segmentation and tracking by color. Performing higher level vision task such as real-time optical flow estimation becomes much more difficult for such traditional approaches because it requires a high amount of computational resources.

Here, we propose a novel approach in building a miniature vision module that is small and consumes little power, yet is powerful enough to solve computationally demanding vision tasks such as e.g. optical flow estimation. The module embeds a computationally efficient analog VLSI (aVLSI) vision sensor within a programmable digital hardware environment. The vision sensor provides efficient and rigorous real-time estimation of 2D optical flow (cf. [1], [2]). Furthermore, it provides the logarithmically encoded and temporally adapted image brightness, thus guarantees high contrast sensitivity over many orders of light illumination. Its computational efficiency originates from its distributed and analog network architecture, where all computations necessary for optical flow estimation are done in parallel and in continuous-time at each pixel. Because the optical flow estimation is performed by the sensor, almost the entire computational capacity of the digital hardware can be used for user-defined higher level post-processing of the sensory brightness and optical flow data. Furthermore, data from multiple such vision sensors or other external queues e.g. inertial, visual, various encoders, etc. can be integrated. The proposed vision module combines the advantages of analog focal-plane processing with digital programmability and standard protocols.

We have outlined a preliminary version of this system in [3]. The here presented work describes an improved system, which also uses a new micro-processor. Its digital processing capabilities are significantly increased by at least an order of magnitude. Also more flexible interfaces can now be integrated, e.g. wireless LAN, touch-screen,

that will give a distinctive advantage in our aims of designing a powerful and user-friendly system.

2 System Architecture

2.1 The aVLSI vision sensor

The applied analog VLSI chip is a prototype of a sensor architecture that can estimate 2D smooth optical flow [1,2] (cf. Fig. 1). The architecture implements an improved version of gradient-based optical flow algorithm of Horn and Schunck [14]. The algorithm reflects a typical optimization problem encountered in higher level vision. The architecture of the chip is such that it maps the optimization problem to a network structure of only nearest connected processing units. Each unit in the network is identical and constitutes a single pixel. Each pixel contains a logarithmic adaptive photoreceptor [6] and the necessary analog circuitry to compute the local optical flow estimate. However, because of nearest neighbor network connections the computation is distributed and the optical flow estimate is the result of a collective computational effort of solving the optimization problem amongst an adjustable neighborhood kernel of pixels. Adjusting the kernel size leads to optical flow estimates of different degrees of smoothness. For total smoothness and a single moving object, the sensor can solve the aperture problem.

Although all processing on the chip is time-continuous, the read-out is sequential using on-chip scanning circuitry. Scanning is controlled by an external clock provided by the cPLD. At each clock cycle three signals from a single pixel are read out:

- the logarithmically compressed and temporally adapted intensity image $I(x, y)$
- optical flow vector $\underline{v} = (u, v)$ (two components).

Read-out rates up to ~2000 frames/s are possible. The applied prototype aVLSI chip estimates optical flow on a 30x30 array using photoreceptor signals from 32x32 pixels [2]. In Figs. 2 and 3 a snap-shot of the sensor's output (intensity image and optical flow field) can be seen while observing a single moving object. It is important to note, that due to its distributed computational architecture, the chip architecture scales, thus there is no trade-off between chip resolution and processing speed. A larger array size is mainly a question of silicon real-estate, thus fabrication costs.

The chip requires a few bias voltages that ensure its correct operation. Some of them also permits changes to the computational behavior of the chip. For example, the spatial smoothness of the optical flow estimate is continuously controlled by one of the bias voltages. Using external D/A converters that are programmed by the PXA270 the computational domain of the chip can be adjusted on the fly. Also auto-calibration of the aVLSI vision sensor can be handled; several different bias settings can be stored in the common memory of the embedded system and appropriately applied under various visual and environmental conditions.

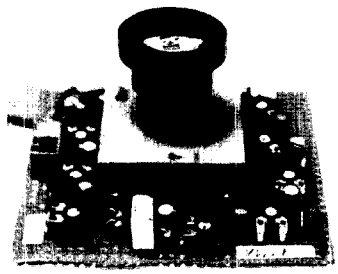

Figure 1. The aVLSI optical flow sensor mounted on a prototype lab-board together with a supporting circuitry and a wide angle lens.

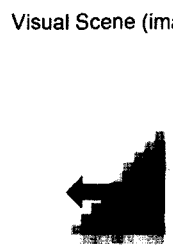

Figure 2. The aVLSI optical flow sensor output for a moving object of triangular shape. Note that the red arrow does not belong to the output of the chip, but is added in order to show the direction of object motion.

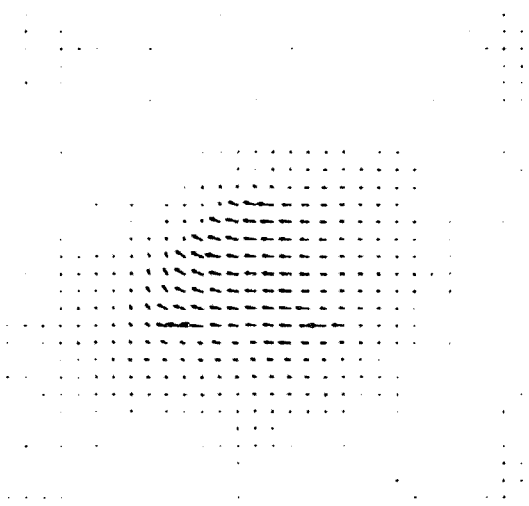

Figure 3. The vector field outputs are the momentary 2D flow field from the example of a leftward moving triangle (cf. Fig. 2).

The scanning circuitry allows read-out rates up to ~2000 Hz, but is set in our system to be < 500 Hz. The chip requires a few bias voltages that ensure the correct operation. They also allow changing the computational behavior of the chip. For example, the spatial smoothness of the optical flow estimate is continuously controlled by one of the bias voltages. Using external D/A converters that are programmed by the PXA270 the computational domain of the chip can be adjusted on the fly. Also auto-calibration of the aVLSI vision sensor can be handled; several different bias settings can be stored in the common memory of the embedded system and appropriately applied under various visual and environmental conditions.

2.2 The Intel XScale PXA270

The Intel XScale PXA270 is specially designed to be used for low power embedded applications and is well suited for relatively computer intense calculations. It is widely used in PDAs, mobile phones etc. The advantages of the PXA270 are its compatibility with a wide range of interfaces common to standard personal computers. It also has some special features like support for touch screen, hardware accelerated graphics instructions through MMX technology and also an integrated instruction set for the control of the Wireless LAN protocol. The main clock on the processor is 104 MHz and the CPU core is 520 MHz. The module that we use in our work is equipped with 64 MB flash-ROM and 64 MB SDRAM (all controlled by the processor). This memory is mainly to be used for the buffering of the streamed sensory data and for storing various tables for the calibration procedure of the optical flow sensor. The PXA270 is furthermore equipped with the special JTAG protocol which makes the debugging of the system very flexible.

2.3 The cPLD gate array as serializer

Programmable logic devices are used in a wide range of applications. In our system we will use the Lattice™ M4A5-256/128 "complex" programmable logic device (cPLD) as the read-out unit for the optical flow chip. The cPLD circuit is programmed to read the sampled data from three ADCs in parallel and then send this data serially to the SPI bus of the PXA270. The cPLD circuit is driven by a clock signal generated by an external oscillator. The aVLSI sensor data is read out sequentially by three 10 bit A/D converters (ADCs) which in turn are watched by the cPLD gate array circuit that is programmed to receive the 3x10 bits in parallel together with a control bit for each ADC. The cPLD will then further serialize the parallel data stream upon receiving a flag from the control bits notifying that data can be read out from the output buffers of the ADCs. The cPLD gate array will serve as the master of the serial communication and in this role initiate the serial transfer to the PXA270 through its SPI serial protocol. This will generate interrupts that are handled by the PXA270 in a way that a frame buffer is filled (double buffering). Each channel is stored separately in corresponding parallel buffers (cf. [3]).

2.4 Overall system architecture

The architecture of the complete module is illustrated in Fig. 4 where it can be seen how the analogue optical flow sensor is interfaced through D/A and A/D converters that read out and also control the operation of the sensor. The cPLD will then further do some simpler processing before it serializes the data and passes it on to the PXA270 for higher level processing.

The PXA270 will interface through standard computer interfaces that require a cable line, but also be able to use wireless LAN communication and to connect to a smaller touch screen.

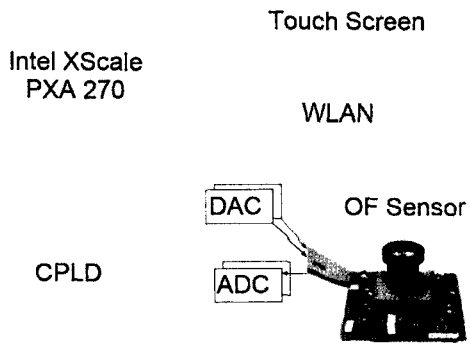

Figure 4. The system architecture with the corresponding data streams indicated.

3 Discussion

The vision module presented in this paper is a novel hybrid system that combines the strength of both, the analog VLSI and the digital microprocessor world. The computational efficiency of the aVLSI vision sensor is improved with the flexibility of a freely programmable microprocessor. A presumptive user of this system can calibrate and program the system from a host PC by using a cross-compiling development environment such as the MS Platform Builder™, Redhat GNUPro™, and others. The former will run Windows CE 5.0 on the PXA270 and the latter is a Linux based solution.

Since aVLSI chips compute in a parallel manner they are computationally very efficient, but they are still not flexible in the way that you can re-program them such as digital systems. Previous approaches have used fully analog motion systems to perform higher-level motion processes based on optical flow [8]. Our system is far more flexible and user-friendly compared to such pure aVLSI approaches. On the other hand, also purely digital hardware solutions have been propose based on optical

flow estimation, but those are either far more expensive than our hybrid system with comparable performance [9], or show a lower performance compared with our solution [10].

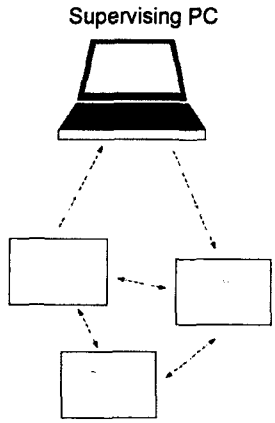

Figure 5. Several vision system modules that operate together with a supervising PC.

The vision system presented in this paper consists of hardware components that are programmable which makes this approach flexible and leaves room for further rapid development.

The final system will also be manufactured in a modular way where parts are connected with adapters and can be stacked on top of each other. In our case there will be two boards of equal physical size where the primary board will host the read-out logic for the vision sensor, and the secondary is reserved for the post-processing task.

4 Conclusions

We proposed a novel miniature vision system, which is based on an aVLSI vision sensor that calculates optical flow. The system combines the flexibility of a freely programmable vision system with the efficient computational power of a custom aVLSI sensor. The vision module, once fully developed, seems particularly well suited for smaller robots such as *e.g. Koala* and *Khepera* [11], which are widely used for educational purposes. Students can easily program their own vision processing algorithms together with some simpler robot behavior. This kind of system architecture might also be well suited for "swarm" robotics [12], or any other robot system that requires a compact and efficient vision system that can be interfaced with complementary processing modules and external sensors.

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