Implementation of Platform System for IEEE 802.15.4 Low Rate WPAN

JooHo Park, YoungJin Kang, JaeYoung Kim

Electronics and Telecommunication Research Institute(ETRI),
161, GajeongDong, Yuseong-gu, Daejeon, 305-700, Korea
joohp@etri.re.kr, kyj64086@etri.re.kr, jyk@etri.re.kr

Abstract *– In this paper the platform system for IEEE 802.15.4 Low Rate WPAN is designed and fabricated. IEEE 802.15.4 Low Rate WPAN system serves the functions and realization of home-area network. According to the IEEE 802.15.4 standard, there are two modes, One is BPSK modulation in 868/915MHz frequency band. The other is O-QPSK modulation in 2.45GHz frequency band. In this paper we implemented the platform system mounted in one PCB board in 868/915MHz frequency band of IEEE 802.15.4 Low Rate WPAN system. We measured that the platform system which consists of digital part and RF part has good performance. Also RF part is realized by design and fabrication of the RF transceiver IC. The key issue is to make the platform system which provides the function of Low Rate WPAN system to meet the requirement of IEEE 802.15.4 standards.*

Keywords: Low Rate WPAN, BPSK, Platform system, Transceiver

1 Introduction

The number of the devices and applications will increase as more devices are controlled or monitored from a distance in my house. We'll need to put them under a control interface that can interconnect into a home-area network. The WPAN (Wireless Personal Area Network) technologies are regarded as the promising in the home network, building automation, and industrial applications. IEEE 802.15.4 Low Rate WPAN system serves the functions and realization of home-area network. According to the IEEE 802.15.4 standard[1], there are two modes, One is BPSK modulation in 868/915MHz frequency band. The other is OQPSK modulation in 2.45GHz frequency band. These modes use a single carrier. The system used single carrier is stronger than the system used multi-carrier about the effect of carrier frequency offset. In specification, the transmitted center frequency tolerance shall be ± 40 ppm maximum. These parameter effect the performance of system.

In this paper we implement the platform system in 868/915MHz frequency band of IEEE 802.15.4 Low Rate WPAN system. The key issue is to make the platform system which provides the function of Low Rate WPAN system to meet the requirement of IEEE 802.15.4 standard. Basically the platform of Low Rate WPAN system consists of MAC, Modem, RF part. In this system, 8051 microcontroller and FPGA are used for the control and implementing the digital logic and RF part is implemented using the RF transceiver IC that we designed and fabricated. RF transceiver IC has the architecture of the direct conversion transmitter and receiver. The system performance is measured by the predefined Packet Error Rate. And the network is implemented using the star topology and tested the transmission of simple character data between systems.

In this design and implementation, we bring to a focus on prototyping the Low Rate WPAN system.

2 Overview

IEEE 802.15.4 Low Rate WPAN system serves the functions and realization of home-area network. According to the IEEE 802.15.4 standard, there are two modes, One is BPSK modulation in 868/915MHz frequency band. The other is OQPSK modulation in 2.45GHz frequency band. Table 1 shows the frequency bands and data rates of IEEE 802.15.4 Low Rate WPAN system standards.

Table 1. Frequency bands and data rates

PHY (MHz)	Frequency band (MHz)	Spreading parameters		Data parameters		
		Chip rate (kchip/s)	Modulation	Bit rate (kb/s)	Symbol rate (ksymbol/s)	Symbols
868/915	868–868.6	300	BPSK	20	20	Binary
	902–928	600	BPSK	40	40	Binary
2450	2400–2483.5	2000	O-QPSK	250	62.5	16-ary Orthogonal

In this paper we implement the platform system in 868/915MHz frequency band of IEEE 802.15.4 Low Rate WPAN system. The Modem of 868/915MHz frequency band is used the method of BPSK(Bi-Phase Shift Keying) for data modulation and the data rate of modem is 20kbps when operating in the 868MHz band and 40kbps when operating in the 915MHz. The modulated signal from modem goes through the RF part. In the RF part there are low pass filter, amplifier, RF mixer and so on. Finally transmitting RF signal using antenna. The received RF signal goes through the RF part and transmits the digital signal to the modem that makes the role of synchronization and demodulation[2].

The Low Rate WPAN platform system is designed and implemented for realizing the overall system control and MAC layer software using 8051 microcontroller and including the modem and RF part. Table 2 shows the specification of the RF block.

Table 2. The specification of RF block

	Parameter	Requirements	Design spec.	Unit
Tx	Pout	> -3	0	dBm
	Range	-	-21 ~ +3	dBm
	OIP3	10	Pout +12	dBm
	LPF order	-	2nd order	Butter-worth
Rx	NF	~ 20	9	dB
	IIP3	~ -39	-20	dBm
	IIP2	~ +12	+20	dBm
	Gain	20 ~ 90	10 ~ 100	dB
	LPF BW	-	fchip	Hz
	LPF order	-	3rd order	Butter-worth

3 Design and Implmentation

The Low Rate WPAN system is realized in single chip for miniaturization, light weight, and low consumption and so on. We have the goal that we design and fabricate the single chip of the Low Rate WPAN system kinds of SoC(System on Chip) . So, The Low Rate WPAN platform system serves the base of designing single chip that included the modem and RF part.

The Low Rate WPAN platform system consists of digital part, RF part in hardware. The digital part consists of the FPGA for realizing and verifying the modem algorithm, the MCU(microcontroller unit) for control signal and programming MAC layer. The RF part is realized one RF transceiver IC which designed and fabricated. Figure 1 shows the overall block diagram of Low Rate WPAN platform system.

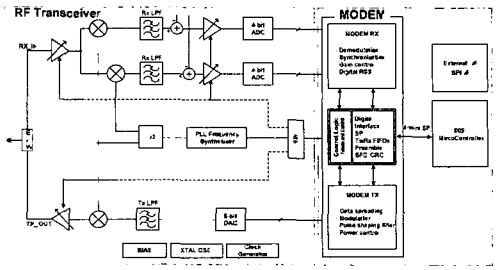

Figure 1. Block diagram of Low Rate WPAN platform system

- Digital part

The digital part consists of the FPGA for realizing and verifying the modem algorithm, the MCU for control signal and programming MAC layer in hardware. Figure 2 shows the detailed block diagram of modem block.

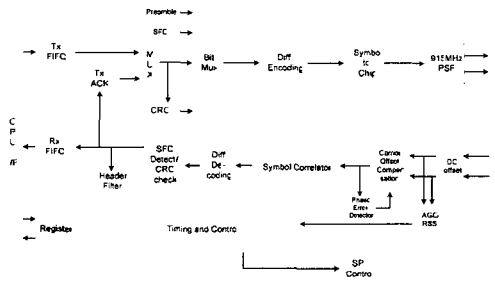

Figure 2. Block diagram of modem block

In modem block there are MCU Interface block for interfacing with MCU, data MUX block, differential encoding block, data spreading block, symbol synchronization block, differential decoding block, and Tx/Rx FIFO. Also there are the SPI block for control RF part, timing and clock generation block, and definition registers.

The Tx modem block executes the functions of transmitting the beacon, data, command, ACK packet to RF part. The transmitting packet data is saved in the Tx FIFO as from length to the last octet of the payload. The Tx ACK buffer is the buffer for using when transmitting the ACK signal of Rx packets and the ACK packet data is saved in Tx ACK buffer.

Differential encoding is the modulo-2 addition(exclusive or) of a raw data bit with the previous encoded bit. This is performed by the transmitter and can be described as following.

$$E_n = R_n \oplus E_{n-1}$$

Each input bit shall be mapped into a 15-chip PN(Pseudo-random Noise) sequence as specified in Table 3.

Table 3. Symbol-to-chip mapping

Bit	Chips (C0, C1, ... C14)
0	1 1 1 1 0 1 0 1 1 0 0 1 0 0 0
1	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1

The pulse shaping filer oversamples the input chip and performs the raised cosine filtering. Figure 3 shows the characteristic of impulse response of the raised cosine filter and the equation is followed.(roll-off factor = 1)

$$p(t) = \frac{\sin(\pi t / T_C)}{\pi t / T_C} \frac{\cos(\pi t / T_C)}{1-(4t^2 / T_C^2)}$$

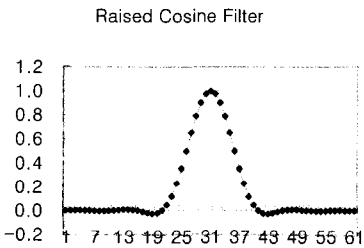

Figure 3. Impulse response of raised cosine filter

The Rx modem block performs the functions of saving in the Rx FIFO the packet signal extracted from Rx_I, Rx_Q signal which received from RF part. The DC offset block for compensating the dc offset of ADC of the Rx I, Q signals.

The RSSI(Received Signal Strength Indicator) block exists for estimation of signal strength and operates x10 chip rates as calculating |Ri*Ri + Rq*Rq|, obtain the average of value for one symbol. The AGC(Automatic Gain Control) block executes the role of control Rx gain according to RSSI signal. For extracting the timing acquisition needs the chip timing recovery block, this block transmits the signal sampled by chip rate with chip timing sync.

The chip carrier recovery block uses the algorithm of Costas-Loop method for carrier offset compensation and transmits the signal compensated carrier phase offset. The symbol block obtains the decided symbol value after correlating between input signals and 15 chip pattern. The length information received next to SFD(Start of Frame Delimiter) is used for controlling other blocks. The received data is saved in Rx FIFO from length and the CRC block operates and checks MAC header data in first. And the part of MAC header goes to the header filtering block, executes the role of receiving the wanted packet signal .The MCU block generates several control signals and programs the MAC layer

- RF part

The CMOS RF transceiver IC is designed and fabricated that satisfies the specification of the PHY layer of IEEE 802.15.4 standards. We derive the system specifications from IEEE 802.15.4 standards and decide the architecture of RF transceiver. Then we decide the specification of sub-block of transceiver and design using CMOS 0.18um technology parameter. The designed schematic is verified according to simulation and complete the layout in accordance with TSMC 0.18um CMOS design rule check, integrate in 2.5mm x 1.65mm size[3][4].

We fabricated the sample IC of the designed transceiver and test the performance of it. The result of transceiver IC satisfies the proposed standards specification.

In the figure 1 can see the architecture of RF transceiver. The architecture of receiver is the DCR(Direct Conversion Receiver) and converts the RF signal into the baseband signal directly. The transmitter is the BPSK modulator. So, we use one signal path without two I, Q paths. The VCO uses the double frequency of the RF frequency and is used divided-by-2 as the LO signal. This has the advantages of that there isn't almost PA-VCO pulling when the PA frequency is the same as the VCO frequency. Because the difference between the PA frequency and VCO frequency exists. In the receiver ADC is used and must maintain the levels of ADC input signal for control the AGC. Therefore the receiver includes the PGA(Programmable Gain Amplifier) which has the wide dynamic range. This can be controlled by 1dB step from digital control word exactly[5].

We implement the digital part and RF part on one PCB board type as shown in figure 4. The RF part is inserted using the daughter board.

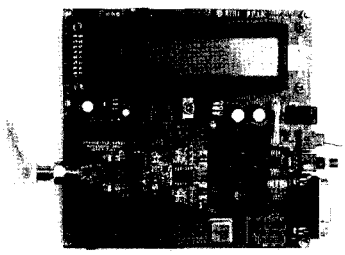

Figure 4. Picture of implemented Low Rate WPAN platform system

4 Test Results

Figure 5, 6, 7, 8 are the test result of Low Rate WPAN platform system. Figure 5 shows the characteristics of modulated output spectrum. As shown Figure 5, this

platform has good spectrum characteristics of satisfying the transmit PSD mask under -20dBc. As shown Figure 6, the characteristics of phase noise is -107dBc/Hz@1MHz offset.

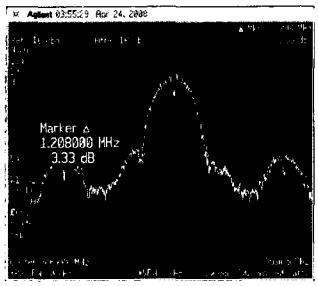

Figure 5. Modulated output spectrum

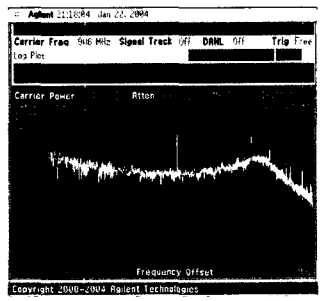

Figure 6. Phase Noise of LO signal

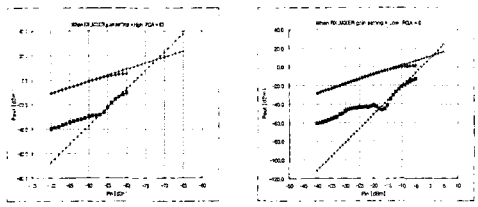
Figure 7. The test result of In-band IIP3

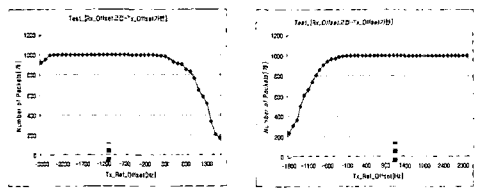
Figure 8. The test result of carrier offset compensation

Figure 7 shows the In-band IIP3 characteristics according to high/low gain setting, Figure 8 shows the characteristics of carrier offset compensation in satisfying PER < 1%

5 Conclusions

The IEEE 802.15.4 Low Rate WPAN platform system that has the functions of data transmitting/receiving is implemented and fabricated. This consists of MCU interface, RF interface and has the compatible feature of IEEE 802.15.4 standards and we measured the characteristics of platform system and satisfied the compensation of carrier offset 80ppm. The designed and fabricated RF transceiver IC is measured according to standards specification. The RF transceiver satisfies the proposed specifications using the simple hardware and integrates 2.5mm x 1.65mm size.

On the basis of implementing the Low Rate WPAN platform system we will merge the modem and RF part, design the single chip of Low Rate WPAN system.

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