Design and Simulation of HomePNA 2.0 MAC Controller Circuit

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Abstract – The Home Phoneline Networking Alliance (HomePNA) 2.0 technology can establish a home network using existing in-home phone lines, which provides a channel rate of 4 – 32 Mbps. HomePNA 2.0 Medium Access Control (MAC) protocol adopts an IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method, a Quality of Service (QoS) algorithm, and a Distributed Fair Priority Queuing (DFPQ) collision resolution algorithm. In this paper, we analyze the HomePNA 2.0 MAC protocol and propose the architecture of HomePNA 2.0 MAC controller circuit. Then, we present the simulation result of each block included in the HomePNA 2.0 MAC controller.

Keywords: HomePNA, MAC, priority level, collision resolution, backoff signal

1 Introduction

Recently the personal computer has become a powerful platform in the home for work, communication, education, and entertainment. And the internet has become an essential means of information access. With the appearance of many new digital appliances, the digital traffic is rising rapidly. Just as there is a critical need for high-speed access network outside the home, there is a growing need for high-speed home network within the home. Businesses accomplish this by deploying Local Area Networks (LANs). However, networks are not commonly deployed in the home due to the cost and complexity of installing the new wiring required by traditional LANs. The HomePNA was formed to develop specifications for interoperable, home-networked devices using already in place phone wiring [1].

The HomePNA standardized the HomePNA 1.0 specification which provides a data rate of 1 Mbps in September 1998, and standardized the HomePNA 2.0 specification which provides a data rate of 4 - 32 Mbps in December 1999.

The HomePNA 2.0 specification operates in the 4.75 - 9.25 MHz band, and uses the Quadrature Amplitude Modulation (QAM) technique and Frequency Diverse QAM (FDQAM) technique. The specification is a technology designed to connect up to 25 stations on each available phone line at cable distances of up to 150 meters. The HomePNA 2.0 MAC protocol adopts an IEEE 802.3 CSMA/CD access method with QoS support, such as eight priority levels for different classes of traffic. And the protocol includes a new collision resolution algorithm called DFPQ [2] [3].

The HomePNA 2.0 Physical Layer (PHY) frame format is shown in Figure 1. The frame consists of a low-rate header section, a variable-rate payload section, and a low-rate trailer. The HomePNA 2.0 specification can adaptively use data rates from 4 to 32 Mbps, according to the channel conditions. This is the rate of transmission used only for the payload. The header and the trailer are always transmitted at 4 Mbps, with a more robust modulation and symbol rate, so that all stations can receive them correctly.

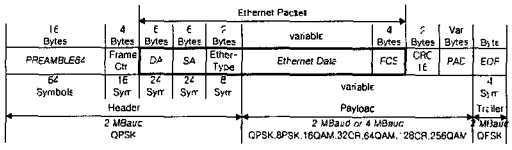

Figure 1. HomePNA 2.0 PHY frame format

The HomePNA 2.0 PHY frame is based on the IEEE 802.3 Ethernet packet. The Ethernet packet is preceded by a Preamble64 of 16 bytes and a Frame Control field of 4 bytes, and followed by a Cyclic Redundancy Check field (CRC16) of 2 bytes, a

variable-length padding and an End of Frame (EOF) sequence of 1 byte. The padding is used when the transmission time of the complete frame is less than 92.5 us to guarantee the minimum valid frame duration, in order that this frame is not misinterpreted as a collision fragment.

In this paper, we analyze the HomePNA 2.0 MAC protocol and propose the architecture of HomePNA 2.0 MAC controller circuit. Then, we present the simulation result of each block included in the HomePNA 2.0 MAC controller.

This paper is organized as follows. In Section 2, we analyze the HomePNA 2.0 MAC protocol. In Section 3, we propose the architecture of HomePNA 2.0 MAC controller circuit and present the simulation result of each block included in the HomePNA 2.0 MAC controller. Section 4 concludes the paper.

2 HomePNA 2.0 MAC protocol

The HomePNA 2.0 MAC protocol uses an IEEE 802.3 CSMA/CD for medium access, and uses a QoS algorithm for multimedia service. The collision resolution algorithm uses a new algorithm called DFPQ that does not exhibit capture effect, which is a problem of Binary Exponential Backoff (BEB) collision resolution algorithm [4].

2.1 CSMA/CD medium access method

The CSMA/CD medium access method is the means by which two or more stations share a common transmission channel. For a frame transmission, a station monitors the Carrier Sense (CS) signal over the channel. If a station detects the CS signal prior to the start of the station's Priority Slot, the station shall defer. If a station doesn't detect the CS signal, the station transmits a Valid CS Frame as shown in Figure 2. If a station detects a collision under transmission, the station ceases transmission no later than 70 microseconds and transmits a Valid Collision Fragment as shown in Figure 3.

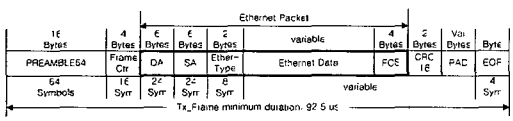

Figure 2. Valid CS Frame

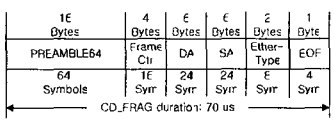

Figure 3. Valid Collision Fragment

Timing of subsequent transmissions following a Valid CS Frame or Valid Collision Fragment is based on a MAC timing reference, established by the receiver. Time following a transmission is divided into slots; an Inter Frame Gap (IFG); three Backoff Signal Slots (following collisions); and 8 Priority Slots as shown in Figure 4. During these time periods, the MAC is synchronized and informs the Frame Controller of exact transmission time while performing the priority access and the collision resolution algorithm. After Priority Slot 0 there may be an unsynchronized period. In this period, any station with traffic at any priority level contends on a first-come, first-served basis. Receivers are only required to correctly detect a Valid CS Frame, Valid Collision Fragments and Backoff Signal.

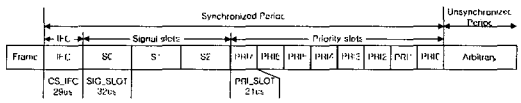

Figure 4. HomePNA 2.0 MAC time slots

2.2 Priority access

The priority access method of HomePNA 2.0 MAC is to delay transmissions to a slot beyond the IFG, based on the priority level of the frame waiting to be transmitted. Slots are numbered in decreasing priority, starting at priority 7. Higher priority transmissions commence transmission in earlier slots and acquire the channel without contending with the lower priority traffic.

2.3 Priority mapping

The link layer of HomePNA 2.0 plays an important role to map the user priority level of traffic to the PHY priority level of HomePNA 2.0. But the method of priority mapping is implementation dependent.

2.4 Collision detection

Two or more stations may begin transmitting in the same Priority Slot following the IFG period. All stations monitor the channel to detect the colliding transmissions of other stations. Active station, that is transmitting, compares a specified part of transmitting frame (from Frame Control field to Ether-Type field) with a specified part of receiving frame. If there is a difference between a specified part of transmitting frame and a specified part of receiving frame, it is confirmed that a collision is occurring, and the station ceases transmission no later than 70 microseconds (Valid Collision Fragment). Passive station, that is not transmitting, monitors the length of CS signal and

generates a Collision Fragment indication to the Collision Resolution function if the duration of carrier is 32 – 92 microseconds.

2.5 Collision resolution

A collision occurs when two or more stations are active with ready frame and are contending for access to the channel at approximately the same time; generally, collisions are between frames at the same priority level. If a collision occurs, a DFPQ algorithm is run, which results in stations becoming ordered into Backoff Levels where only one station is at Backoff Level (BL) 0 and can therefore acquire the channel.

After the winning station completes its transmission, all stations reduce their BL by one if it is greater than zero, and the new station(s) at BL 0 attempt transmission. All stations even those with no frame to transmit, monitor the activity on the medium. The collision resolution cycle is closed, so that stations that did not collide are not allowed to contend for access to the medium until all stations that collided have transmitted on frame successfully. Ultimately all stations that were contending for access in the initial collision gain access to the wire and the collision resolution cycle is ended. This results in access latency being tightly bounded.

Each station maintains eight BL counters, on for each priority. The BL counters are initialized to 0.

After a collision and an IFG, three special Backoff Signal Slots (S0, S1 and S2) are present before the normal sequence of priority contention slots occurs as shown in Figure 4. Signal Slots only occur after collisions, they do not follow successful transmissions. Each active station pseudo-randomly chooses one of the Backoff Signal Slots, and transmits a Backoff Signal. More than one station can transmit a Backoff Signal in the same slot. The active stations transmit Backoff Signals to indicate ordering information that determines the new Backoff Levels to be used.

All stations (even passive stations) monitor collision events and the Backoff Signal Slots to compute the BL. If an active station sees a Backoff Signal in a slot prior to the one it chose, it increases its BL. Those stations at BL 0 that saw no Backoff Signals prior to the one they chose, remain at BL 0 and contend for transmission in the Priority Slot equal to TX_PRI that immediately follows the Backoff Signal sequence. Eventually, only one station remains at BL 0 and successfully gains access to the channel.

All stations, even those not contending for access to the wire, also maintain a Maximum Backoff Level (MBL) counter per priority, which is incremented for each Backoff Signal seen and decremented when a successful transmission occurs.

3 Design of HomePNA 2.0 MAC controller circuit

In order to implement the HomePNA 2.0 MAC protocol, we designed the HomePNA 2.0 MAC controller. Figure 5 shows the block diagram of HomePNA 2.0 MAC controller that we have designed. In Figure 5, the HomePNA 2.0 MAC controller consists of Tx MAC block, Rx MAC block, DFPQ block and Pseudo Random Number Generator (PRNG) block. Tx MAC block transmits a TxDataOn signal that informs the transmitting Frame Controller of exact transmission time and a TxSigType signal that distinguishes whether a transmitting frame of Frame Controller is a Valid CS Frame or Backoff Signal. Rx MAC block receives the CS signal from the demodulator, distinguishes whether a receiving frame is a Valid CS Frame or Valid Collision Fragment or Backoff Signal, and generates suitable MAC time slots. DFPQ block performs a DFPQ collision resolution algorithm. PRNG block, if a collision occurs, generates a pseudo-random number that enables the transmitting Frame Controller to select a BL.

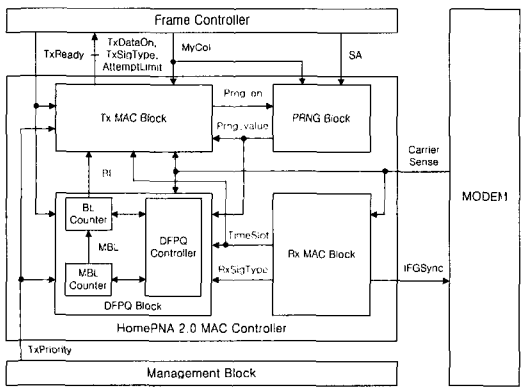

Figure 5. Block diagram of HomePNA 2.0 MAC controller

In order to implement the HomePNA 2.0 MAC controller circuit, we designed each block using the Very highspeed integrated circuit Hardware Description Language (VHDL) code, and synthesized using the Design Compiler of Synopsys. Then we performed simulation in order to evaluate the operation and the performance of each block of HomePNA 2.0 MAC controller, and used the Modelsim of Mentor as a simulator.

Figure 6 shows simulation result of Tx MAC block. As the result of simulation, we confirmed that Tx MAC block exactly transmits to the Frame Controller a TxDataOn signal, a TxSigType signal and

AttemptLimit counter value that indicates the number of attempting Backoff Signal.

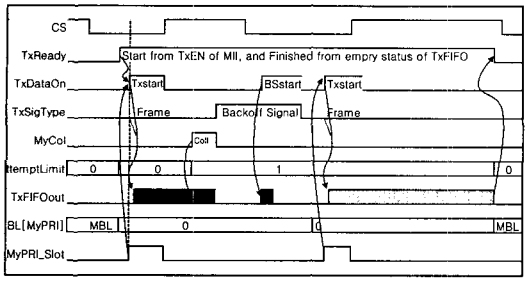

Figure 6. Simulation result of Tx MAC block

Figure 7 shows simulation result of Rx MAC block. As the result of simulation, we confirmed that Rx MAC block generates exact MAC time slots.

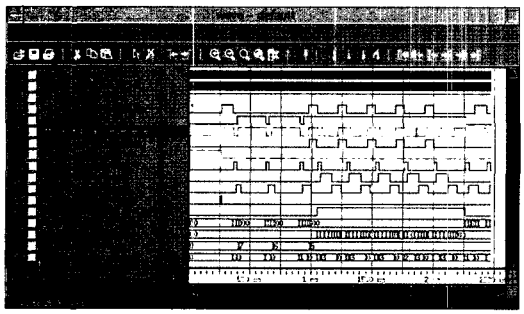

Figure 7. Simulation result of Rx MAC block

Figure 8 shows simulation result of DFPQ block at priority level 7. As the result of simulation, we confirmed that DFPQ block performs an exact DFPQ collision resolution algorithm.

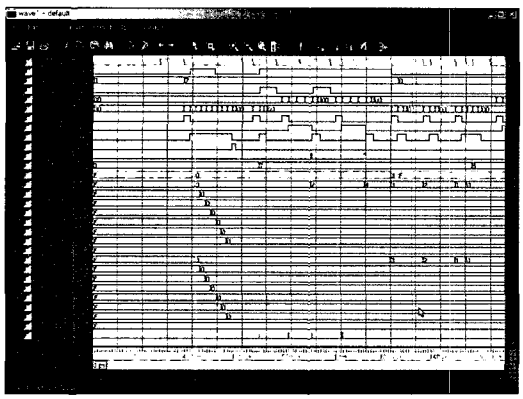

Figure 8. Simulation result of DFPQ block at priority level 7

Figure 9 shows simulation result of PRNG block. As the result of simulation, we confirmed that PRNG block exactly generates a pseudo-random number after a collision.

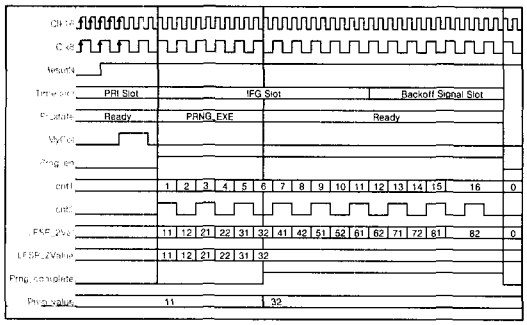

Figure 9. Simulation result of PRNG block

4 Conclusion

In this paper, we analyzed the HomePNA 2.0 MAC protocol and proposed the architecture of HomePNA 2.0 MAC controller circuit that we had designed in order to implement the HomePNA 2.0 MAC protocol, and we presented the simulation results of HomePNA 2.0 MAC controller.

HomePNA 2.0 MAC controller consists of Tx MAC block, Rx MAC block, DFPQ block and PRNG block. Also we presented the simulation result of each block included in the HomePNA 2.0 MAC controller. We confirmed that each block operates exactly and shows the high performance.

The circuit of HomePNA 2.0 MAC controller in this paper can be applied to the fabrication of HomePNA 2.0 MAC chip. It shall be required to pursue further study on the design and fabrication of HomePNA 2.0 transceiver chip that implements HomePNA 2.0 MAC functions and HomePNA 2.0 PHY functions.

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