The gate delay time and the design of VCO using variable MOS capacitance

Ji-Hwan Ryeo

School of Electronic Engineering, Daegu University
e-mail: Jhryeo@daegu.ac.kr

Abstract

In the paper, a proposed VCO based on bondwire inductances and nMOS varactors was implemented in a standard 0.25 μm CMOS process. Using the new drain current model and a propagation delay time model equations, the operation speed of CMOS gate will predict the dependence on the load capacitance and the depth of oxide, threshold voltage, the supply voltage, the channel length. This paper describes the result of simulation which calculated a gate propagation delay time by using new drain current model and a propagation delay time model. At the result , When the reverse bias voltage on the substrate changes from 0 voltage to 3 voltage , the propagation delay time is appeared the delay from 0.8 nsec to 1 nsec. When the reverse voltage is biased on the substrate, for reducing the speed delay time ,a supply voltage has to reduce. The g_m value of MOSFET is calculated by using new drain current model.

1. Introduction

Design of analog or hybrid circuits for lower power dissipation and high speed operation applications poses a very challenging task, especially in the area of video processing , dynamic image processing , and multimedia computing. The area required for the implementation of a certain function can often be reduced by exploiting the full functional capacity differed by the MOS transistor. As CMOS technology approaches the deep submicrometer regime, many effects appear.

According to a rapid development of semiconductor industry, a high performance in VLSI realized and ASIC technology is highlighted. The MOS transistor is scale down little by little. Because the MOS is scale down, many effects is appeared. At the narrow device, the drain depletion layer is increased and interacted between the source and the channel. Accordingly, the below problem is appeared. The potential is lowering effect (drain-induced barrrier lowering), subthreshold current effect, velocity saturation effect, short channel effect, vertical channel electric field increasing effect, the source-drain series resistance of LDD structure etc. The leakage in the drain is a big problem for scaling the MOS FET toward the deep submicrometer regime. To prevent power dissipation causing the subthreshold current, the controling threshold voltage circuit[1]-[3] is developed by biasing back-gate reverse bias or substrate reverse bias. The back-gate reverse bias or substrate bias has been widely utilized with the following advantages- created: suppressing subtheshold leakage, lowering parasitic junction capacitances, increasing immunity against latch-up or parasitic bipolar, etc. This method is used the CMOS IC and DRAM but the disadvantage is appeared due to bias back gate bias or substrate back bias. The disadvantage is speed delay and noise increasing etc.

2. The new current model of the drain saturation current for predicting delay time and simulation

Among all MOSFET parameters, saturation drain current I_{dsat} has the strongest impact on circuit speed, therefore it is one of the most important device parameters. the following poor approximation for I_{dsat} has been used by people in many circumstances to analyze or even to predict the effect of T_{ox}, L_{eff}, and V_{dd} because no analytical I_{dsat} model for deep sub-micron MOSFETs was available:

$$I_{dsat} = \frac{1}{2}\left(\frac{W_{eff}}{L_{eff}}\right)\mu_{eff}\left(\frac{\varepsilon_{ox}}{T_{ox}}\right)\left(V_{gs}-V_{th}\right)^2$$

W_{eff} : effective channel width
ε_{ox} : permittivity of oxide
L_{eff} : effective length
μ_{eff} : effective mobility
T_{ox} : depth of oxide

The MOS variable capacitancecircuit of CMOS on the substrate is shown in Fig 1. and the diagram of capacitance in the CMOS inverter (P- type substrate) is shown in Fig2.

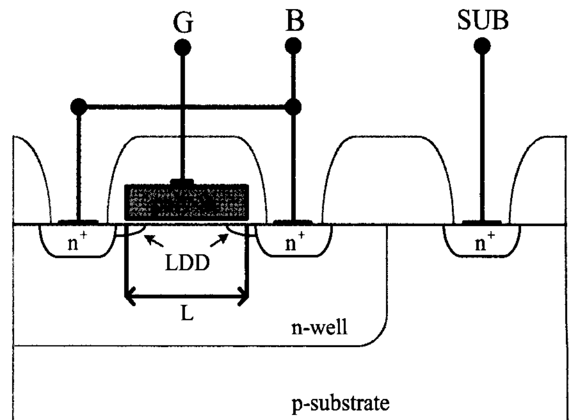

Fig1. The MOS variable capacitance

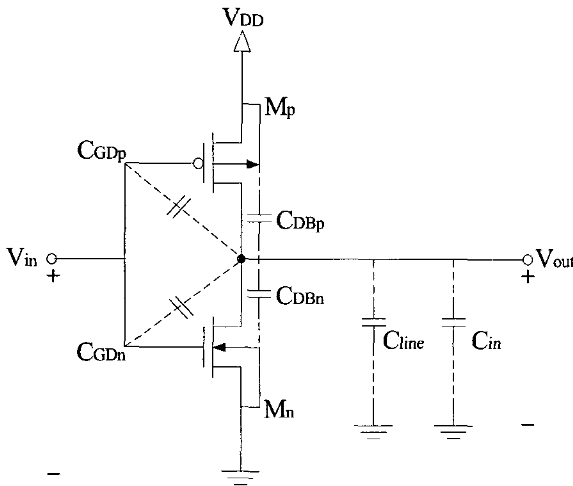

Fig. 2. The The diagram of capacitance in CMOS inverter

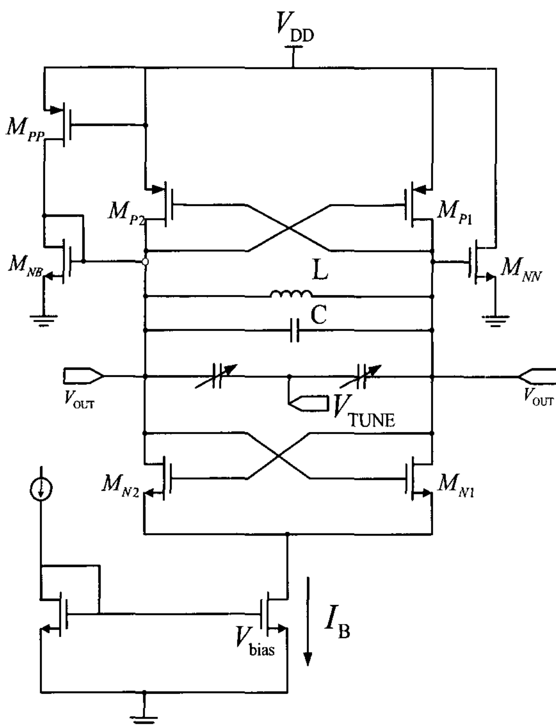

Fig. 3. Proposed voltage-controlled oscillator[7]

3. The propagation delay time model and simulation of CMOS inverter

To predict the operation of futuer MOS device and IC , the present empirical SPICE model is not accurate. An accurate I_{dsat} model for MOSFET has been developed. the mobility degradation is considered by the model. The obtain a handy equation similar to (1) for quick evaluation of device and supply voltage scaling on I_{dsat}, numerous simulation for different conditions using the new accurate I_{dsat} model has been carried out. It was found that the following empirical equation is a good approximation for I_{dsat} projection for deep sub-micron MOSFETs:

$$I_{dsat} = k(R_s)L_{eff}^{-0.5}T_{ox}^{0.8}\left(V_{gs} - V_{th}\right)^{1.25}$$

The saturation drain current model of sub-micron MOS transistor is shown to (2)[4] and the model of gate delay time is the following equation (3) [4].

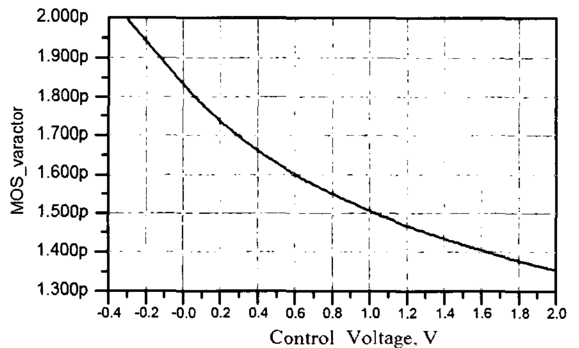

Fig. 4. The MOS capacitance and controlled voltage

$$t_{pd} = \frac{C_L V_{dd}}{n}\left(\frac{1}{I_{dsatn}} + \frac{1}{I_{dsatp}}\right)$$

C_L : A load capacitance of the gate

n : 3.7 A constant which can be determined by SPICE simulation

I_{dsatn} : NMOS saturation drain current

I_{dsatp} : PMOS saturation drain current

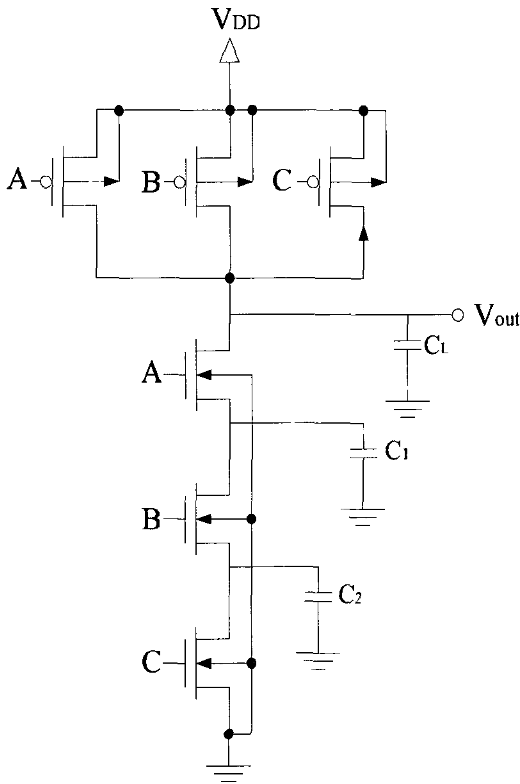

Fig. 5. The effect of substrate reverse bias on the CMOS logic circuit.

The MOS capacitance with controlled voltage is shown in Fig4. when reverse bias is applied on the substrate. The Accurate gate delay time model is necessary to predict the CMOS IC operation speed. This paper is presented to simulation for the gate delay time using (2), (3) equation on the CMOS inverter biasing back gate reverse bias. The Fig 5 is shown the propagation delay time model with load capacitance C_L. The Fig 6 is shown the simulated delay time by using new current model (2) equation. on the biasing back gate reverse bias on the substrate. When the no reverse bias on the substrate, The delay time is 8.0*10 sec and the delay time is 1.01 nsec when the reverse bias voltage is 3 V. Here , the supply voltage is 3.3 voltage and the threshold voltage is 0.5V .

The value of the out of parenthesis on (2) equation is the $5.916*10^{-4}$ $A/V^{1.25}$ and the parameter by using the simulation is shown the Table 1 and Table 2 is the increased threshold voltage and drain current calculated by using new current model on biasing reverse bias on the substrate. To show in the simulated result , in spite of advantage of reverse bias on the substrate , the signal delay time effect is appeared. To cancel delay time resulting from biasing reverse back gate bias on the substrate, the power supply voltage must be reduced. Owing to use P type substrate, to simulate the delay time ,the reverse bias voltage influenced largely the threshold voltage of NMOSFET. the Table 2 is the increased threshold voltage and drain current which calculated by using new current model when substrate is applied on reverse back gate bias.

CL(ff)	Jn/Jp	Vdd	Nsub	d	Vth	L
600	2	3.3	5×10^{17}	60Å	0.5V	0.3 ㎛

Table 1. The parameters to be used at simulation

VB \ ΔVT Id	ΔVT	Idsat	tpd(sec)
1V	0.71	1.5 ㎃	8.6×10^{-10}
2.5V	1.12	1.1 ㎃	9.7×10^{-10}
3.0V	1.23	1.0 ㎃	10.1×10^{-10}

Table 2. The increased threshold voltage and calculated drain current which applied the reverse bias on substrate

4. Voltage Gain of The MOSFET

In strong inversion, it shows in the expression of drain current equation (4) conventionally.

$$I_{dsat} = \frac{W\mu C_{ox}}{2L}(V_{gs} - V_{th})^2$$

The value of transconductance to drain current ratio, gm/Id , can be obtained from the following relationship.

$$\frac{g_m}{I_d} = \frac{dI_d}{I_d dV_g}$$

The maximum voltage gain of a MOSFET is obtained when the value of gm/Id is largest.

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta I_d}{g_d}\frac{1}{\Delta V_{in}} = \frac{\Delta V_{in} g_m}{g_d}\frac{1}{\Delta V_{in}} = \frac{g_m}{g_d}$$

g_m : transconductance

g_d : drain conductance

The Fig. 6 is the calculated g_m value by using new saturation drain current equation (2).

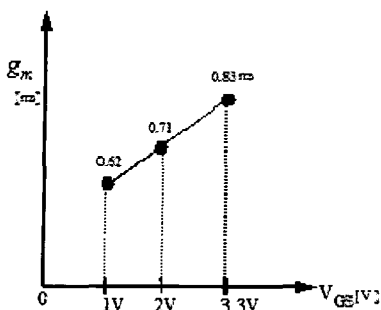

Fig.6 The value of calculated g_m by using new drain current model

5. The design of VCO circuit and the result of simulation

Proposed VCO uses a CMOS differential oscillator type and it fabricated in a 0.25 um standard CMOS processes. In order to watch mobility of the pMOS and the nMOS (mobility) the size of the nMOS transistor and the pMOS transistor decided at the degree where the amplitude of VCO output will be saturated at 1:3 ratio, the size of nMOS transistor W decided with 20 um. Fig3 is shown VCO circuit and Fig7 is shown the characteristic VCO.

In this paper, the ADS(advanced Design system) which is RF circuit design simulator is used and tested a

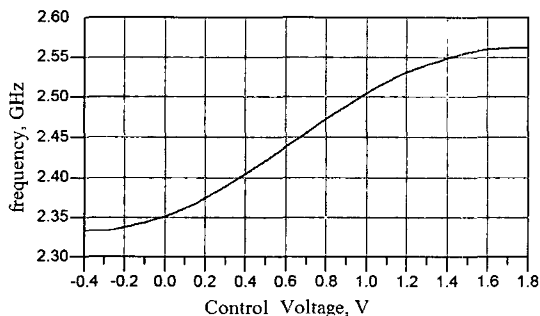

Fig. 7 Tuning characteristic of the voltage-controlled oscillator

6. Conclusion

This paper describes the result of simulation which calculated a gate propagation delay time by using new drain current model and a propagation delay time model.

In the CMOS IC and DRAM, the back gate reverse bias or substrate bias has been widely utilized with the following advantage created: suppressing subthreshold leakage , lowering parasitic junction capacitances , increasing immunity against latch-up or parasitic bipolar etc

In the paper, a proposed VCO based on bondwire inductances and nMOS varactors was implemented in a standard 0.25 μm CMOS process. A proposed VCO operates between 2.33 GHz and 2.56 GHz. With a 2.5 V supply voltage, a 10% tuning range is achieved for a 3 mA supply current. The phase noise shows between -118.3 dBc/Hz and -124.5 dBc/Hz at a 600 kHz offset frequency across the whole tuning range.

A better power consumption and phase noise behavior of the VCO requires the use of inductances with a higher quality factor

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