A Split Time-Ratio Gray Scale Diving Technique for AMOLED Displays

Mayank Prakash Gupta
Dept. of Electrical Engineering and Samtel center for Display technologies, Indian Institute of Technology, Kanpur, India
B. Mazhari
Dept. of Electrical Engineering and Samtel center for Display technologies, Indian Institute of Technology, Kanpur, India

Abstract
A modified Time-Ratio Gray Scale AMOLED drive technique is described in which the frame period is split into two half-frames, each of which is divided into binary weighted sub-frames and driven in the conventional time-ratio manner. The proposed technique improves aperture ratio by reducing TFT sizes in pixel circuits.

1. Introduction
Organic light emitting diode (OLED) displays are being increasingly viewed as the flat panel technology of the future due to their several advantages including wide viewing angle, fast response time, thin size and low cost [1]. These displays can be built either as passive matrix panels consisting of only OLEDs or active matrix panels (AMOLED) in which the OLED is integrated with thin film transistors (TFT) in a suitable manner. Although active matrix displays are more complex and expensive, they have superior characteristics and are necessary for high resolution applications. AMOLED displays can be built by integrating either amorphous Silicon TFTs [2-3] or Poly-silicon TFTs [4-5] with the light emitting diode. Amorphous silicon technology has the advantage of being less expensive, while poly-silicon technology provides better performance and allows system-on-glass to be implemented.

The addressing schemes for AMOLED can be broadly classified into analog or digital techniques. In the analog technique the current through the OLED (and hence brightness) can be varied continuously over a certain range using either current or voltage as an input. This technique has the disadvantage that pixel circuit has to work satisfactorily over the entire range of OLED drive currents which may be problematic due to spatial or temporal variations in TFT threshold voltage. In the time ratio grayscale (TRG) [5] digital drive technique, the OLED is driven either off or on at a single current value and gray levels are obtained by dividing the frame period into a number of binary weighted sub-frames. Depending on whether a pixel is driven or not in each sub-frame, one can have different average currents flowing through the pixel and hence different levels of OLED brightness. The difficulty with this technique is that time available for addressing a pixel reduces as the number of sub-frames is increased to obtain higher number of grey levels. For example, for a frame rate of 50 and VGA resolution, one obtains a minimum row address time of ~0.6μs when 6 sub-frames are used to achieve 6-bit or 64 grey levels. In order to charge the storage capacitor in the 2-TFT voltage driven pixel circuit shown in Fig. 1, TFT sizes have to be chosen large enough to reduce the RC time constant sufficiently below the row address time. Larger TFT sizes results in smaller aperture ratio of the OLED display and also introduce errors as a result of clock-feedthrough problems. This problem worsens with increase in number of sub-frames thereby limiting the number of grey levels that can be practically achieved.

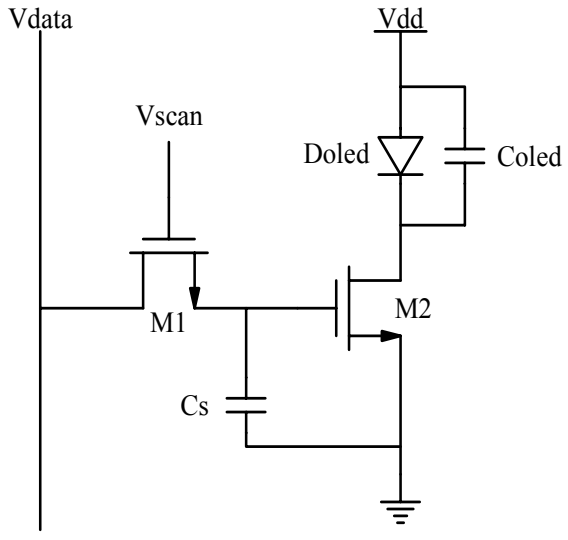

Figure 1: 2-TFT voltage-driven Pixel circuit

2. Proposed Drive Scheme

To alleviate the problem of small row-address time for larger number of gray levels, we propose a modified digital time ratio technique in which the OLED in the on state can be driven at two different current values. To illustrate the proposed technique, consider one possible approach for obtaining 64 grey levels in which two OLED drive currents I_{OA} and $I_{OB} = 8I_{OA}$ are used. The total frame period (T_F) is first divided into two equal half-frames, HF_A and HF_B of duration $0.5T_F$ as illustrated in Fig. 2.

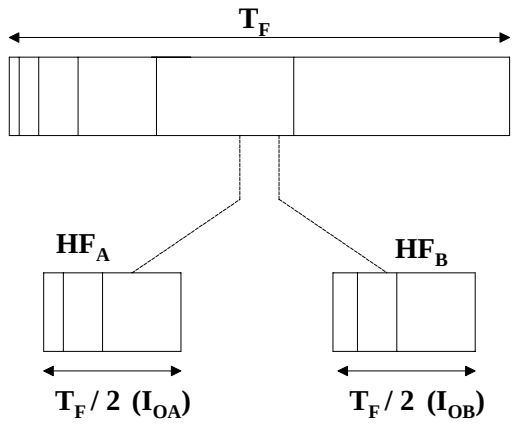

Figure 2: Split-time ratio grayscale technique

Each of the half-frames is subsequently re-divided into three binary weighted sub-frames like in the conventional time ratio technique. For sub-frames $SF^A_{0\to2}$, an OLED current of I_{OA} is used while for sub-frames $SF^B_{0\to2}$, a current of I_{OB} is used. The average current flowing through a pixel can be expressed as :

$$I_{av}=\frac{I_{OA}}{2}\times\left(\frac{a_0 2^0+a_1 2^1+a_2 2^2}{2^3-1}\right)+\frac{I_{OB}}{2}\times\left(\frac{b_0 2^0+b_1 2^1+b_2 2^2}{2^3-1}\right) \quad (1)$$

where $a_{0\to2}$ and $b_{0\to2}$ represent the bits corresponding to sub-frames in half-frames A and B respectively. Substitution of $I_{OB} = 8I_{OA}$ in the above expression shows that 64 gray levels can be achieved by the proposed technique. The new split-time ratio grayscale (STRG) technique however has the advantage that minimum row address time of ~3μs is a factor of 5 larger than that required in the conventional time ratio method. A larger row address time means that smaller TFT sizes can be used yielding more area efficient pixel circuits. For larger number of gray levels, each of the sub-frames can be further subdivided before conventional time ratio technique is applied. Using the methodology discussed, design was carried out for the 2 TFT and 3-TFT voltage driven pixel circuits [6] shown in Fig. 1 and Fig. 3 respectively. For ease of comparison sizes of transistors M1 and M2 in Fig. 1 were taken to be equal and similarly for circuit shown in Fig. 3 TFT sizes were chosen to be equal. Fig. 4 and 5 show minimum TFT sizes required for 2-TFT and 3-TFT circuits to work satisfactorily obtained through AIMSPICE simulations using the default Level 15 PASIA2 TFT parameters. It can be seen that TFT sizes for the STRG drive technique are smaller by a factor of ~3 as compared to those obtained using conventional TRG technique.

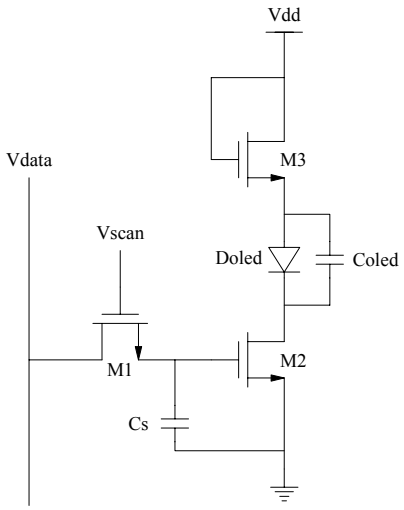

Figure 3: 3-TFT voltage-driven Pixel circuit

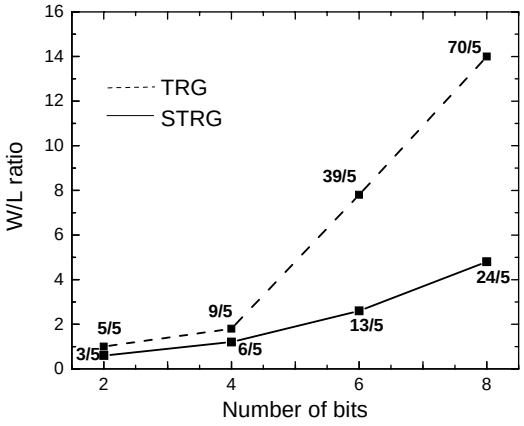

Fig. 4: TFT sizes as a function of no. of bits of grayscale for conventional (TRG) and proposed technique (STRG) for 2-TFT circuit.

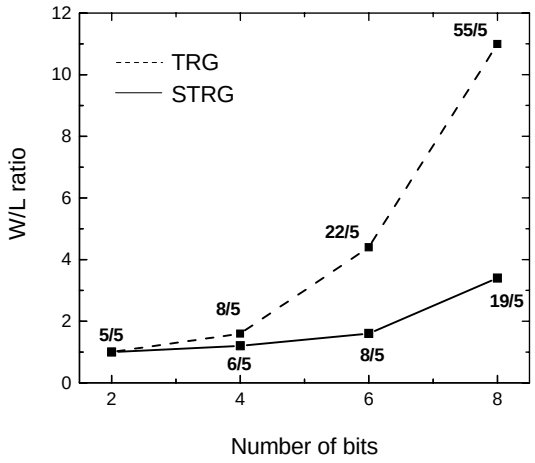

Figure 5: TFT sizes as a function of no. of bits of grayscale for conventional (TRG) and proposed technique (STRG) for 3-TFT circuit

3 STRG: non-uniform splitting

We have so far described a drive technique in which the frame period was divided into two equal half-frames and each of the half-frames consisted of equal number of sub-frames. By relaxing these two constraints, different STRG techniques can be obtained. As an example, consider a scheme STRG-1 in which time of both the half-frames is equal i.e. $T_F/2$ but the number of sub-frames allocated to each half frame is uneven. Assuming that α and β represent the number of sub-frames in HF_A and HF_B respectively, one obtains:

Time for the smallest sub-frame in $HF_A = \dfrac{T_F/2}{2^{\alpha}-1}$

Time for the smallest sub-frame in $HF_B = \dfrac{T_F/2}{(2^{\beta}-1)}$

The relationship between drive currents in the two half-frames can be obtained from the constraint that the light intensity obtained from sub-frames should vary in binary weighted manner

$$I_{OB}\left(\frac{T_F/2}{2^{\beta}-1}\right)=2^{\alpha}I_{OA}\left(\frac{T_F/2}{2^{\alpha}-1}\right) \tag{2}$$

Assuming that a drive current of I_O is used in conventional time ratio technique, one obtains the following constraint for maintaining peak brightness level constant

$$I_{OB}(2^0+2^1...+2^{(\beta-1)})\left(\frac{T_F/2}{2^{\beta}-1}\right) + I_{OA}(2^0+2^1...+2^{(\alpha-1)})\left(\frac{T_F/2}{2^{\alpha}-1}\right)=I_O*T_F \tag{3}$$

Using (2) and (3) we can calculate I_{OA} and I_{OB} and carry out design of pixel circuit.

As a second example, consider a drive scheme STRG-2 in which the time allocated to each half-frames is made different as well. This is done by keeping the time allocated to the smallest sub-frame in each half-frame to be the same but using different number of sub-frames in each half-frame.

Let duration of $HF_B = t_{HF_B}$ ms

Duration of $HF_A = T_F - t_{HF_B}$ ms

$$\frac{t_{HF_B}}{2^{\beta}-1}=\frac{T_F-t_{HF_B}}{2^{\alpha}-1} \tag{4}$$

$$t_{HF_B}=\frac{(2^{\beta}-1)*T_F}{(2^{\beta}-1)+(2^{\alpha}-1)} \tag{5}$$

The currents I_{OA} and I_{OB} can be obtained from the following two constraints

$$I_{OB}=2^{\alpha}I_{OA} \tag{6}$$

$$I_{OB}(2^0+2^1...+2^{(\beta-1)})\left(\frac{T_{HF_B}}{2^{\beta}-1}\right) + I_{OA}(2^0+2^1...+2^{(\alpha-1)})\left(\frac{T_{HF_B}}{2^{\beta}-1}\right)=I_O*T_F \tag{7}$$

Using (4)-(7) we can calculate I_{OA} and I_{OB} and carry out design of pixel circuit. Figure 6 shows a comparison of the STRG-1 and STRG-2 techniques described above with conventional TRG technique for the 3-TFT pixel circuit when the number of bits of the grayscale is odd. The results shown are for the case where number of bits allocated to half-frame A is larger than that allocated to half-frame B by 1, i.e $\alpha = \beta+1$ (in STRG-1) and where number of bits allocated to half-frame B is larger, i.e $\beta = \alpha+1$ (in STRG-2). The superior performance of STRG-1,2 techniques can be clearly noticed from the results. Figure 7 shows a comparison of the STRG-1,2 techniques described above with STRG-0 (technique described in Section 2) for the 3-TFT pixel circuit when the number of bits of the grayscale is even. The results

shown are for the case where number of bits allocated to half-frame A is larger than that allocated to half-frame B by 2, i.e $\alpha = \beta+2$ (in STRG-1) and when number of bits allocated to half-frame B is larger, i.e $\beta = \alpha+2$ (in STRG-2). It can be seen that STRG-2 technique requires smaller TFT sizes as compared to STRG-1 technique.

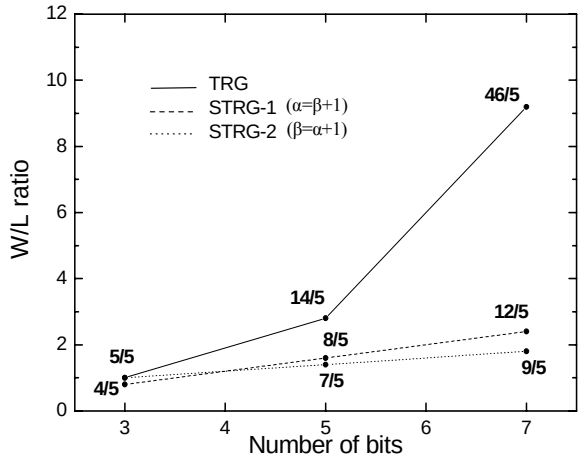

Figure 6: TFT sizes as a function of no. of bits of grayscale for conventional TRG , STRG-1 and STRG-2 techniques for odd no. of bits

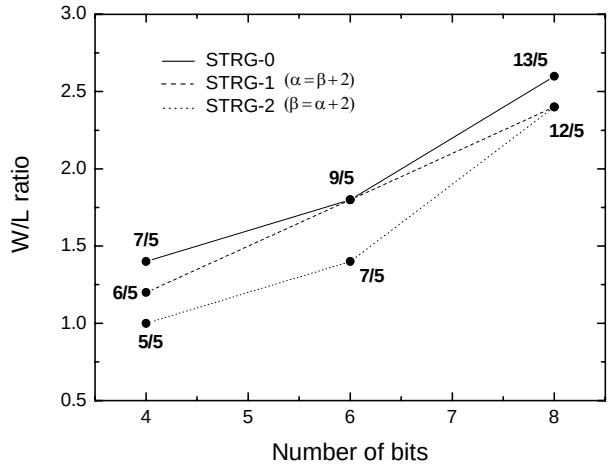

Figure 7: TFT sizes as a function of no. of bits of grayscale for STRG-0, STRG-1 and STRG-2 techniques for even no. of bits

4 Conclusions

To summarize, a new time-ratio drive scheme for AMOLED pixel circuits has been developed which results in more area efficient pixel circuits by allowing larger row address times. It is shown that the proposed technique can result in reduction of TFT sizes by a factor as large as three. It is further shown that better performance can be obtained through non-uniform splitting of frame period along with non-uniform allocation of sub-frames to each of the half-frames.

5 References

[1] C.W. Tang and S. Van Slyke, "Organic Electroluminescent Diodes", Appl. Phys. Lett., Vol. 51, pp. 913, 1987.

[2] Y. He, R. Hattori and J. Kanicki, "Improved A-Si:H TFT Pixel Electrode Circuits for Active Matrix Organic Light Emitting Displays", IEEE Tran. Electron Dev., Vol. 48 p. 1322 (2001).

[3] S. K. Bhowmick, B. Mazhari, "An improved four TFT circuit for Active Matrix Organic Light Diode display", SID 2002, pp. 606, 2002.

[4] Y. Hong and J. Kanicki, "Novel poly-Si TFT pixel electrode circuits and current programmed Active Matrix driving methods for AMOLEDs", SID2002, pp. 618, 2002.

[5] S.W.-B.Tam,Y.Matsueda, H.Maeda, M.Kimura, T. Shimoda and P. Migliorato, "Poly-Si Driving Circuits for Organic EL Displays", Conf. 4925A, Electronic Imaging 2001, San Jose, California, U.S.A.

[6] Joo Han Kim, Jerzy Kanicki, "Amorphous Silicon Thin-film Transistors based Active-Matrix Organic Light-Emitting Displays", SID '02 Digest