Effects of Ramp Type-Common Electrode Bias on Reset Discharge Characteristics in AC-PDP

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Abstract

The ramp type bias voltage applied to the common electrode during a reset-period is newly proposed to lower the background luminance and to improve the address discharge characteristics in AC-PDP. The positive ramp bias voltage is applied during the ramp-up period, whereas the negative ramp bias voltage is applied during the ramp-down period. The effects of the voltage slopes in both the positive and negative ramp bias voltages on the background luminance and address voltage characteristics are examined intensively. It is observed that the optimized positive and negative ramp bias voltages applied to the common electrode during the ramp-period can lower the background luminance and also enhance the address discharge characteristics of the AC-PDP.

1. Introduction

Plasma display panel is a promising candidate for the large area, self-emitting, digital high definition televisions (HD-TVs). The dark room contrast ratio is a very important factor for the high image quality in plasma TV. Thus a lot of researches on the reset waveform have been made [1, 2, 3, 4, 5, 6]. Nonetheless, the investigation on the effects of the common X-biasing condition on the reset discharge characteristics has been often neglected.

Accordingly, this paper proposes the ramp type bias voltage applied to the common electrode during a reset-period so as to lower the background luminance and to improve the address discharge characteristics of a PDP. The positive ramp bias voltage is applied during the ramp-up period, whereas the negative ramp bias voltage is applied during the ramp-down period. The effects of the voltage slopes in both the positive and negative ramp bias voltages on the background luminance and address voltage characteristics are examined intensively.

2. Experimental setup

The 7-in. AC PDP was used as a test with a conventional three-electrode coplanar structure. Fig. 1 shows the driving waveforms including the proposed ramp type bias voltage applied the common (X) electrode. For case 1, the positive ramp bias voltage is applied during a ramp-up reset period, where Δt means the application time of the positive ramp bias, whereas for case 2, the negative ramp bias voltage is applied to the X electrode during a ramp-down reset period, where ΔV means the voltage difference at the ending point of the ramp-down reset period. The address electrode remains grounded during reset period.

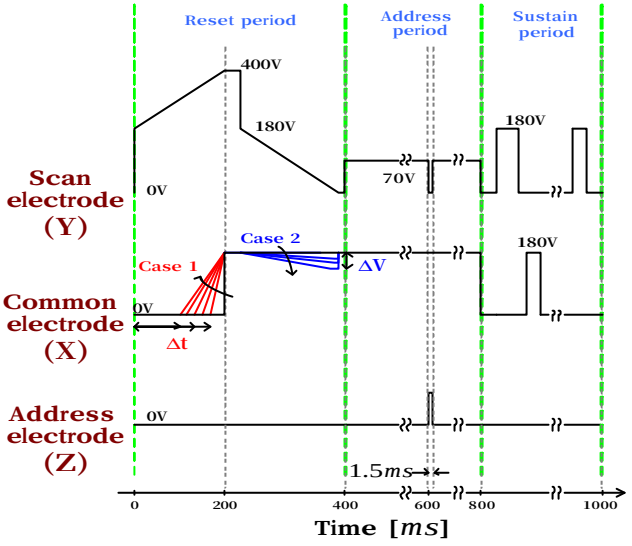

Fig. 1. Driving waveform including proposed ramp-bias voltage applied to common (X) electrode.

3. Results and Discussion

Fig. 2 shows the driving waveforms including the positive ramp bias voltage (=case 1) applied to the X electrode so as to lower the background luminance during the ramp-up period. Fig. 3 shows the changes in the background luminance and the minimum address voltage of the reset discharges as a function of Δt ranging from 100 to 200μs (= conventional case).

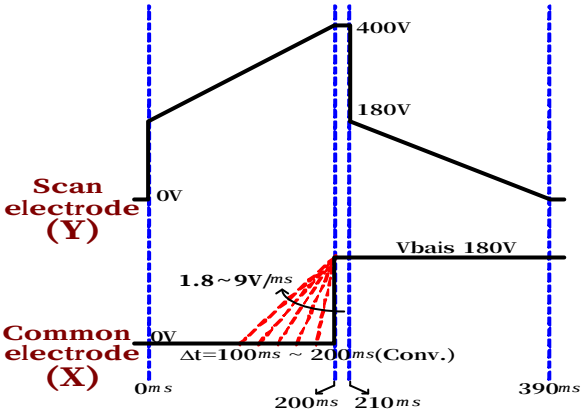

Fig. 2. Driving waveforms including positive ramp bias applied to common (X) electrode during ramp-up period (case 1).

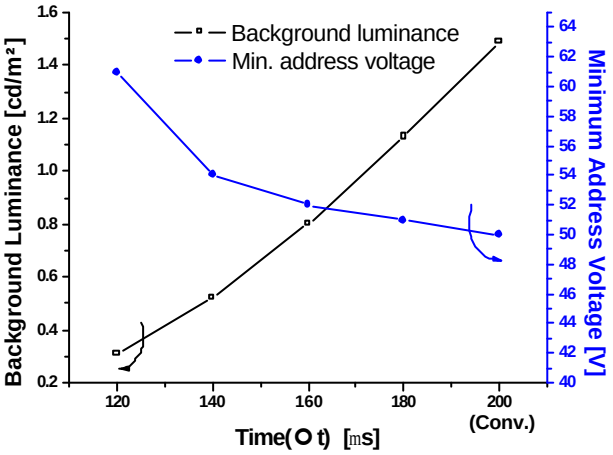

Fig. 3. Changes in background luminance and minimum address voltage during reset discharges as a function of Δt in case 1.

As shown in Fig. 3, with a decrease in the Δt, the background luminance was decreased, but the minimum address voltage was increased. The decrease in the Δt means the surface discharge intensity between the X and Y electrodes, causing the reduction of the background luminance, and also causing the increase in the address voltage due to the insufficient accumulation of the negative charges on the scan (Y) electrode. Fig. 4 shows the IR (828 nm) waveforms emitted during the reset discharge at Δt = 160 μs (= voltage slope of 4.5 V/μs). At Δt = 160 μs, the background luminance was reduced considerably by about 85% even though the minimum address voltage was increased slightly by about 2 V.

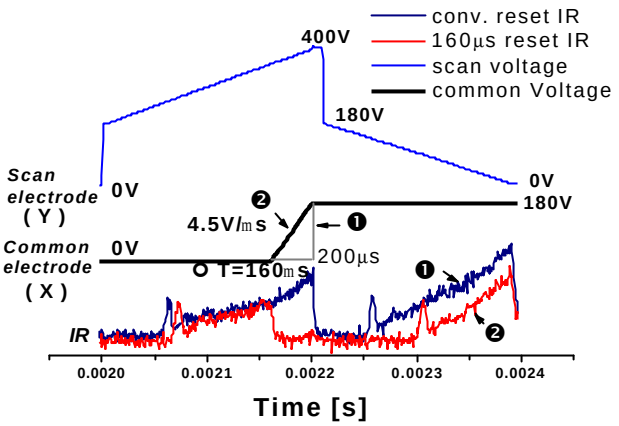

Fig. 4. IR (828 nm) waveforms emitted during reset-period when applying positive ramp bias voltage with voltage slope of 4.5 V/μs at Δt =160 μs.

Fig. 5 shows the driving waveforms including the negative ramp bias voltage (=case 2) applied to the X electrode so as to lower the background luminance and to improve the address discharge characteristics during the ramp-down period. Fig. 6 shows the changes in the background luminance and minimum address voltage during the reset discharge as a function of ΔV in case 2 where ΔV of 0V means the conventional case, and ΔV is varied from 0 to 20V at intervals of 5V. As shown in Fig. 6, with an increase in the ΔV, the background luminance was decreased, and the minimum address voltage was decreased simultaneously. The increase in the ΔV means the weakening of the discharge intensity between the X-Y and X-Z electrodes, thus causing the reduction of the background luminance, and also causing the decrease in the address voltage due to the less erasing of the wall charges accumulating on the Y and Z electrode.

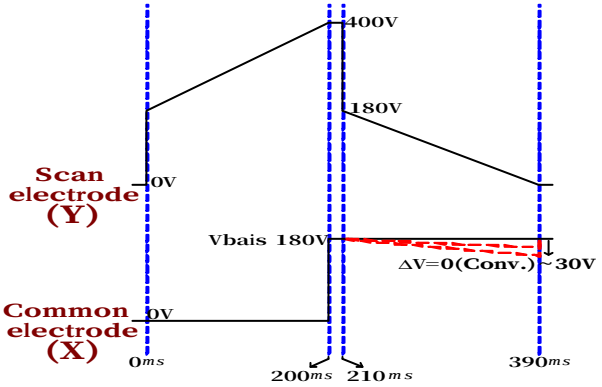

Fig. 5. Driving waveforms including negative ramp bias applied to common (X) electrode during ramp-down period (case 2).

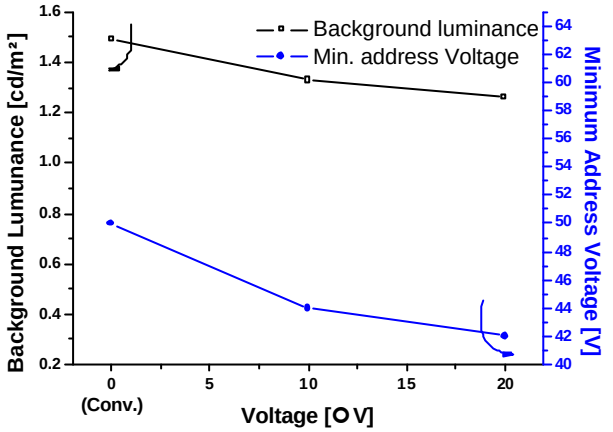

Fig. 6. Changes in background luminance and minimum address voltage during reset discharges as a function of ΔV in case 2.

Fig. 7 shows the IR (828 nm) waveforms emitted during the reset discharge at ΔV = -20V (= voltage slope of -0.11V /μs). At ΔV = -20V, both the minimum address voltage and the background luminance are simultaneously reduced by about 8V and 18 %.

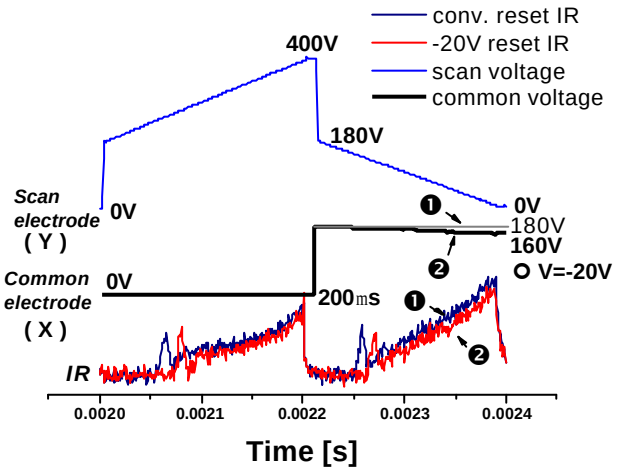

Fig. 7. IR (828 nm) waveforms emitted during reset discharge at ΔV = -20V (= voltage slope of -0. 11V /μs).

Fig. 8 shows the proposed driving waveform including the optimized positive and negative bias voltage applied to the X electrode where Δt is 160 μs, and ΔV is -20V. As a result of applying the driving waveforms of Fig. 8, the IR emission intensity was reduced considerably during the reset-period, as shown in Fig. 9.

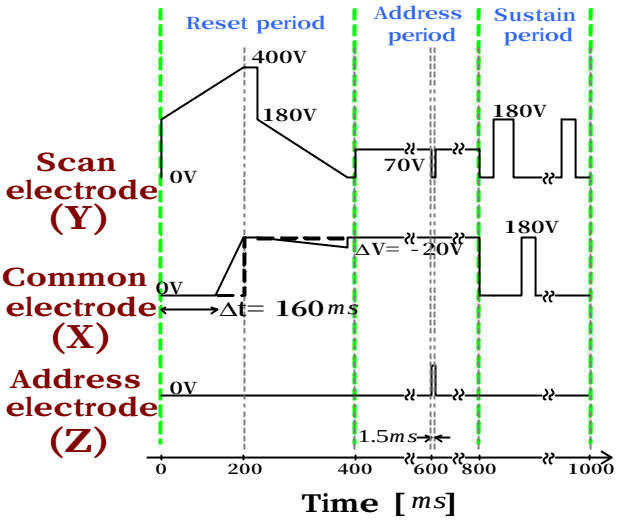

Fig. 8. Proposed driving waveforms including optimized positive and negative ramp bias voltages.

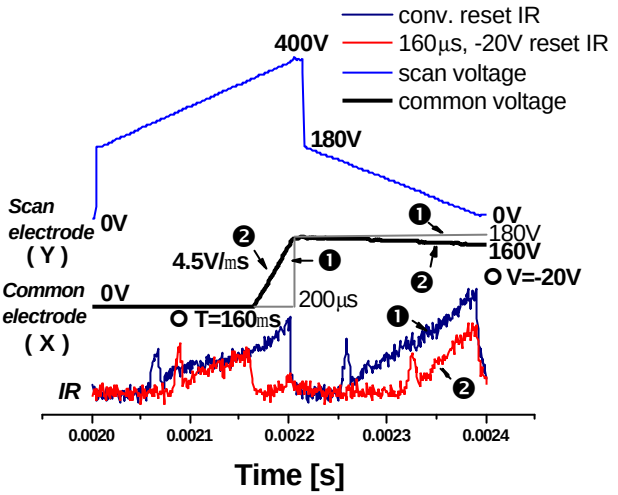

Fig. 9. The light emission of the reset discharge at Δt=160μs, ΔV= -20V.

The address discharge characteristics were improved significantly at an address voltage of 50 V and width of 1.5 μs during the address-period, as shown in Fig. 10. This result means the increase in the dynamic voltage margin when applying the proposed driving waveforms, as shown in Fig. 11. As shown in Table. 1, as a result of adopting the proposed driving waveforms of Fig. 8, both the minimum address voltage and the background luminance are lowered by about 4 V and about 129 %, respectively, in comparison with the conventional driving waveform.

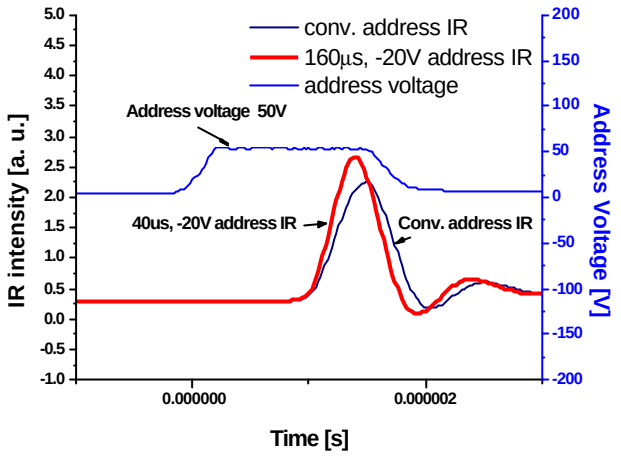

Fig. 10. Comparison of the address light emission in case of adopting the conventional reset and the modified reset driving waveform at the address voltage 50V, the address width 1.5μs.

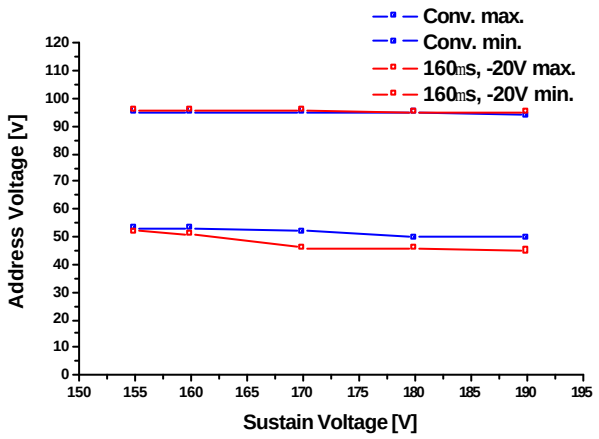

Fig. 11. Comparison of dynamic voltage margins in case of adopting the conventional reset and the modified reset driving waveform.

4. Conclusion

In this paper, the effects of the ramp type-common bias voltage on the reset discharge characteristics are examined in AC-PDP. It is observed that the positive ramp bias during the ramp-up period and the negative ramp bias during the ramp-down period contributes to lower the background luminance and to improve the address discharge characteristics.

	Conventional Reset Waveform	**Proposed Reset Waveform**
X-bias type	Square	Ramp
Application time	200μs	160μs
Slope of X-bias during ramp-down reset period	No change	Negative voltage slope ΔV=-20V (-0.11V /μs)
White luminance	275 [cd/m²]	275 [cd/m²]
Background luminance	1.49 [cd/m²]	0.65 [cd/m²] (129.24%)
Min. address voltage	50 [V]	46 [V]

Table. 1. Comparison of results between the conventional reset and the modified reset driving waveforms.

5. References

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