Stainless Steel Foil Substrates: Robust, Low-Cost, Flexible Active-Matrix Backplane Technology

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Abstract

In this paper, key issues of stainless steel foil substrates for display applications have been described. We studied and analyzed technical issues on substrate passivation/planarization to control surface roughness and capacitive coupling from conductive substrates. A thick (either multiple or single) passivation/planarization layer needs to be applied on the nonelectronic-grade stainless steel substrate to provide a smooth surface and electrical insulation from the conductive substrate. Especially for large size, high-resolution display applications, low k and thick passivation/planarization layers should be used for appropriate capacitive coupling. Based on our initial study, a unit area capacitance of less than 2 nF/cm^2 of passivation/planarization layers is needed for 32" HD TV OLED displays.

1. Introduction

Today, glass substrates are mainly used in the flat panel display industry owing to their many advantages, such as transparency, high temperature process compatibility, low dimensional change under temperature or wet process cycles, high chemical resistance, and high moisture barrier. However, the glass substrates are generally fragile, and their cost and weight become higher as the substrate size increases. In addition, it is difficult to be used for roll-to-roll (RTR) process applications. Therefore, for robust, low-cost, eventually RTR process-capable backplanes, many research groups have been working on fabricating devices or electronic circuits on alternative substrates, such as plastic [1][2] and stainless steel (SS) foil [3][4][5][6] substrates. Several key properties of glass, a few plastic, and SS substrates are compared in Table 1.

For plastic substrates, due to their limited thermal budget, low-temperature (<150 °C) processes have been used for hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) [1], and thermal barrier engineering has been applied for low-temperature polycrystalline silicon (LTPS) TFTs [2]. However, for SS foil substrates, high-temperature polycrystalline silicon (HTPS) TFT [5] and conventional (250~300 °C) a-Si:H TFT technology can be used. In addition, in the solar cell industry, the SS foil substrate is already being used for RTR process manufacturing [7].

In addition to the higher thermal budget of SS foil substrates, they have several advantages, such as long-term stability, compatibility with standard complementary metal oxide silicon (CMOS) process, better thermal dissipation, good adhesion to the following thin films, flexibility, ruggedness, availability at low cost, possible common signal or power provision, and potential electromagnetic interference shielding. In fact, the SS itself is a good oxygen and moisture barrier, which is critical for OLED display applications. Recent progress in top-emission OLED technology [8][9] removes transparency from the required property lists of the substrate.

In this paper, some of the key issues of stainless steel foil substrates have been studied and analyzed, which includes options for passivation/planarization layers for nonelectronic-grade SS substrate and capacitive coupling from the conductive substrate.

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Table 1. Substrate Property Comparison

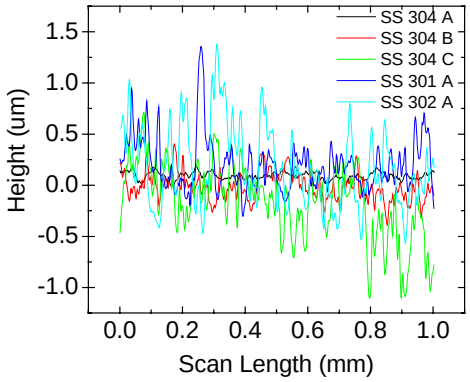
Substrate	Max. Process temperature	CTE	Transparency	Chemical Resistance	Moisture Uptake	Surface
Stainless steel	900 °C	~18 ppm	Opaque	OK	~0 %	Rough (vendor dependent)
Glass	600 °C	~3-4 ppm	Transparent	Good	~0 %	Good
Kapton	300 °C	~15-35 ppm	Semi-transparent (Orange)	Good	~2-4 %	Rough
PEN	150 °C	~20 ppm	Transparent	Good	~0.8 %	Good
PET	120 °C	~20 ppm	Transparent	Good	~0.8 %	Good

2. Issues of SS Foil Substrates

2.1 Surface Roughness

There is no easily available SS foil substrate manufactured specifically for electronics applications; therefore, the surface roughness of SS foil substrates is generally poor and dependent upon manufacturing methods. Most of the cold-roll type SS foil substrates, without specific surface treatment, typically show vertical stripe patterns on the surface reflected from the roller. Figure 1 shows an example of a micrograph picture of the surface stripes and measured variable surface roughness of SS foil substrates (3 mil to 8 mil thickness) from different vendors. The graph shows profilometry data that contains substrate curvature during the measurement. Therefore, we read the neighboring peak-to-peak variation to compare the results with each other. The neighboring peak-to-peak roughness (scanning perpendicular to the stripe patterns) varies from 2~3 um down to less than 0.2 um over scan length of 1 mm, with a 6 mg stylus force, and at 50 um/s scan speed, for different substrates.

(a)



(b)

Figure 1. Surface roughness of SS foil substrates: (a) an example of a micrograph picture of surface stripes, and (b) surface roughness profilometry measurement result (scan direction is perpendicular to the stripes patterns).

We used the SS 302 substrate with a rough (0.8~1.2 um) surface to investigate the effect of passivation/ planarization layer on the surface roughness change and substrate leakage behavior. To reduce surface roughness, we first used the electropolishing method for the surface treatment and a single layer of passivation/planarization coating (~300 nm thick SOG). However, because of the poor (0.8~1.2 um) peak-to-peak surface roughness, the thin SOG layer was not thick enough for the electrical isolation of the conducting substrate. As shown in Figure 2, when a TFT is fabricated on a SS foil substrate with a thin SOG passivation/ planarization layer, we observed leakage current flow through the conductive substrate. Although a different surface treatment, such as the

chemical-mechanical polishing (CMP) method [9], can also be applied for further improvement of the substrate surface roughness, it might not be the right solution for a low-cost, RTR process given that it is typically a high-cost process.

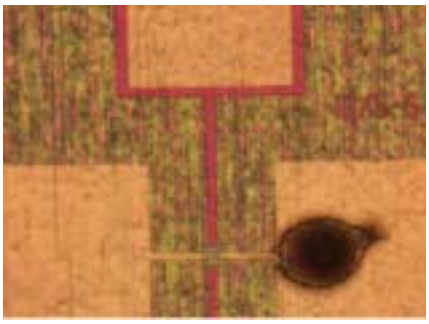
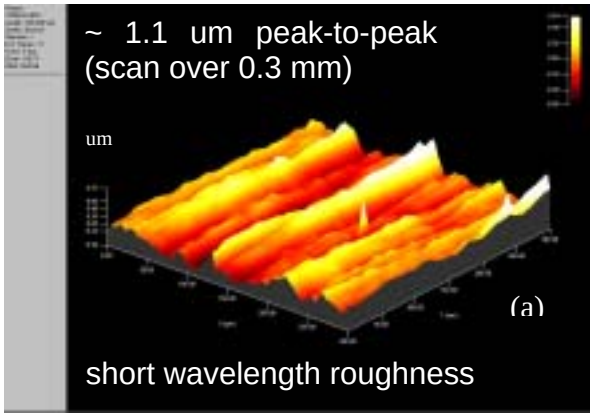


Figure 2. Damaged TFT during measurement as a result of substrate leakage current

Therefore, we have placed more focused on optimizing the passivation/planarization layer for nonelectronic-grade SS substrates. We studied double-coatable SOG and benzocyclobutene (BCB) to further reduce the surface roughness. We observed the surface roughness changed from short to long wavelength-type patterns for both double-coated SOG (1~1.2 um thick) and BCB (~1.2 um thick). The surface roughness was ~0.4 um peak-to-peak (scan over 0.3 mm) and 0.2~0.3 um (scan over 1 mm) for a double layer SOG and BCB, respectively, as shown in Figure 3. Based on our initial result, BCB is one of the good candidates for single layer thick passivation/ planarization coating so that we can use off-the-shelf nonelectronic-grade SS foil substrate for electronic applications. At the same time, we are currently investigating new manufacturing methods of metal foil substrates to achieve super smooth surface



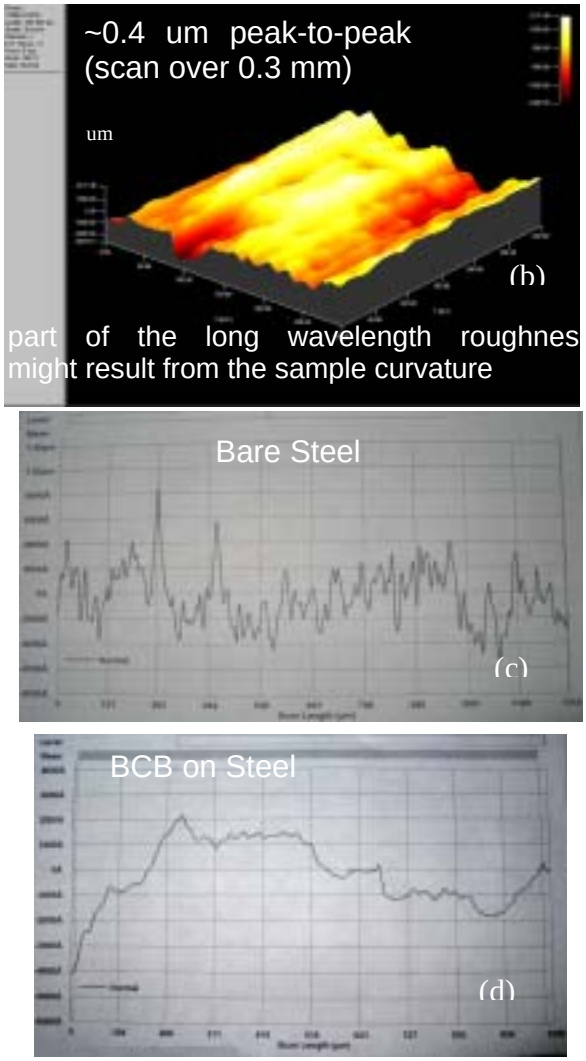


Figure 3. Measures of surface roughness: (a) and (c) are obtained for bare SS substrate, and (b) and (d) are obtained after coating a double-layer of SOG and a single-layer BCB, respectively.

roughness. We believe that the surface roughness of nonelectronic-grade SS foil substrate of less than 0.2 um is preferred and a surface roughness of less than 100 nm can be achieved with this type of single coating.

2.2 Capacitive Coupling

When electronic devices or circuits are fabricated on a conductive substrate, capacitive coupling between electrode lines and the conductive substrate through the passivation/planarization layer is very important for an appropriate circuit operation. Therefore, in

addition to the smoothing surface, the passivation/ planarization layer should have a low dielectric constant and thick-layer processability without serious film stress or cracks to reduce capacitive coupling from the conductive substrate. The bi-layer of SOG and silicon oxide [5], and the single layer of silicon oxide [4] or silicon nitride [3] have been typically used in display applications. However, the dielectric constant of these materials are relatively high (4~7), requiring large thicknesses to reduce the capacitive coupling effect from the conductive substrate. Therefore, so-called low k materials should be applied for this application.

To evaluate the required dielectric constant and corresponding film thickness of the passivation/ planarization layer, we analyzed the effect of the capacitive coupling of SS foil substrates on data and scan line delay for many different combinations of dielectric constant and passivation/planarization layer thickness. Figure 4 shows unit-area capacitance for different dielectric constant and layer thickness by using the first approximation parallel plate capacitor equation as follows.

$$c = \frac{\varepsilon_r \varepsilon_0}{t},$$

where ε_r and ε_0 are dielectric constants of passivation/ planarization material and air, respectively, and t is the layer thickness.

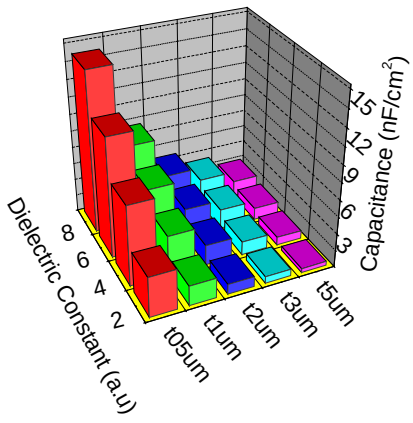
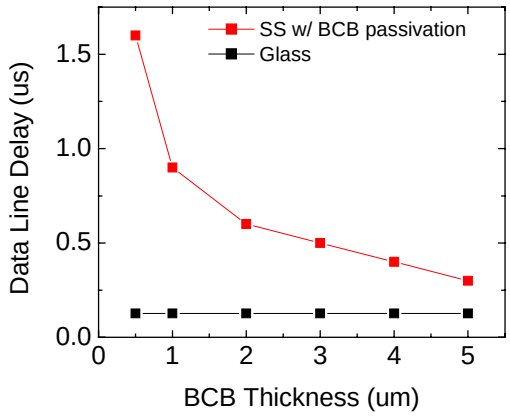


Figure 4. Unit area capacitance distribution for different dielectric constant and layer thickness.

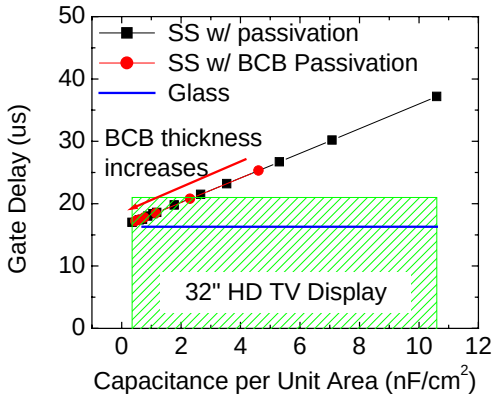
Typically, the capacitance (C) and resistance (R) of the electrode lines will determine the operational RC time delay, which directly affects the possible operational display size. We expect that a SS foil substrate would cause more data and scan line delay as a result of the additional capacitive coupling from the conductive substrate. Therefore, we analyzed the capacitive coupling effect on data and scan line delay and compared the result with the glass substrate case. Figure 5 shows the data and scan line delay for different unit area capacitance, which is calculated by using the first approximation equation as follows.

$$Line \cdot Delay = R_P \times C_P \times N^2 \text{ [11]},$$

where, R_P and C_P are of equivalent resistance and capacitance for each pixel, and N is the number of pixels in a row or column, respectively. R_P was calculated by assuming aluminum lines with a 10 and 20 um width, and a 100 and 200 nm thickness for scan and data lines, respectively. C_P was calculated by considering capacitive elements of (1) scan-to-data crossover, (2) S/D overlap of switching TFT, (3) switching TFT channel, (4) scan-to-substrate, and (6) data-to-substrate. Figure 5 show an example of data and scan line delay analysis based on 32" OLED HDTV (RGBW stripe, 1920 × 1080i) applications for glass and SS foil substrates. A two TFT pixel circuit has been assumed for this analysis and a two-dimensional field solver (HyperLynx) was used in combination with the parallel plate approximation. Figure 5(a) shows that the data line delay can be 0.4~1.6 us for SS foil substrate when different thicknesses (0.5~5 um) of the BCB material is used for the passivation/planarization layer. It is noted that, for a glass substrate, 0.24 us was obtained for glass substrate from our analysis. Figure 5(b), shows that the dielectric constant and the passivation/ planarization layer thickness need to be carefully selected. In this case, the pixel data charging time, including the data line effect, was assumed to be about 10 us, which would depend on the TFT



(a)



(b)

Figure 5. Data (a) and scan (b) line delay analysis for 32" OLED HD TV applications.

characteristics and OLED structure, and unit area capacitance of less than 2 nF/cm^2 is required. According to Figure 5(b), a BCB layer of the thickness of 2~3 um thickness can be used for this application.

5. Conclusion

We have studied key issues of SS substrates, focusing on surface roughness and capacitive coupling in display applications. Double-coated SOG and single-coated BCB layers show promising results for surface roughness control for nonelectronic-grade SS substrates, though it is still preferred to start with substrates with smoother surface (<0.2 um peak-to-peak preferred) for single-coating process applications. Based on the analysis, we ascertained that the unit capacitance of less than 2 nF/cm^2 is needed from the passivation/planarization layer, for 32" OLED HD TV applications.

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