PCB power-bus 에 장하된, 결합제거 커패시터와 금속선의 상관관계적 영향 연구

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Correlated effects of decoupling capacitors and vias loaded in the PCB power-bus

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Abstract

This paper investigates how the PCB power-bus sturcture's characteristics are influenced by the loading of decoupling capacitors that are placed close to vias, on purpose or not. It is worthwhile to see the correlated effects of the aforementioned lumped elements in that when they inevitably share one DC power-bus they will result in positive or negative changes in the PCB EMC design. The EM fields and impedance profiles are rigously calculated on the PCB power-bus cases loaded with the above components and their effects will be given to bring better PCB EMC countermeasurs.

Key words : PCB level EMC, PCB power-bus, decoupling capacitors, vias, field calculation

1. Introduction

Communication systems today are typically equipped with stacked PCBs with ascending operating frequency and complexity in their architecture. The more densely each of the layers is populated, the more care needs taking of to avoid unwanted EMIs. In particular, when it comes to the digital functions together with the analog ones for one circuit, a couple of layeres are assigned as power suppliy planes like DC power-bus and ground, and they form cavity-type parallel plates that will possibly leave the system with spurious resonances as in area-fills[1-6].

To take some steps against the resonance, its precise prediction is prerequisite with rigorous analyses of the power-bus structures without any approximation[2,3]. Based upon the results, it needs examining that placing local elements on the power plane and ground affects the initial resonances[2-6]. As the local components, decoupling capacitor(deCap)s are commonly used to circumvent the resonance. However, in a significant number of cases, this is not that effective due to the disturbance of other surface mounting elements or vias.

This paper suggests the full-wave based calculation of the DC power-bus lodaed with decoupling capacitors along with vias in the same structure. Besides the electromagnetic fields and impedance profiles, the correlated influence of the decoupling capacitors and vias is given.

2. Theory

The PCB typically holds drivers, traces and receivers. Also, multiple PCBs are stacked, following the design rule to assure required EMC properties. They are connected through vias or isolated between digital and analog functions. Most of them can be considered parallel plates without loss of accuracy in electromagnetic modeling. Particularly, the DC power supply plane and its ground are a good example of parallel planes. In Figure 1, such a structure is illustrated with Wx by Wy by Wz in size.

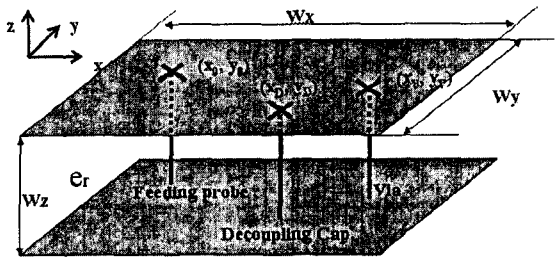

Figure 1. DC power bus modelled as parallel-planes

Using the feeding probe denoted as (X_0, Y_0), the current is given and works as the DC supply. The point of field excitation is assumed to coincide with that of the observation at (X_0, Y_0). The intermediate region between the metal planes corresponds to the PCB's substrate and 4.2 and 0.02 are each chosen as its relative dielectric constant and loss tangent, which is confined within the magnetic-walls. Outside the planes, air is assumed as the medium. The electromagnetic field(E_z) is expressed as well-known as in [2] and can be converted to the voltage or interpreted as the impedance with no difficulty. On account of its denominator's zeroes, the impedance profile in the frequency range shows a spiky behavior as resonances. The resonance points are determined depending on size-related modes, substance and frequency. What is intriguing with the resonance is attributed to the emiited radiation, ground bounce, Delta-I noise, etc that end up with EMIs. Researches have seen the mounted elements on either or both of the parallel planes can change the resonance characteristics. Many such activities have followed the mounting of decoupling capcitors to lower the impedance's increase due to the stacked PCB's inductive loop behavior. In addition, other local elements such vias are forced to exist together with the decoupling capacitors in the same power-bus. Since it is easy to guess that

they affect each other and the overall resonance characteristcis, both of them need considering for one geometry. In Figure 1, the placement assigns a via and a decoupling capacitor at (X_D,Y_D) and (X_V, Y_V), respectivley. These lumped elements' influences are reflected in the field calculation as is in Ref. [3].

3. Numerical Results

Among other things, in the number 1 spot, the impedance profiles are inspected on the power-bus of 200mm by 150mm by 1.5mm. This structure is dealt with for 4 different loading conditions. The cases are of no loading, only 1 deCap, 1 via alone, and 1 deCap and 1 via. For all the cases, it is electrically fed at (X_0=0, Y_0=0), and one type of via at (X_V =100mm,Y_V =75mm) and one sort of decoupling capacitor at (X_D =200mm,Y_D =75mm) are used. Quantatatively, the decoupling capacitor is set at C_D=47pF with R_D=5.2Ohms and L_D=3.8nH to weaken the (1,0) resonance mode. Similary, the value of the via is given as L_V=1.097nH as can be done in Ref. [5].

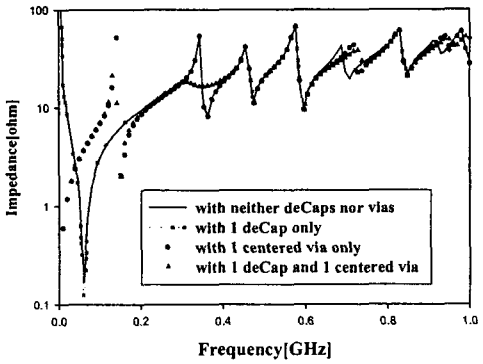

Figure 2. Input impedance profile of the DC power bus with and without loading of the deCap and the via

As case 1 goes with neither vias nor deCaps, it shows its original resonance modes. With only the deCap loaded, case 2 sees the successful damping of (1,0)-mode. It is a matter of course that the other resonance modes at higher frequencies undergo slight changes. In case 3, a via centered at the planes shifts (2,0) and (0,2) modes and results in no intended damping, but causes an additional resonance around 120MHz which is believed to be a critical noise. This via still brings that extra resonance with (1,0) resonance mode damped by the deCap in case 4. These noises could stem from added inductance. As of now, we'll take a gander at the field distribution(Ez) over the DC power-bus, for it will make things clear. Primarily, Ez is plotted with and without the deCap at 376MHz of (1,0)-mode.

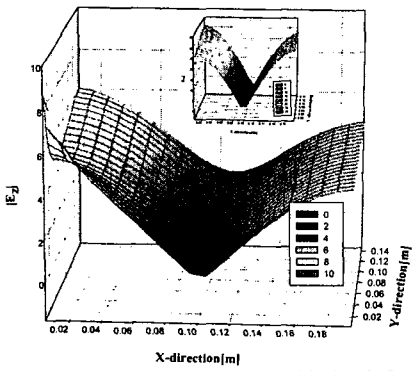

Figure 3. Ez over the DC power bus with the deCap (Inset : without the deCap)

Without any loading except for the feed, Ez is formed satisfying (1,0)-resonance mode condition where along the edges one half wavelength and zero variation of Ez are seen along the x and y-directions, respectively. And the intensity of Ez is of significace. Applying the deCap to it, the damping occurs and is quite ettective, since most of the plane area comes to have reduced intensity. Secondarily, the via is added to the deCap. The location is the center of the planes and the simulation is performed at 376MHZ as before.

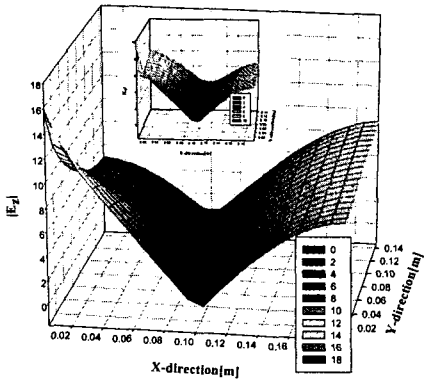

Figure 4. Ez over the DC power bus with the deCap and the via (Inset : with the deCap alone)

Obviously, the deCap dominantly lowers the intensity of Ez in both the cases. And note the via at the center plays an important role in reducing more of the resonance, while the Ez has not changed a bit right at the feeding point. Going through the macro-model pole extraction, it is found out that below (1,0)-mode frequency, the deCap loaded case has no complex poles with -14952 and $-5.19*10^9$ (like LPF), while the addition of via results in the poles at $-4.32*10^6$ +/- $j0.184*10^9$ with $j=\sqrt{-1}$ (like BPF). At this point, one must bear in mind that if the via is placed near a null of Ez that is primarily damped by the deCap correlated effects of damping can be achieved.

4. Conclusion

Considering the EMI-causing resonances related to the DC power-bus modelled as cavity-type parallel planes, the structure's field and impedance are rigorously calculated. And then, certain deCaps are mounted on the planes to damp the undesired resonances. This leads to success in suppressing the specific resonance. Particulary, this paper enlightens the way vias can affect the function of deCaps in a positive manner for better PCB EMC countermeasures. And their LPF and BPF behaviors have been mentioned in terms of pole extraction.

Acknowledgement

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References

[1] S. Van den Berghe et al, "Study of the ground bounce caused by power plane resonances," *IEEE Trans. EMC*, vol. 40, no.2, pp. 111-119, May 1998

[2] J.Trinkle et al, "Efficient impedance calculation of loaded power ground planes," in *Proc. 15th Zurich Symp. EMC*, Zurich, Switzerland, Feb.18-20, 2003, pp. 285-290, I8

[3] T. Okoshi, *Planar Circuits for Microwaves and Lightwaves*, Berlin, Germany: Springer-Verlag, 1985

[4] V. Ricchiuti, "Supply decoupling on fully populated high-speed digital PCBs," *IEEE Trans. EMC*, vol. 43, pp. 671-676, Nov. 2001

[5] J. Fan et al, "DC power-bus modelling and design with an MPIE formulation and circuit extraction," *IEEE Trans. EMC*, vol. 43, no.2, pp. 426-436, May 2001

[6] X. Ye et al, "DC power-bus design using FDTD modeling with dispersive media and surface mount technology," *IEEE Trans. EMC*, vol. 43, no.4, pp. 579-587, Nov. 2001

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