Load-Adaptive Address Energy Recovery Technique

for Plasma Display Panel

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Abstract

A high speed address recovery technique for AC plasma display panel(PDP) is proposed. By removing the GND switching operation, the recovery speed can be increased and switching loss due to GND switch also becomes to be reduced. The proposed method is able to perform load-adaptive operation by controlling the voltage level of energy recovery capacitor, which prevents increasing inefficient power consumption caused by circuit loss during recovery operation. Thus, the technique shows the minimum address power consumption according to various displayed images, different from prior methods operating in fixed mode regardless of images. Test results with 50" HD single-scan PDP(resolution = 1366×768) show that less than 350ns of recovery time is successfully accomplished and about 54% of the maximum power consumption can be reduced, tracing minimum power consumption curves.

I. Introduction

Many kinds of digital display have been developed to meet the market requirements but PDP takes an advantage over other flat panel display(FPD) by the wide view angle, large screen, high brightness, and thinness[1]. Thanks to the attractive merits, PDP is expected to widen its market share in the digital display market. Fig. 1 shows the simplified PDP structure with three electrodes and matrix cell structure. It consists of two glass plates with chemically stable rare gases filled between them. The scanning and sustaining electrodes are built on the front glass, which is coated with dielectric layer and the addressing electrode is on the rear glass. A desired color light can be obtained by exciting the phosphors on the addressing electrode to emit visible light with the ultraviolet photons generated by gas discharge[2]. The PDP cell structure naturally forms capacitances among three electrodes and it causes heating problem of switching devices. Therefore, an energy recovery circuit should be developed in order to save power consumption of address drive ICs. The half-resonant method that is similar to sustain driver suggested by L.F. Webber et. al. and quarter-resonant

method have been adopted by most of the PDP makers. Power consumption is successfully reduced with the help of these methods but they cannot be applicable to PDPs requiring a high speed addressing such as large size and high resolution PDPs or single-scan PDPs, due to their slow recovery speed and circuit loss. Another simple method to reduce heat stress is proposed by Y. Sano et. al[3]. It is very simple structure using only resistor but excessive heat dissipated from resistor cannot be accommodated by larger size PDPs.

In this paper, a new address energy recovery technique with fast recovery operation for AC PDP is proposed. This method has load-adaptive power saving characteristic with the help of charge-pumping operation, which makes it possible to consume the minimum address powers according to various images by controlling the voltage level of recovery capacitor. The load-adaptive operation is desirable characteristic since energy recovery operation may not give a help to power saving at small data switching images whose address powers are dissipated mostly by circulating current for energy recovery rather than data switching. Prototype circuit has been designed and experimented for 50"HD single-scan PDP to show the validity of the proposed circuit.
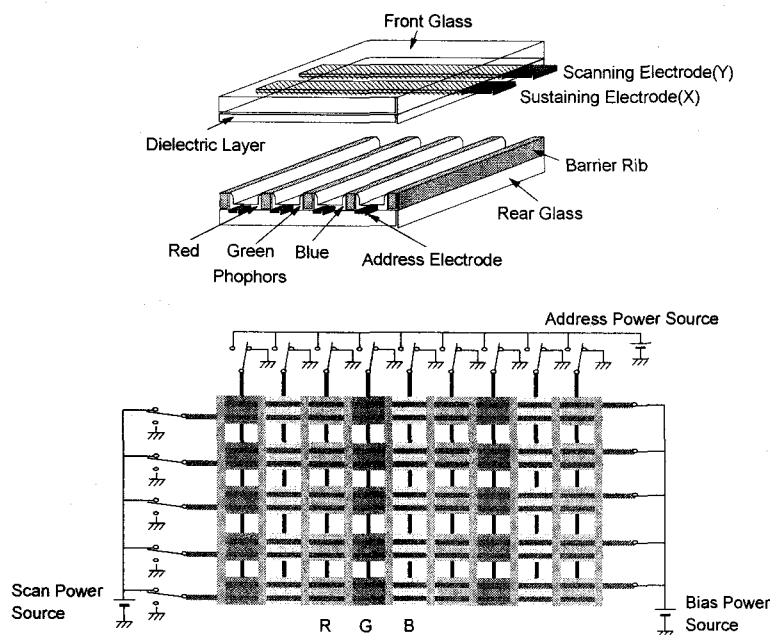

Fig. 1   Simplified PDP structure with three electrodes

II. Mode analysis

Fig. 2 is the proposed fast address energy recovery circuit(AERC) with address drive IC model at heavy data switching pattern. It has separate recovery path to reduce switching loss of recovery switches. GND switch is replaced by diode only for GND clamping to save recovery time and switching loss. At white dot on/off image that produces the most address power consumption in practice, the address data switching occurs at each scan line and all capacitances existing among three electrodes are applied. In this case, address drive ICs can

be modeled by four switches of A_{H1}, A_{L1}, A_{H2}, and A_{L2}, as shown in Fig. 5, and the load capacitance C_L can be written as

$$C_L = \frac{N_d}{N_M}\left(\frac{1}{2}C_{b,line} + \frac{1}{3}C_{a,line}\right)$$ (1)

where N_M is the number of recovery circuit blocks. The key waveforms of the proposed method with this address driver model are depicted together in this figure and the mode diagrams of proposed method are shown in Fig. 3. Before the mode explanation, it is assumed that parasitic components of switching devices are ignored and $L_1=L_2=L$.

Mode 1 $(t_0 \leq t < t_1)$: Mode 1 begins at t_o when A_r is turned on. Since A_a switch is already maintained as conducting state, there forms current path including A_a, L_2, D_f, and A_f in sequence. Accordingly, I_{L2} linearly is increased with the slope of $(V_a-V_c)/L$ to store the magnetic energy in the inductor L_2. The current is expressed as

$$I_{L2} = \frac{V_a - V_c}{L}(t - t_0).$$ (2)

The current built up before the energy charged in panel capacitances is recovered helps to reduce transition time from V_a to zero and, thus, increase the energy recovery speed. By minimizing recovery time, address pulse width that is necessary for address discharge is ensured as long as possible. In addition, since this build-up current can be used for the voltage level control of recovery capacitor, recovery operation becomes different according to load condition.

Mode 2 $(t_1 \leq t < t_2)$: When A_a is turned off, the current built up during mode 1 flows through C_L, L_2, D_f, and A_f in sequence. The resonant current caused by panel capacitance starts to flow and the terminal voltage V_o goes down from V_a to zero. During this mode, the equations of I_{L2} and V_y are written as:

$$I_{L2} = I_{L2}(t_1)\cos\omega_c(t - t_1) + \frac{V_a - V_c}{Z}\sin\omega_c(t - t_1),$$ (3)

$$V_o = V_c + (V_a - V_c)\cos\omega_c(t - t_1) - ZI_{L2}(t_1)\sin\omega_c(t - t_1)$$ (4)

where $Z = \sqrt{\dfrac{L}{C_L}}$ and $\omega_c = \dfrac{1}{\sqrt{LC_L}}$.

Mode 3 $(t_2 \leq t < t_3)$: After mode 2, the diodes of D_g is turned on and V_o is clamped by GND level. Accordingly, the current I_{L2} starts to flow through D_g, D_f, L_2, and A_f. I_{L2} is ramped down to zero with the slope of V_c/L and it can be written as follows:

$$I_{L1} = I_{L1}(t_2) - \frac{V_c}{L}(t - t_2).$$ (5)

If data switching happens during V_o is maintained as around GND level, switching losses of data drive ICs, which should be dissipated by heat, can be reduced.
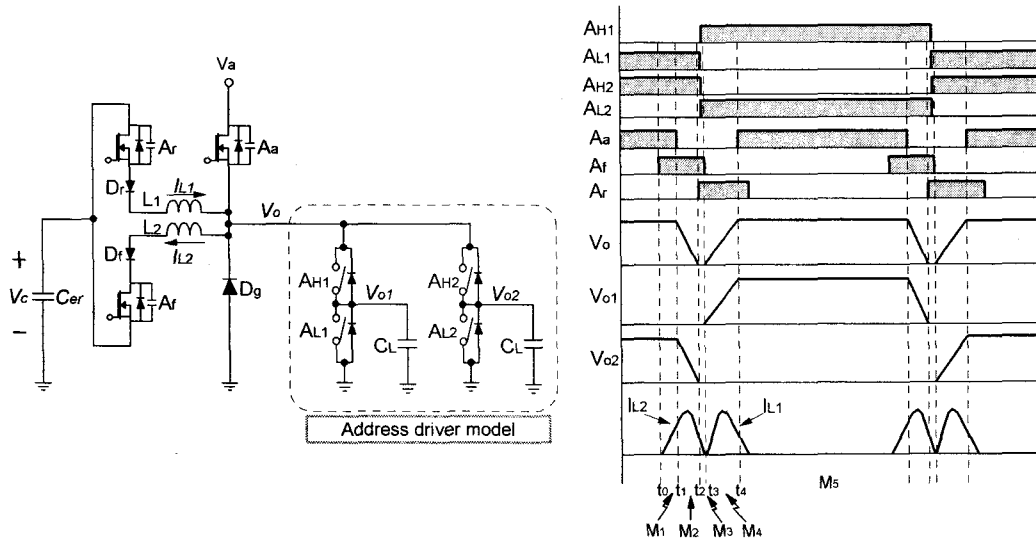
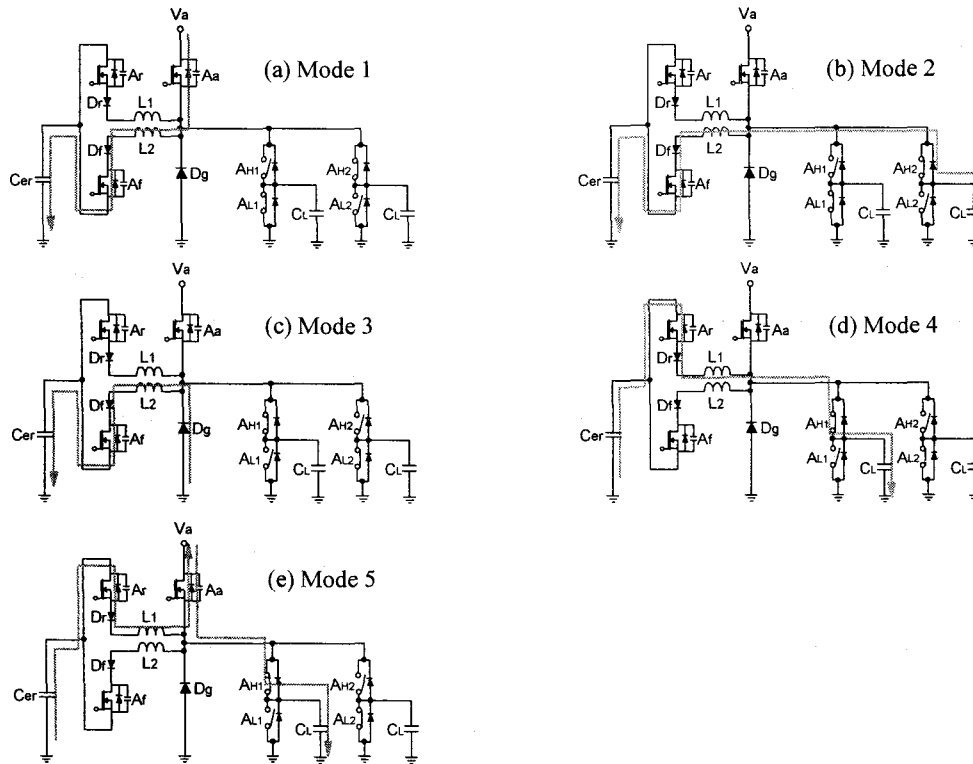Fig. 2 Proposed method with address driver model and its key waveforms

Fig. 3 Operational mode diagram

Mode 4 $(t_3 \leq t < t_4)$: After I_{L2} is reduced to zero, the current starts to flow to C_l through A_r, D_r, L_l, and A_{H1} because A_r is already turned on during mode 3. The terminal voltage V_o goes up from zero to V_a. Similar to eqs. (3) and (4) in mode 2, I_{L1} and V_o can be written as

$$I_{L2} = \frac{V_c}{Z}\sin\omega_c(t - t_3), \tag{6}$$

$$V_o = V_c \left(1 - \cos \omega_c \left(t - t_3 \right) \right). \tag{7}$$

Mode 5 ($t_4 \le t < t_5$) : After increasing the terminal voltage of address drive ICs increase to V_a, the rest of magnetic energy of L_1 starts to be recovered toward address voltage source through A_r, D_r, L_1, and the body diode of A_a and it makes the ZVS condition of A_a and A_g. During this mode, I_{L1} decreases to zero with the slope of $(V_c-V_a)/L$, which is expressed as

$$I_{L1} = I_{L1}\left(t_4 \right) + \frac{V_c - V_s}{L}\left(t - t_5 \right). \tag{8}$$

When A_a is turned on to induce address discharge, mode 1 starts again.

III. Operational characteristics

To realize an image, all channels of address drive IC generate data and their switching numbers are changed from zero to the number of scan lines. The energy recovery capacitor voltage level V_c is important factor to control recovery operation. This level is controlled by the build-up current explained in mode 1, which would make V_c tend to maintain a higher voltage level than $V_a/2$. For instance, while address recovery circuit comes into no load condition, i.e, no address data condition, there exits only build-up current flowing into energy recovery capacitor. In this case, V_c eventually increases to V_a and the recovery operation cannot be performed anymore. As data gets increased, then discharge current from energy recovery capacitor becomes increased and it makes V_c lower to some voltage level. Accordingly, the energy stored in panel capacitor starts to be recovered by address recovery circuit. At small data switching images, recovery operation may not give a help to save power consumption because the inefficient power consumption caused by circulating current for recovery operation is larger than that caused by data switching. Therefore, this load-dependant recovery operation is desirable characteristic to minimize address power consumption. The expression of V_c can be determined by power-balancing condition of recovery capacitor during recovery operation, which is written as

$$\int \left(i_{charge} \times v_c \right) dt = \int \left(i_{discharge} \times v_c \right) dt. \tag{9}$$

Using this concept, the expression of V_c can be obtained as

$$V_c = \left(1 - \sqrt{\frac{(N_s - N_1)C_L}{\sqrt{N_s T_b^2 / 2L + N_1 C_L \left(1 + \sqrt{1 + \left(T_b / \sqrt{LC_L} \right)^2} \right)}}} \right) V_a. \tag{10}$$

where, N_s is the number of total scan electrodes and N_1 is the number of scan electrodes that address data exist on, Also, The current build-up time T_b is defined as t_1-t_0. The recovery capacitor voltage is the function of circuit parameters and load conditions. According to load applied to recovery circuit C_L and N_1, Calculated V_c with eq. (10) is in Fig. 4. As N_1 and C_L are increased, V_c level becomes lowered. That is to say that while ineffective energy dissipated by address dive ICs is saved when heavy data switching occurs, recovery

operation can be minimized in case of small data switching images at which power consumption caused by recovery operation is larger than data switching.

IV. Recovery time T_R

To determine address recovery time T_R defined by sum of falling transition time T_f and rising transition time T_r, it is necessary to express the transition time between GND and V_a as the function of design parameters. The falling transition time T_f defined by t_2-t_1 is obtained from eq. (4) by replacing V_o with zero. However, V_c varies according to load changes and it causes that V_o may not go down to zero. Thus, this definition of T_f can not be applicable to all load conditions. Fortunately, t_2-t_1 is nearly equal to t_3-t_1 which is defined by the time during which I_L goes down to zero and it can be used for all load conditions. Therefore, using eq. (3), T_f can be approximately expressed as follows:

$$T_f = \sqrt{LC_L}\left[\pi - \tan^{-1}\left(\frac{ZI_{Lo}}{V_a - V_c}\right)\right] \qquad (11)$$

where $I_{Lo} = (V_a - V_c)T_b / L$. Assuming that the circuit does not contain any parasitic components, the rising transition time T_r is same as eq. (12). Since the transition time of this proposed method is the function of T_b as well as L, the pulse rising and falling times can be shortened by adjusting T_b. It helps to widen the address discharge time by minimizing the time required by recovery operation.
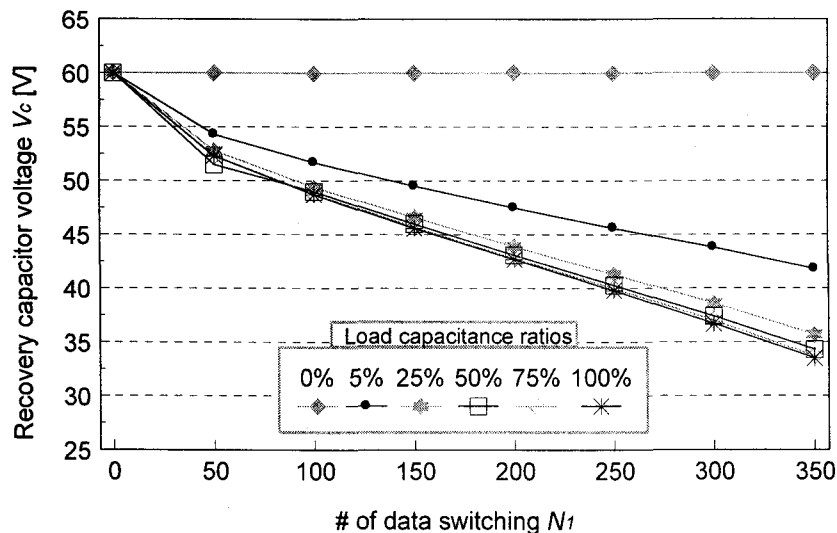

Fig. 4 V_c changes according to load capacitance and number of data switching at $V_a = 60$V
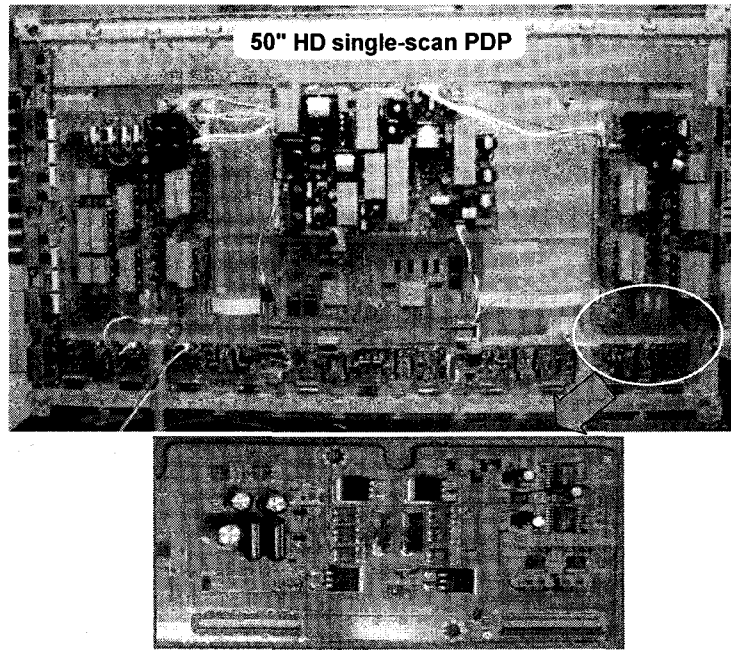
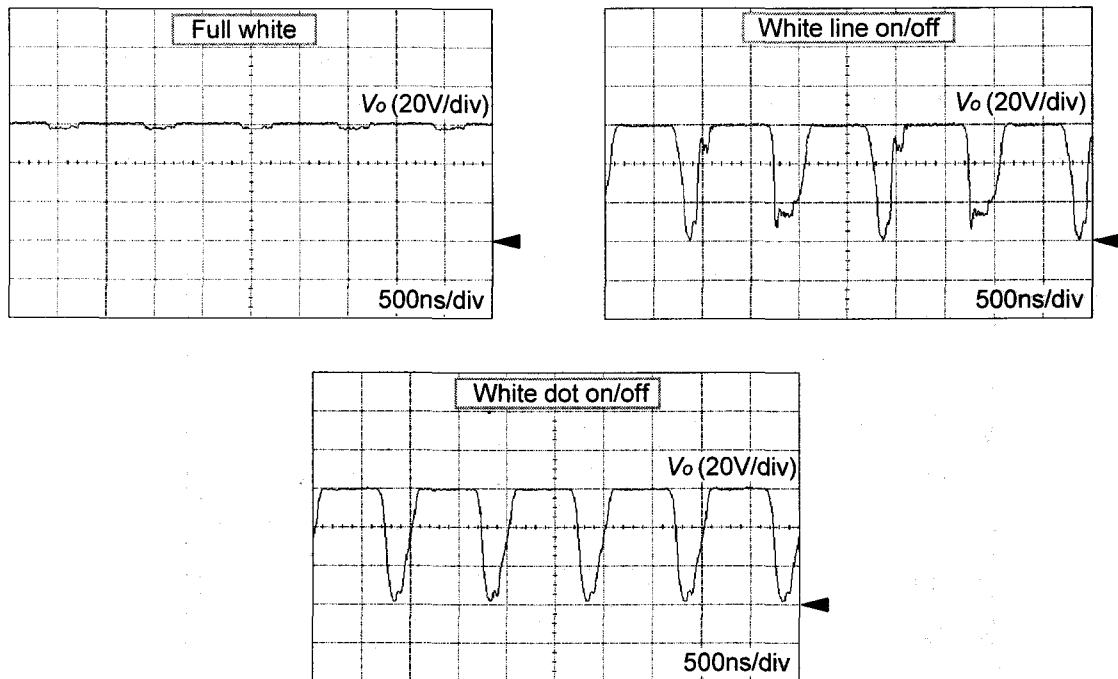Fig. 5 Prototype of proposed method built in 50" HD single-scan PDP

Fig. 6 Measured terminal voltages according to data switching

V. Experimental results

A prototype circuit of the proposed method has been designed for 50" HD single-scan PDP with specifications of Address voltage V_a = 60V, total recovery time T_R = 350ns, and max. load capacitance per one circuit block C_L=28nF. Key design parameters of L=0.1μH

and T_b=20ns has been chosen under considering that too small values of L is not difficult to design and too large build-up time may cause a power loss of circuit due to large circulating current. Fig. 5 shows prototype system of proposed method built in 50″ HD single-scan PDP. Because address data are applied from single side, the address signal buffer board which six recovery circuit blocks are installed on are allocated only at bottom side. The detailed figure of one circuit block is also shown. Measured terminal voltages according to data switching are shown in Fig. 6 and less than 350ns of recovery time is successfully accomplished. As explained before, full white image which does not require a heavy data switching makes the recovery operation stop automatically and heavy data switching images such as white line on/off and white dot on/off images lower the energy recovery capacitor voltage so that the energy charged in capacitance can be recovered. Fig. 7 shows the power consumption comparisons according to address energy recovery methods. It shows that conventional series LC resonant type reduces well at heavy switching images but dissipates inefficient power caused by circulating current at small switching images. On the other hand, the proposed method can trace the minimum power consumption curve owing to load-adaptive operation. Thus, at small data switching images, address power consumptions has the characteristic similar to the case without recovery circuit and, at heavy switching patters, address power can be saved like conventional recovery method. The measured data shows that above 54% of address power can be reduced.
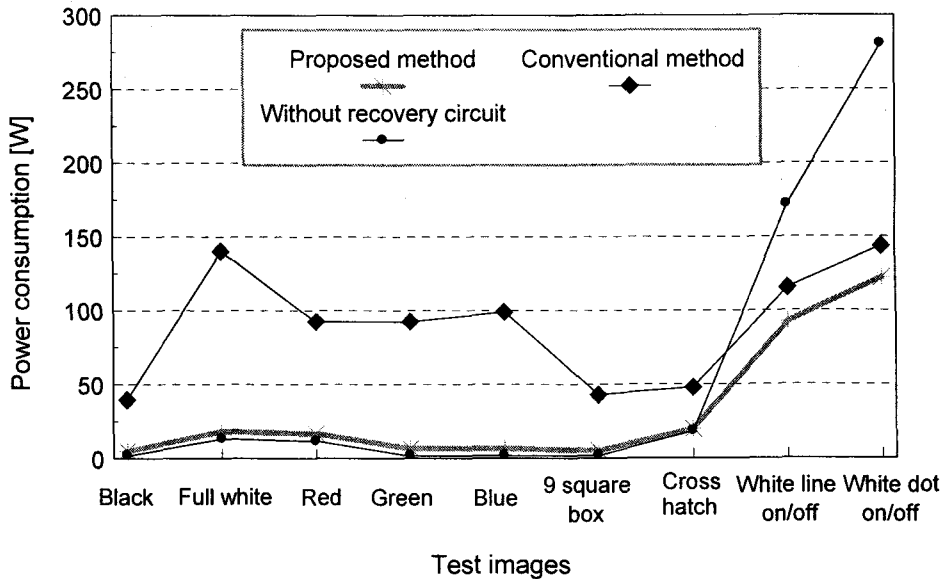

Fig. 7   Address power consumption comparisons

VI. Conclusions

In this paper, a high speed address recovery technique for AC plasma display panel is proposed. By controlling the voltage level of energy recovery capacitor, the proposed method has load-adaptive characteristic that shows minimum address power consumption according

to displayed images. In addition, recovery speed can be increased by saving the GND hold time because this method does not use GND switch operation. Prototype circuit has been implemented for 50" HD single-scan PDP and six blocks was designed to drive overall panel. Test results show that less than 350ns of recovery time is successfully accomplished and the maximum power consumption can be reduced from 280W to 130W.

References

[1] A. Sobel, "Plasma Displays,"IEEE Trans. on Plasma Science, vol. 19, no. 6, pp. 1032-1047, December, 1991.

[2] H. Hirakawa, T. Katayama, S. Juroki, H. Nakahara, T. Nanto, K. Yoshikawa, A. Otsuka, and M. Wakitani, "Cell Structure and Driving Method of a 25-in(64cm) Diagonal High-Resolution Color ac Plasma Display," Poc. Sym. Society for Information Display, vol. 29 pp. 279-282, 1998.

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