기능성 원자간력 현미경 캔틸레버 제조 방법과 특성

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Method of manufacturing and characteristics of a functional AFM cantilever

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ABSTRACT

To illustrate an application of the field effect transistor (FET) structure, this study suggests a new cantilever, using atomic force microscopy (AFM), for sensing surface potentials in nanoscale. A combination of the micro-electromechanical system technique for surface and bulk and the complementary metal oxide semiconductor process has been employed to fabricate the cantilever with a silicon-on-insulator (SOI) wafer. After the implantation of a high-ion dose, thermal annealing was used to control the channel length between the source and the drain. The basic principle of this cantilever is similar to the FET without a gate electrode.

1. Introduction

When an electric charge spreads on or beneath the surface of a dielectric media, the distributions are measured through scanning probe microscopes (SPMs), namely: electrostatic force microscopes[1] (EFM) and scanning capacitance microscopes[2-4] (SCMs). These SPMs have spatial resolutions of tens of nanometers, with a potential sensitivity of several mV. SPMs, however, are rather slow in terms of measuring speed, which is determined by the feedback time constant. The surface potential variations are measured by enhanced measuring speed and voltage sensitivity, after an active device, such as a field effect transistor[5, 6] (FET) or a single electron transistor[7] (SET), is mounted on or near the scanning probe of the cantilever in an atomic force microscope (AFM). The AFM is used to scan the surface while the FET or the SET detects the surface potentials.

This study focuses on a cantilever array in the entire SPM-based storage system. The FET cantilever is an array cantilever (with or without a tip) that was developed as a field effect transistor (FET) device type for the application of charge storage. A combination of the MEMS technique of surface and bulk, and the complementary metal oxide semiconductor (CMOS) process, was used to build the

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cantilevers on the silicon-on-insulator (SOI) wafer. The device characteristics were examined using the HP 4155A-parameter analyzer in the dielectric gate, which consists of a high-quality oxide-nitride-oxide (ONO) film, or a special aluminum oxide (Al_2O_3 or AlO_x) on p-type silicon.

2. Process and Results of FET cantilever

Figure 1 shows the schematic diagram of the FET cantilever process without a sharpened tip (Type I; top) and with a sharpened tip (Type II; bottom). The silicon-on-insulator (SOI) wafer was used to fabricate the FET cantilever. The thickness of the top Si of the boron-doped layer, the insulating layer, and the bulk Si layer under the insulator, measured 4.0 ± 0.5 μm, 1 μm, and 540 μm, respectively. Both Si layers and the SOI wafer had a (100) direction and a 4-inch diameter.

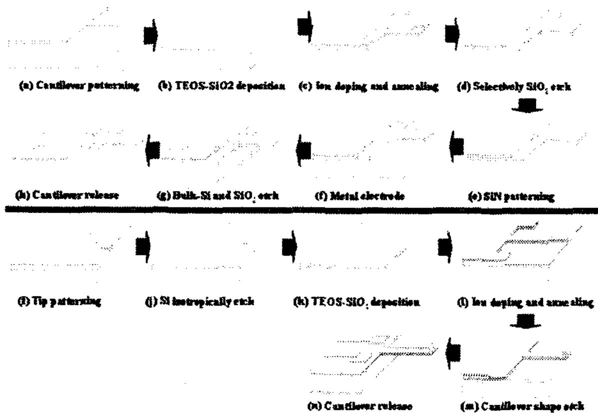

Fig. 1: Schematic diagram of process flow of SOI-based FET cantilevers. Top region is the case of without a sharpened tip (Type-I) and bottom region is the case of with a sharpened tip (Type-II).

Figure 2 shows the resulting FE-SEM images of each cantilever, with or without a sharpened tip. Figure 2(a) shows the 4×1 array and 5×5 array types of FET cantilever on the left and right side, respectively. Figures 2(b) and 2(c) show the magnified FET cantilever region of the 4×1 array and 5×5 array types, respectively. In addition, Figure 2(d) shows the three types of FET cantilevers developed in this study, namely: two arms (left image), three arms (center image), and single arm (right image). Figure 2(e) shows the magnified image of the cantilever edge without a sharpened tip. On the other hand, Figure 2(f) shows the magnified image of the Type II process with a height tip of about 2 μm. The source and drain were not visible in the FE-SEM images, even though they were deposited into the cantilever arm. The channel length was about 0.5 μm in the center region. The resonance frequency of the Type II and Type I FET cantilevers measured around 60 kHz in a non-contact mode operation.

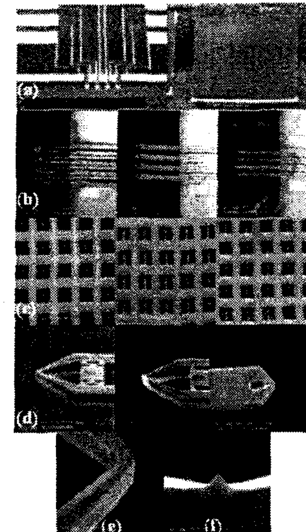

Fig. 2: FE-SEM images of array-type FET cantilevers. (a) is 4 × 1 array (left hand) and 5 × 5 array case (right hand). (b) is closed up view of 4 × 1 array. (c) is magnified images of 5 × 5 array. (d) is the shape of three types of cantilevers. (e) is closed up view of cantilever edge in the case without a sharpened tip. (f) is magnified image of the tip in the case of with a sharpened tip.

Figure 3 shows the drain current (I_D) as a function of the voltage between the source and

drain (V_{DS}) within various gate biases (V_G) using an ONO gate in dark condition [Figure 3(a)] and with lights on condition [Figure 3(b)] of Type II cantilever. The I_D-V_{DS} device characteristics were very similar to those of the conventional n-channel MOSFET (NMOSFET). In a Type I cantilever, which is not shown here, the characteristic curves were very similar to Type II cantilever. In addition, it was apparent that the drain currents, with or without a sharpened tip, were less different. This may be due to the distance of the sharpened tip from the channel point to the gate material, which is greater than that of the cantilever without a sharpened tip. The cantilevers of two- [Figure 2(d), left] and three-arms type [Figure 2(d), center] had the similar properties as the conventional NMOSFET and the resistance (R_{DS}) of 0.7 MΩ, which was measured at I_D = 2.0 μA. The cantilever of single-arm type [Figure 2(d), right], however, the R_{DS} was like as multi-arms type and I_D was abruptly increased when the V_G is about ≥ 6 V. At a gate bias of 0 V, the curves appear different from those of a conventional NMOSFET, suggesting a shift in the threshold voltage (V_T). This may have resulted from the surface or subsurface charge in the present oxide-nitride-oxide sample. In addition, we have been studied the I_D-V_{DS} device characteristics using an oxidized Al film in dark condition of the Type II cantilever (not shown in this study). In this experiment, the V_G was applied of negative voltages to the gate material. However, no difference was noted of the I_D in the V_G is about ≤ -10 V due to the poor dielectric quality arising from the oxidized Al film in the air.

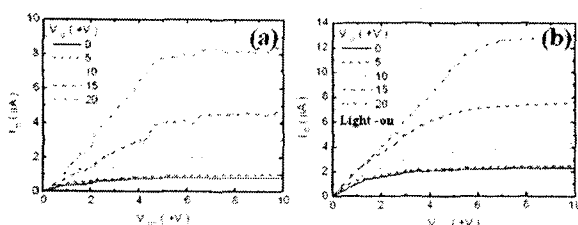

Fig. 3: Characteristics curve graph by voltage-current of two different cantilevers. (a) is current-voltage results of with a sharpened tip in dark condition. (b) is results of with a sharpened tip case in light-on condition.

3. Summary

In this study, Si-based-array FET cantilevers, with and without a sharpened tip, were fabricated using the MEMS and modified CMOS process. The resonance frequency of the FET cantilevers, with and without a sharpened tip, was measured at around 60 kHz, using a non-contact mode operation. The device characteristics of the FET cantilevers resembled those of the conventional NMOSFET.

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