기능성 원자간력 현미경 캔틸레버를 이용한 표면 전위 측정

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Surface potential mapping using a functional AFM cantilever

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Key Words : 차세대 이동형 정보저장장치, 기능성 캔틸레버

ABSTRACT

The surface potential variations are measured, according to the enhanced measuring speed and voltage sensitivity, using an active device, such as a field effect transistor (FET)[1-3]. In this study, the surface potential was mapped in the patterned SiO_2 medium at room temperature. An improved FET-tip cantilever, which has a source, a drain, and an n-channel, was used in this study. The potential images were analyzed both in the contact mode and the non-contact mode, using only a pre-amplifier system instead of a lock-in the amplifier.

1. Introduction

The surface potential variations were measured according to the enhanced measuring speed and voltage sensitivity, using an active device, such as a field effect transistor (FET) [1-3] or a single electron transistor (SET) [4], which is mounted at or near the scanning probe of the cantilever in an AFM. The AFM is used to scan the surface while the FET or SET detects the surface potentials. Chen *et al.* fabricated an AFM cantilever with an FET sensor [1], using the two-dimensional electron gas (DEG) of a GaAs/GaAlAs quantum. When operated at 4 K, a charge noise of « 1 e/$Hz^{1/2}$ was achieved at 30 kHz. They measured a charged tip with a spatial resolution of 340 nm. When the SET was used on an AFM cantilever [4], a high charge sensitivity of 0.01 *e* was obtained. They mapped a surface potential, a surface electric field, and a dopant fluctuation on semiconductor surfaces with a spatial resolution of 100 nm. Despite their good resolution, the cantilevers with an FET or an SET probe were operated only at a cryogenic temperature. Park *et al.* proposed a resistive probe that has a semiconductor resistor at the apex, where surface charges in the ferroelectric material could be observed, without a signal modulation technique, at room temperature [5]. Park called this probe "scanning resistive probe microscopy" (SRPM), and reported the measurement results of the triglycine sulfate (TGS) single crystal and $Pb(Zr_{0.4}Ti_{0.6})O_3$ (PZT) thin films. This probe was proven to have enough sensitivity to detect the image on

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the surface charge of the ferroelectric domains at high speed, and the ability to locally modify the ferroelectric domains.

In this study, the surface potential was mapped in the patterned metal and SiO_2/Si medium at room temperature. An improved FET-tip cantilever, which has a source, a drain, and an n-channel, was used in this study. The potential images were analyzed both in the contact mode and the non-contact mode, using only a lock-in amplifier system instead of a rock-in amplifier.

2. Experiments and Results

As shown in Figure 1(a), it is generally very difficult to assemble a metal-oxide-semiconductor field-effect-transistor (MOSFET) device directly on the AFM cantilever. Since several complex processes are involved therein, the device speed may be too slow to effectively scan the AFM cantilever. A cantilever with an FET structure, which has a source and a drain, has been developed to overcome this limitation. In Figure 1(b), a sample is used as the gate. As shown in the figure, when a bias (V_{DS}: source-drain voltage) is applied to the source, the current flows toward the drain while the current I_D is controlled by the gate bias. This scheme works not only in the non-contact AFM mode, on a bare conducting surface, but also in the contact AFM mode, on a conducting sample with dielectrics or a metal oxide.

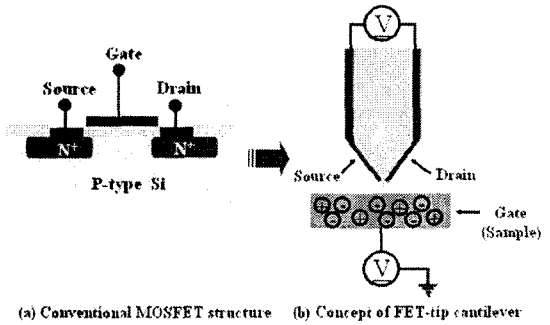

Fig. 1: Cross section of a field-effect-transistor (FET) structure. (a) The schematic diagram of conventional n-channel metal-oxide-semiconductor field-effect-transistor (NMOSFET) device. (b) Concept of working mechanism of a FET-tip cantilever.

Figure 2 shows the FE-SEM images of the cantilever with a sharpened tip. As Figure 2(a) and 2(b) show, the FET-tip cantilever has two arms, and a magnified image with a height tip of about 2 μm. The FET-tip cantilever can be processed with 7 mask layers. The thickness of the top Si of the boron-doped layer, the insulating layer, and the bulk Si layer under the insulator, measured 4.0 ± 0.5 μm, 1 μm, and 540 μm, respectively. Both the Si layers and the SOI wafers had a (100) direction and a 4-inch diameter. The SOI wafers were thermally oxidized at a thickness of 1 μm. Conventional photolithography was performed to produce the circular pattern and to process the probe tip. Dry etching was also performed. The wafer was reoxidized, while the area over the source and drain were dry-etched. A high-dose P^+ implantation was performed to create a highly conductive source and drain after activation in a furnace. The top Si layer was isotropically dry-etched to form the cantilever shape. Aluminum contact electrodes were made using silicon nitride film masks. The bulk Si and middle oxide in the SOI wafer were dry-etched, while the remaining resists were ashed to release the cantilever. The source and drain were not visible in the FE-SEM images, even though they were deposited into the cantilever arm. The channel length was separated about 0.5 μm in the center region. The resonance frequency of the FET-tip cantilever measured around 60 kHz in the non-contact mode operation.

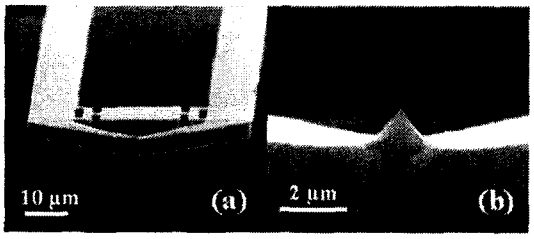

Fig. 2: FE-SEM images of FET-tip cantilever. (a) The shape of two-arm case of FET-tip cantilevers. (b) Magnified image of the tip in the case of with a sharpened tip.

Figure 3 shows the AFM image [Figure 3(e)] and the surface potential maps [Figures 3(a)-3(d)] as a function of gate bias, at room temperature. The AFM was operated in the contact mode, using a scan length of 5 μm × 5 μm. Together with the AFM image, the I_D was measured with a V_{DS} of 0.10 V. As the biases of 5.00 [Figure 3(a)], 7.00 [Figure 3(b)], 10.50 [Figure 3(c)], and 20.00 V [Figure 3(d)] were applied to the bottom-side Si substrate, the spatial variation of the surface potential was visible. The variation originated from the oxide thickness. The gray scale denotes the measured I_{DS}, which was represented by the 0.2 V converted white voltage and the 0 V black voltages. Based on the sharpness of the measured surface potential, the spatial resolution of the scanning FET microscope was estimated to be about 90 nm.

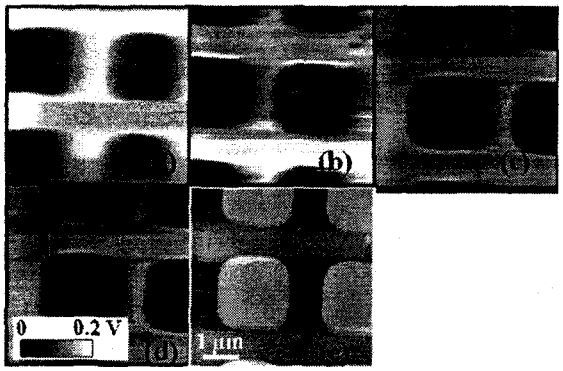

Fig. 6: The images of a surface potential in SiO_2/Si system versus various gate voltages (V_G) at the room temperature. The source-drain bias (V_{DS}) is fixed at 0.10 V and the bias is applied in the backside Si at (a) 5.00, (b) 7.00, (c) 10.50, and (d) 20.00 V, respectively. (e) A typical AFM topography.

3. Summary

This study has demonstrated surface potential images using a new FET-structure cantilever, at room temperature. The FET-tip cantilever was used to successfully read the potential for the dielectric gate and the metal system. The image of the surface potential slowly increased as the gate voltage increased in the SiO_2/Si system. When the V_{DS} was higher than +6.00 V, the images were not clear due to AFM lithography. In addition, the experiment showed that the charge-trapping time in the SiO_2/Si system was very fast.

Acknowledgement

This work was supported by National R&D Project for Nano Science and Technology.

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