Wafer-Level MEMS Packaging : Fundamentals, Reliability Issues and Applications

Suk-Jin Ham
(Samsung Advanced Institute of Technology/Korea)

Wafer-Level MEMS Packaging

S. J. Ham*, B. G. Jeong, J. H. Lim, M. S. Choi, S. W. Lee
K. D. Jung, J. S. Hwang, M. C. Lee, J. O. Kwon, Q. Wang,
W. B. Kim, and C. Y. Moon

Packaging Center
Samsung Advanced Institute of Technology
E-mail* : sj.ham@samsung.com

Contents

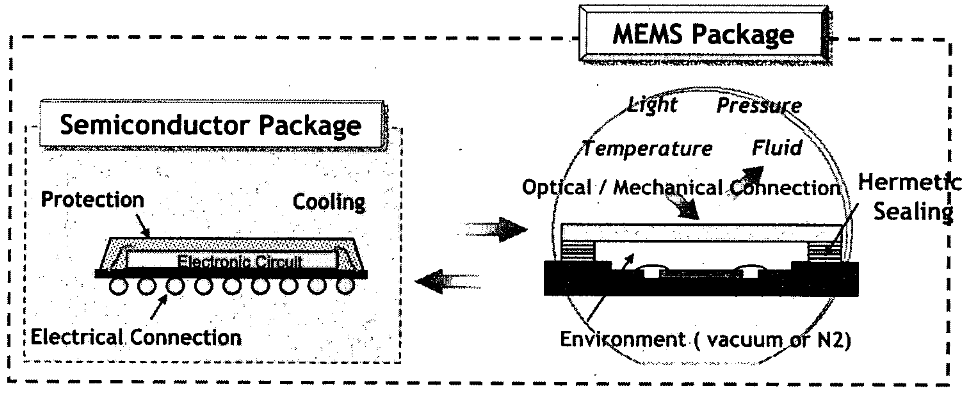
1

- ❑ **MEMS Packaging Issue**
- ❑ **SAIT WL-μP Trends**
- ❑ **Application**
  - **WLP for SAIT Gyroscope**
  - **WLP for RF-Device**

PACKAGING CENTER   Leading the Next

MEMS vs. IC Packaging

- Semiconductor Packaging :
  Electrical Connection, Heat dissipation, Mechanical Protection
- MEMS Package :
  Electrical, Optical and Mechanical Connection
  Hermetic or Vacuum Cavity for moving structure

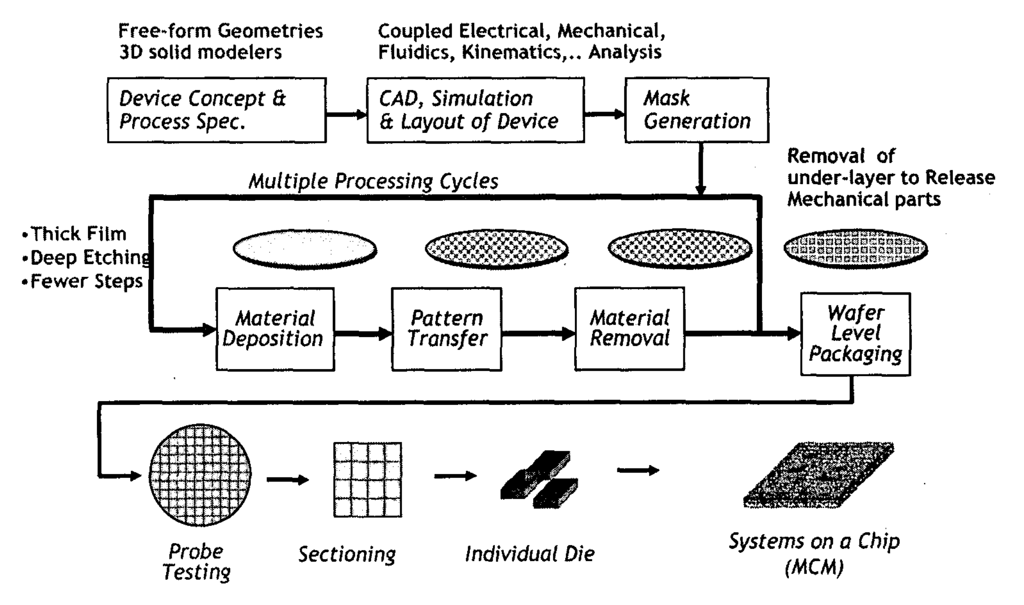


MEMS vs. IC Package

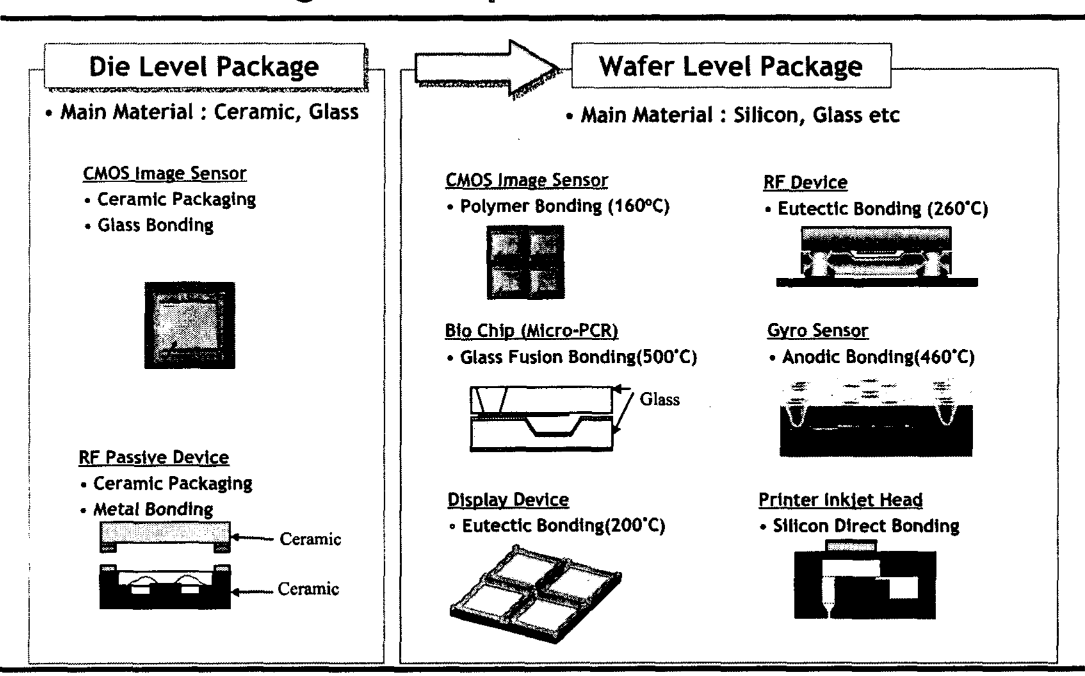
- MEMS PKG vs. Semiconductor PKG

		Semiconductor PKG	MEMS PKG
Applications		• High Volume : Telecommunications Consumer electronics	• Multiple application : Medical, Bio, Automobile Telecommunication, Display
Structure	Geometry	•2-Dimension •Quasi-hermetic	•3-Dimension •Hermetic /Vacuum Package
	Film Thickness CD Aspect Ratio Topology	• 1um • Sub micron • < 2:1 • < 1um	• 1 ~ several hundred um • > 1um • < 100:1 • < several hundred um
Technical Issue		• High speed • Small size • High density • Thermal dissipation • EMI	•Micro level Issue Stress-induced deformation, Stiction, Wear-out •Material Issue Chemical Reaction Biological Compatibility
Needs		• High Performance • Small Form-Factor • System Integration	▪ Low Cost ▪ Yield & Infrastructure ▪ Reliability ▪ Standardization

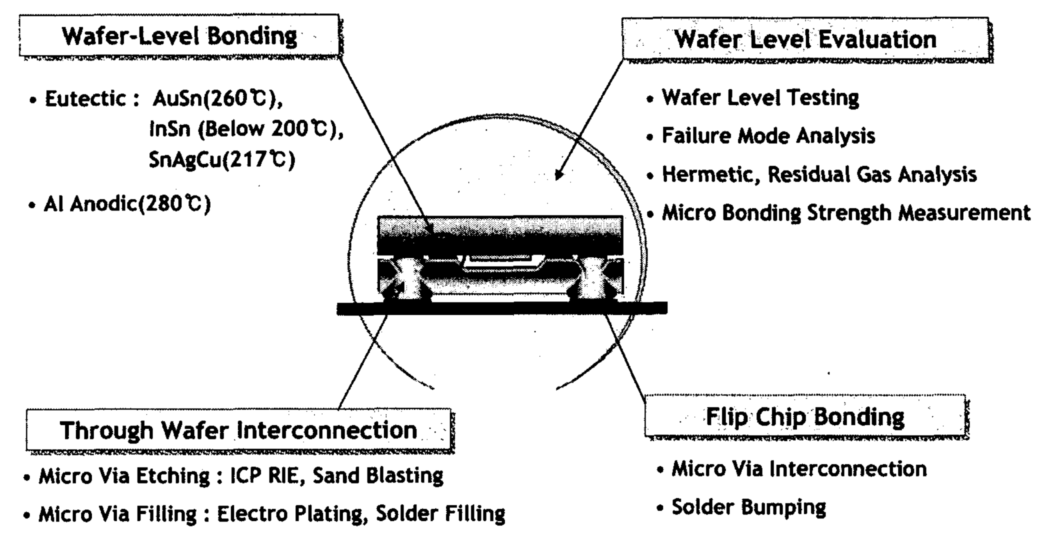
MEMS vs. IC Package



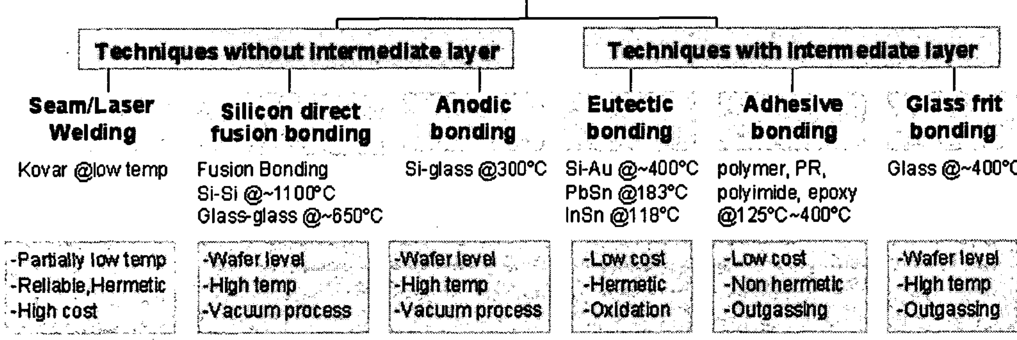
MEMS Package Development Trends of SAIT



Key Technology of WL-μP

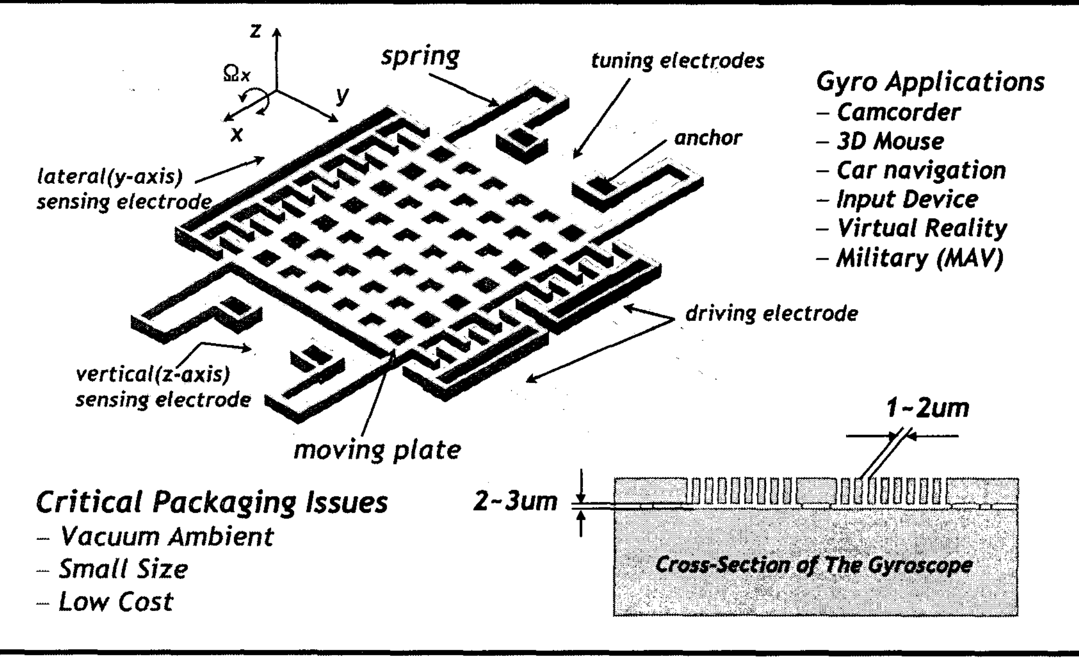


Wafer Bonding Technology



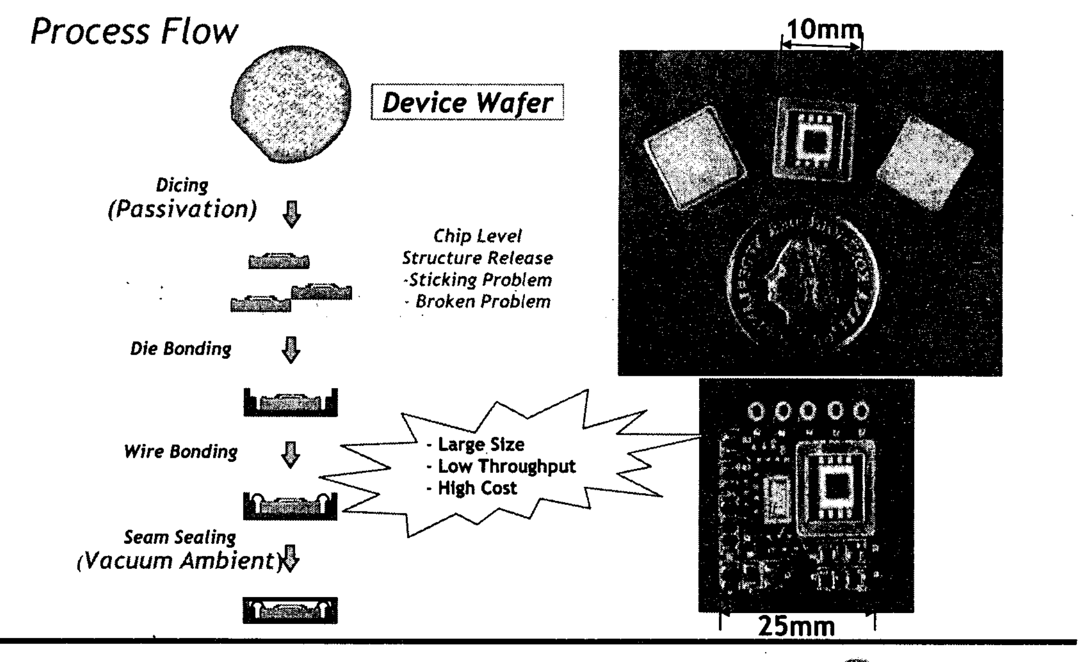
Application : SAIT Gyroscope PKG

MEMS Gyroscope Overview



Ceramic Packaged Gyroscope

10

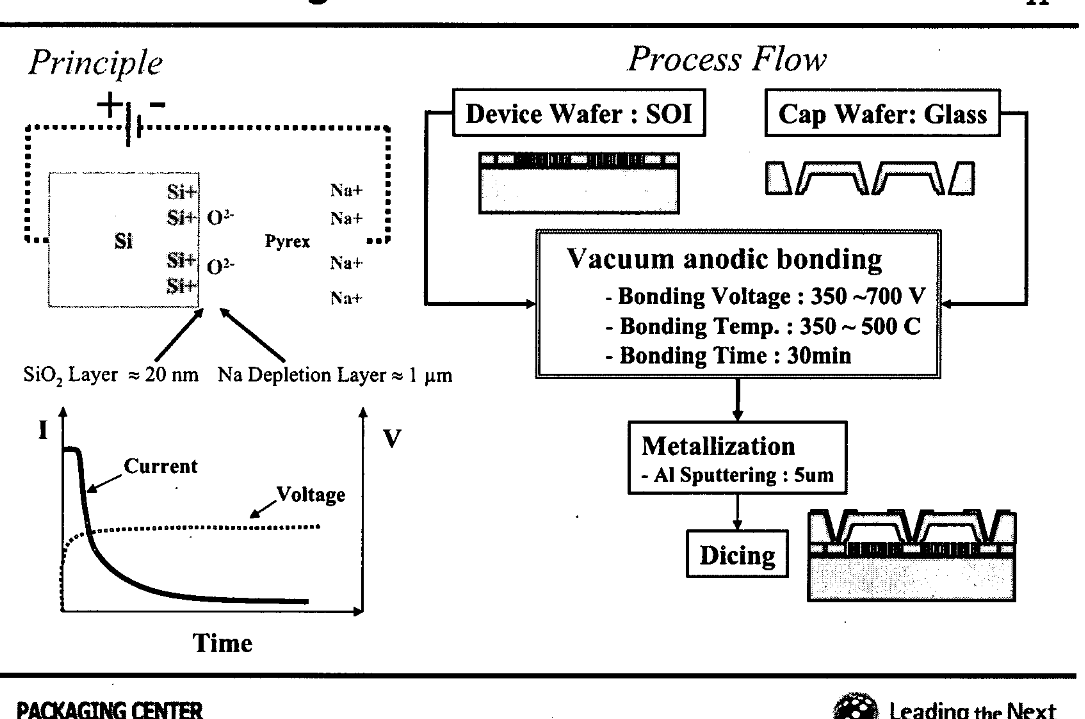


PACKAGING CENTER

Leading the Next

Anodic Bonding

11

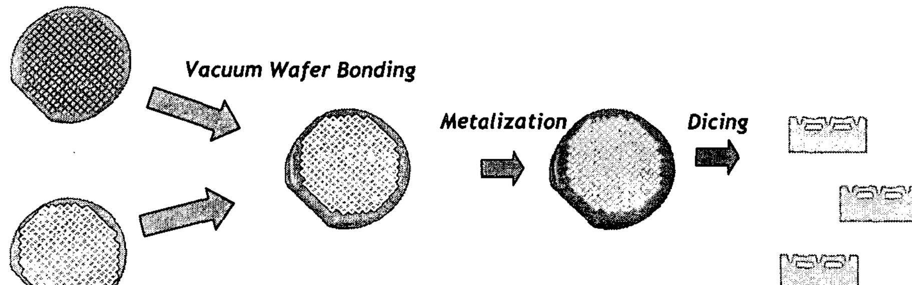


PACKAGING CENTER

Leading the Next

Wafer Level Vacuum Packaging

Device Wafer
-Moving Plate
- Wafer Level Structure Release

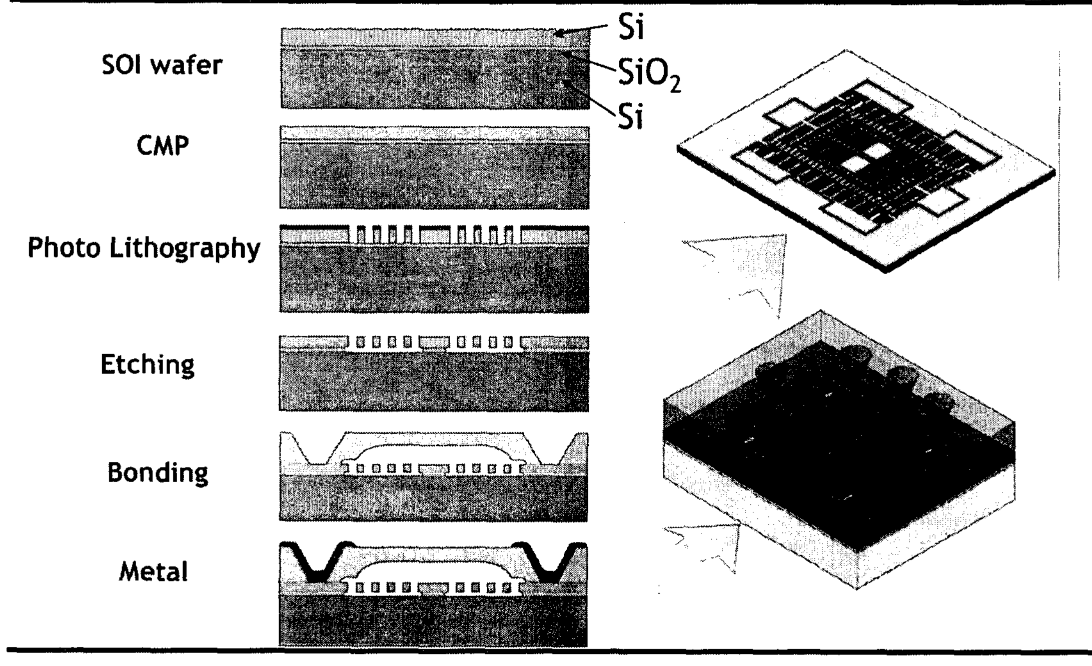


Cap Wafer
-Via hole
-Cavity

Bonded Wafer
-Eutectic Bonding
-Anodic Bonding

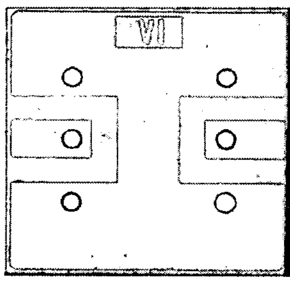
Gyro Chip Package

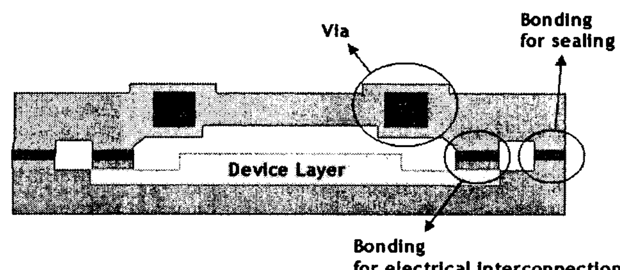
Fabrication Process



Application : RF-Device PKG

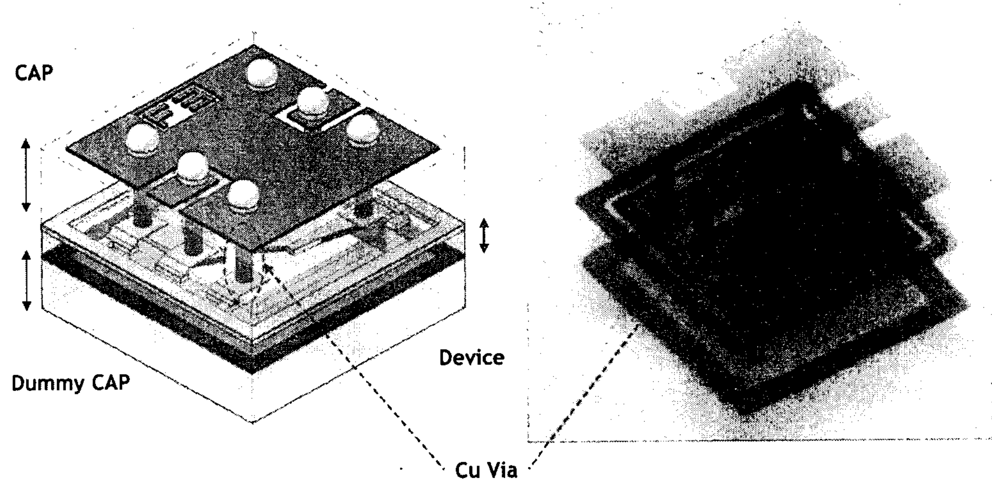
Representative SAIT RF-Device WLP



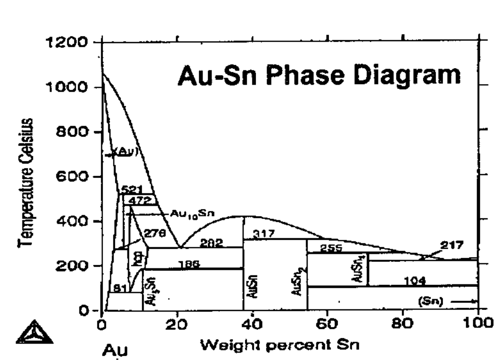


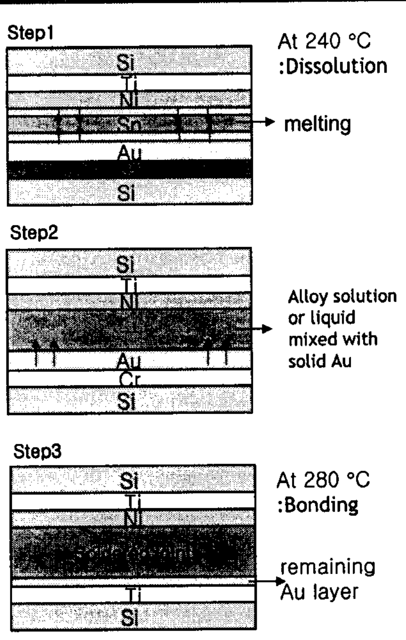
- Package size : 1 x 1 x 1 mm, 2.5 x 2.5 x 1 mm
- The number of via : 6 ~ 20
- Via diameter : 40 ~ 80 um
- Wafer bonding : 2 or 3 wafers using Au/Sn Metal Layers

Schematics & X-Ray Inspection Image



Stable Flux-free Au-Sn Eutectic Bonding

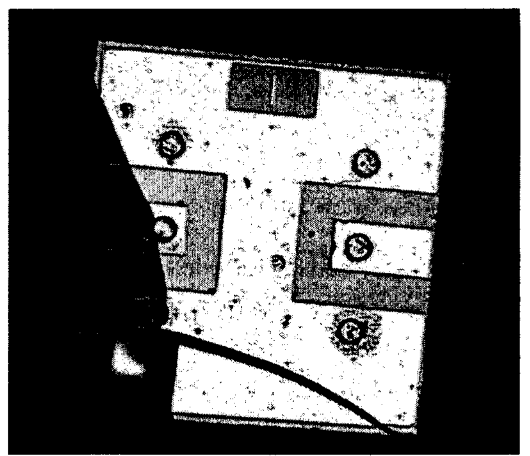




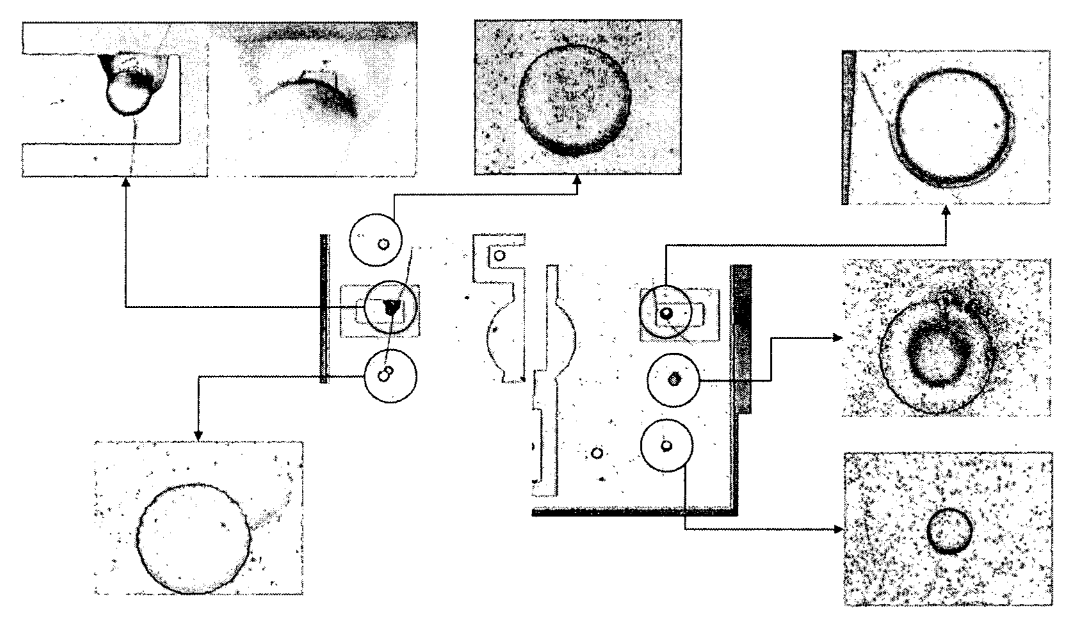
- ❑ Au-Sn Eutectic bonding
- ❑ Solid Liquid Interface Diffusion
  - Uniform bonding
    - Solder formation using e-beam
  - Remelting temp. above 280C
    - Stable bonding
    - Merit for process design

Reliability Tests

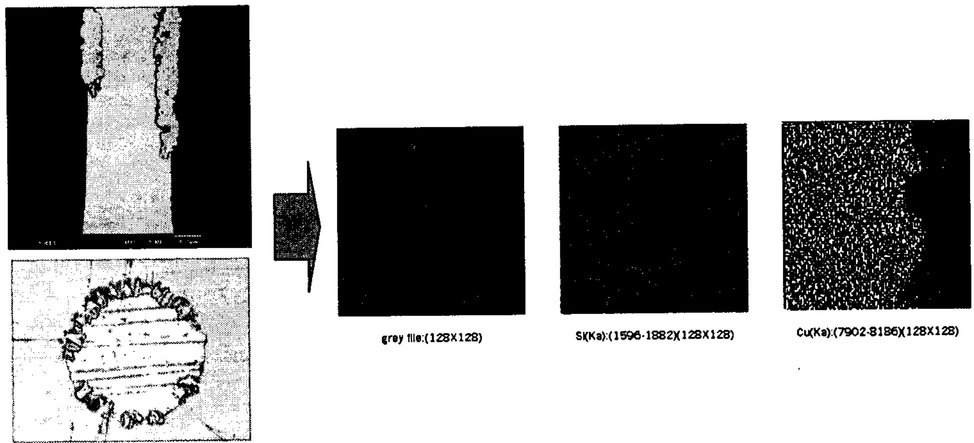
번호	테스트명	실험 조건	측정 조건
1	열 cycle	-40℃/+85℃, 5 min transition, 2 Hours 유지, 15 cycles	@상온상습
2	고온고습방치	+85℃, 85% RH, 120 Hrs	2시간 방치 후 @상온상습
3	PCT	+121℃, 100% RH, 2 atm, 48 Hrs	@상온상습
4	고온고습동작	+50℃, 95% RH, 48 Hrs	@+50℃, 95% RH
5	저온동작	-30℃, 48 Hrs	@-30℃
6	낙하	150g Jig 152cm 19회(6면체 각 면당 3회 + 1회) 120cm 12회(6면체 각 면당 2회)	@상온상습
7	ESD	HBM, Class 1A(250V) 이상, 단자별 1회	@상온상습
8	Reflow	max 245℃ (기존 max 230±5 ℃, 10초)	@상온상습



Mechanical Failure after Reliability Test

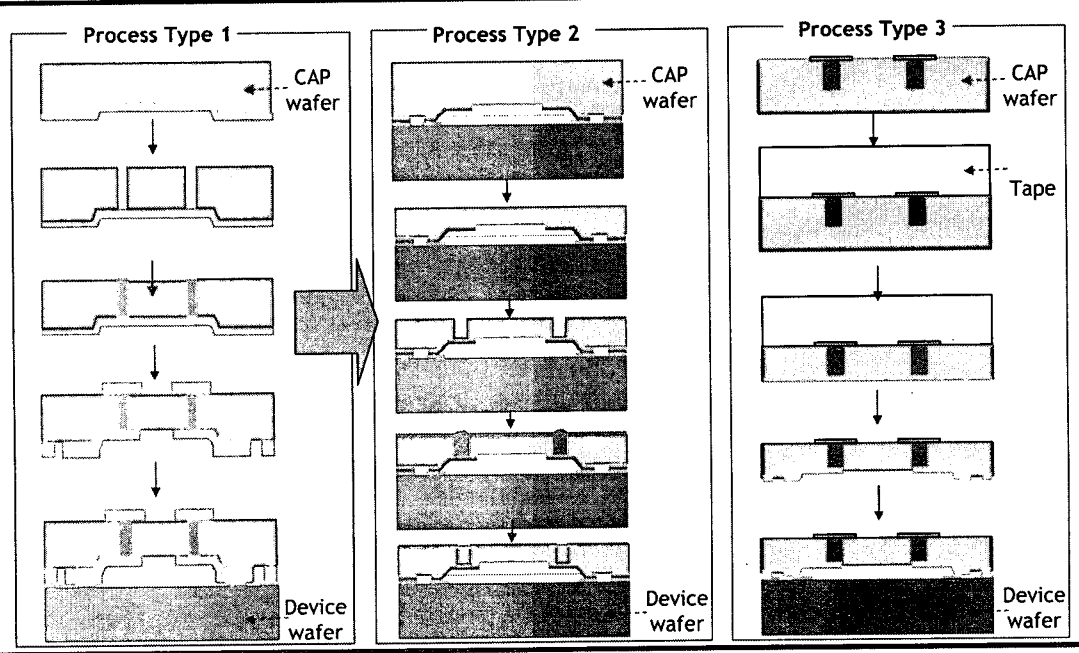


Interface Analysis (Element Scanning)



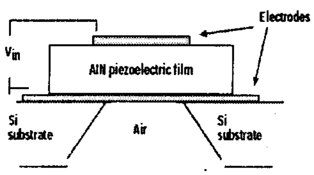
- Left are the distribution of Si and Cu for a cluster.
- The red one is element Si and the yellow one is the Cu.
- The distribution indicates the cluster is composed by Si and Cu.

Design Change

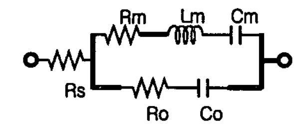


RF-Resonator for Reliability Test

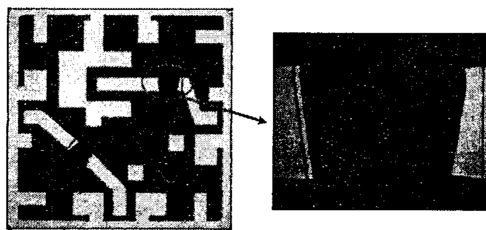
❑ Film Bulk Acoustic Resonator (FBAR)

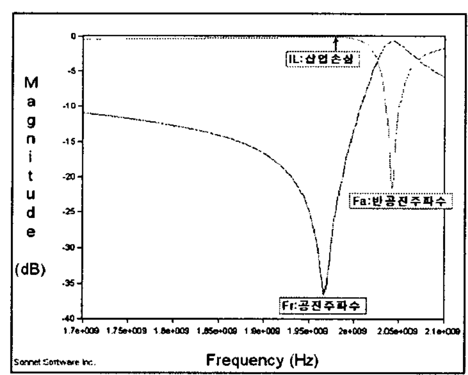


- Schematics

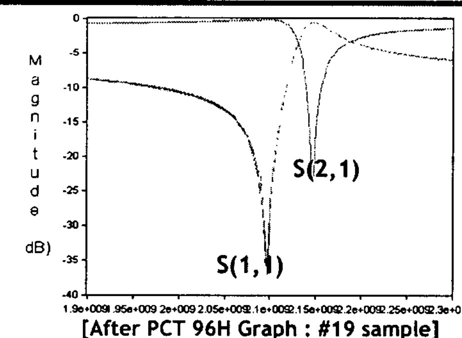


- Equivalent Circuit Model





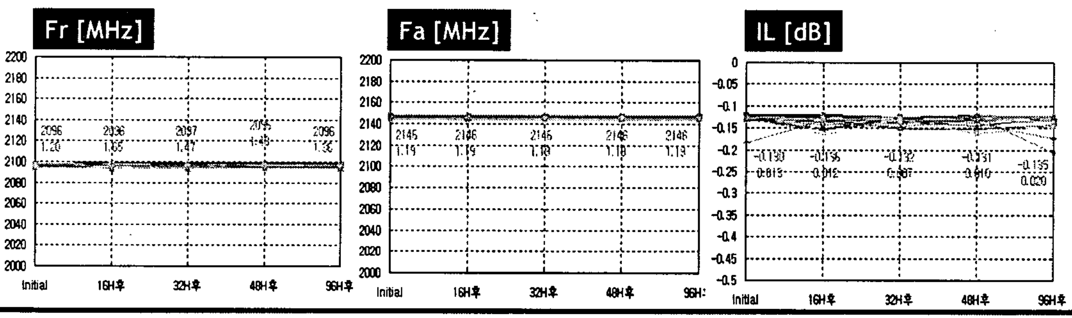
Pressure Cooker Test (121℃ / 100%RH / 2atm)



[After PCT 96H Graph : #19 sample]

[After PCT 96H]

	Fr(MHz)	Fa(MHz)	IL(dB)
Mean	0.57	0.00	-0.005
Stdev	1.08	0.00	0.024
Max	4	0.00	0.048
Min	-1	0.00	-0.080



Summary of Reliability Test

[Table1. NRES#03 Sample Reliability Test Result]

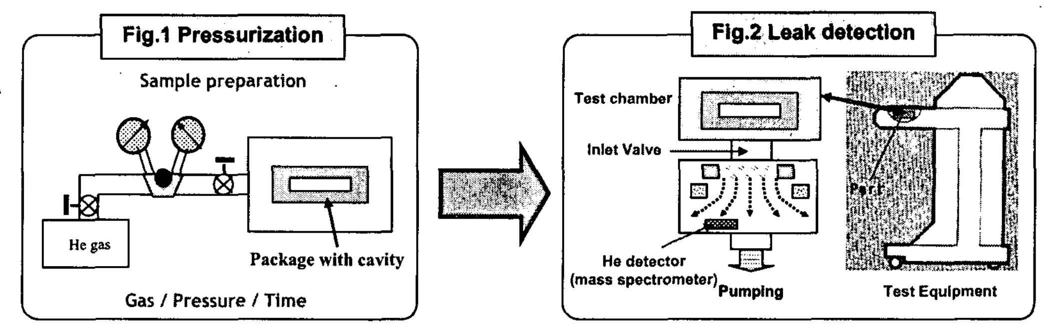
Item	Condition	Duration	RF-Performance			Result
			Fa (MHz)	Fr (MHz)	IL (dB)	
1. PCT	121℃/100%RH/2atm	96 Hours	0.57	0.00	-0.005	Pass
2. Humidity Test	85℃/85%RH	120 Hours	0.48	0.10	0.010	Pass
3. High Temp. storage	125℃	120 Hours	0.24	0.00	0.010	Pass
4. Temp. Cycle	-40℃/85℃ 2 Hours/Cycle	30 Cycles	0.38	0.05	0.010	Pass

Residual Gas Analysis

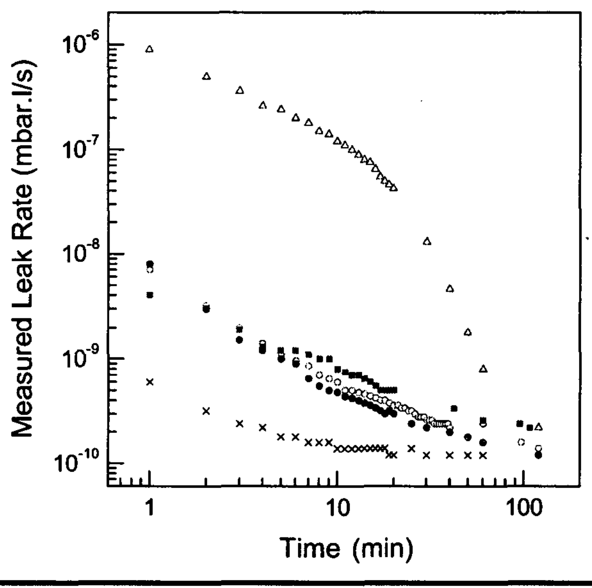
Gas	Gas detected after breaking the packages					
	Before the tests		After PCT 96 Hours		85/85 120 Hours	
	μl	%	μl	%	μl	%
H_2O	0.02	2.2	0.02	2.0	0.02	2.5
N_2	0.91	97.8	1.12	98.0	0.90	97.5
Total	0.93	100.0	1.14	100.0	0.93	100.0

Helium Leak Test

- *1st Step - Pressurization :*
  The object(e.g. package with cavity) is placed in a vessel containing helium under pressure (Fig. 1). Helium penetrates the object if it has a leak.
- *2nd Step - Leak detection :*
  The object is then removed from vessel and placed in the test chamber which is connected to the detector (Fig.2). The helium escapes from the object through the leak and produces a signal.



Measured Leak Rate



- × Without sample
- • Bare Wafer (25.1mmx25.1mm)
- ○ WLP without via
- △ WLP with back-seed EP via
- ▪ WLP with damascene EP via

Batch test using multiple packages
Bombing Pressure : 5 atm

Concluding Remarks

- **Driven Technologies in MEMS Packaging – WLP**
- **Key Technology for WLP**
  - **Wafer-Level Bonding Technology**
  - **Through Wafer Interconnection Technology**
  - **Hermeticity Evaluation Technology**
- **Suitable for MEMS - Low Temperature Bonding**