Wafer Level Package Technology Applied to System Packaging

Takeshi Wakabayashi

(Casio Computer/Japan)

The 4th International Symposium on Microelectronics and Packaging
COEX Convention Center, Seoul
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Wafer Level Package Technology Applied to System Packaging

"WLP and EWLP®" as a new "JISSO" Technology

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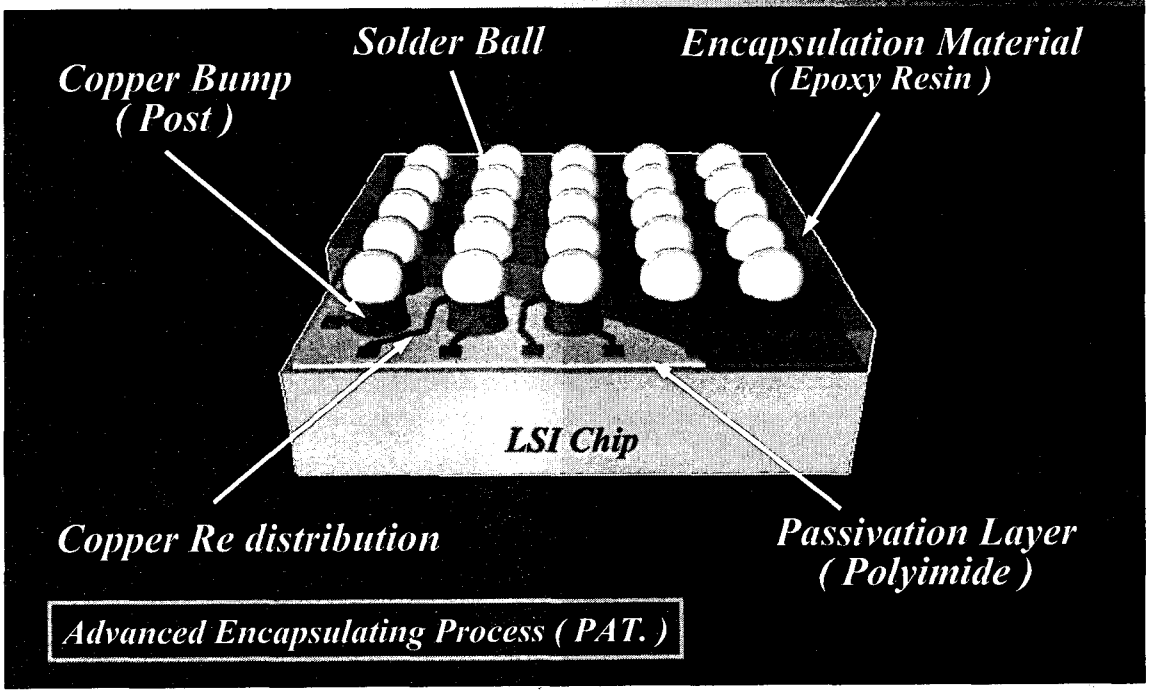
CASIO

Basic Structure of WLP

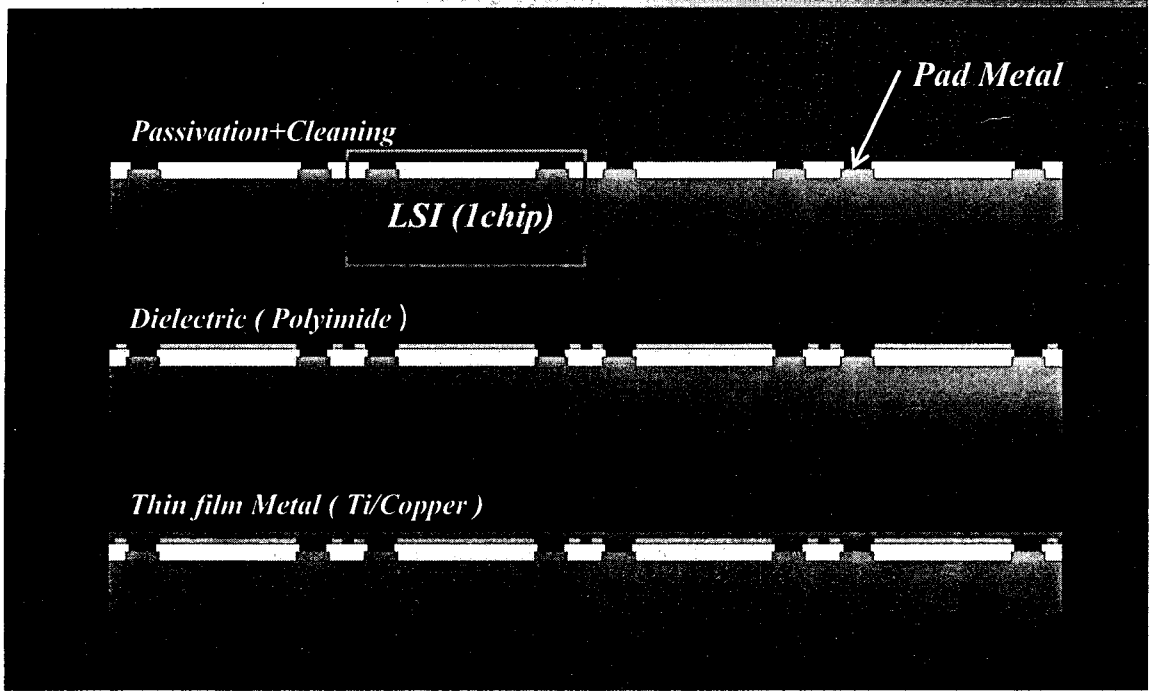


Advanced Encapsulating Process (PAT.)

CASIO.

WLP Process Flow "Thin film"

Page 5



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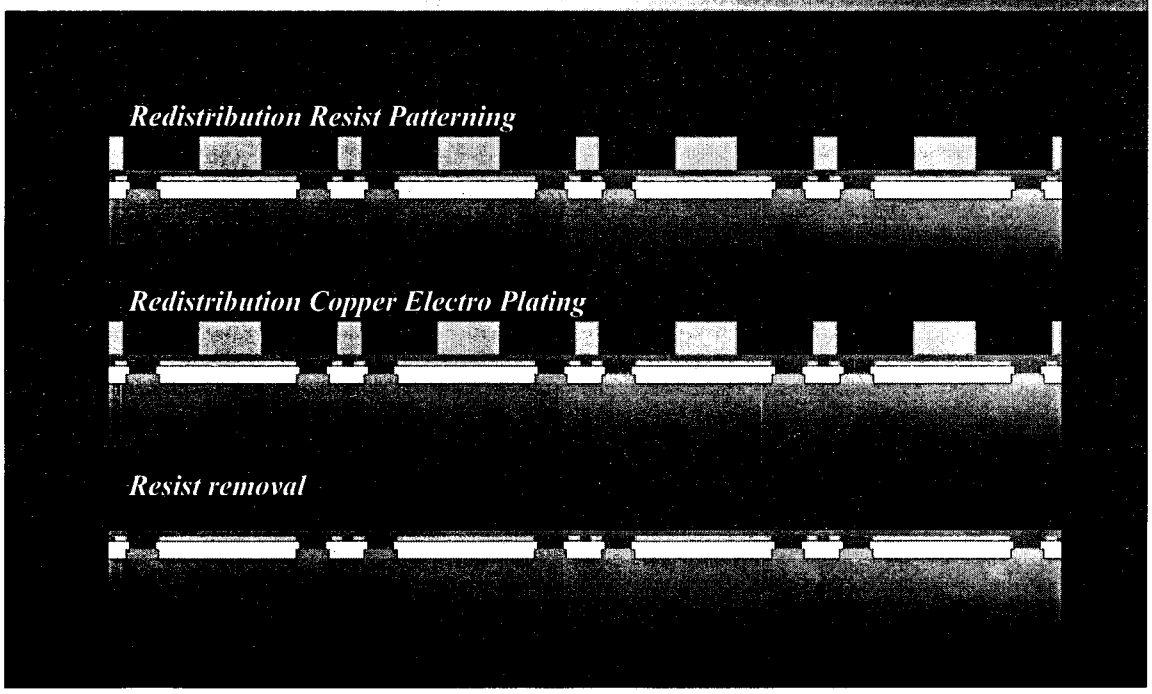
WLP Process Flow "Re distribution"

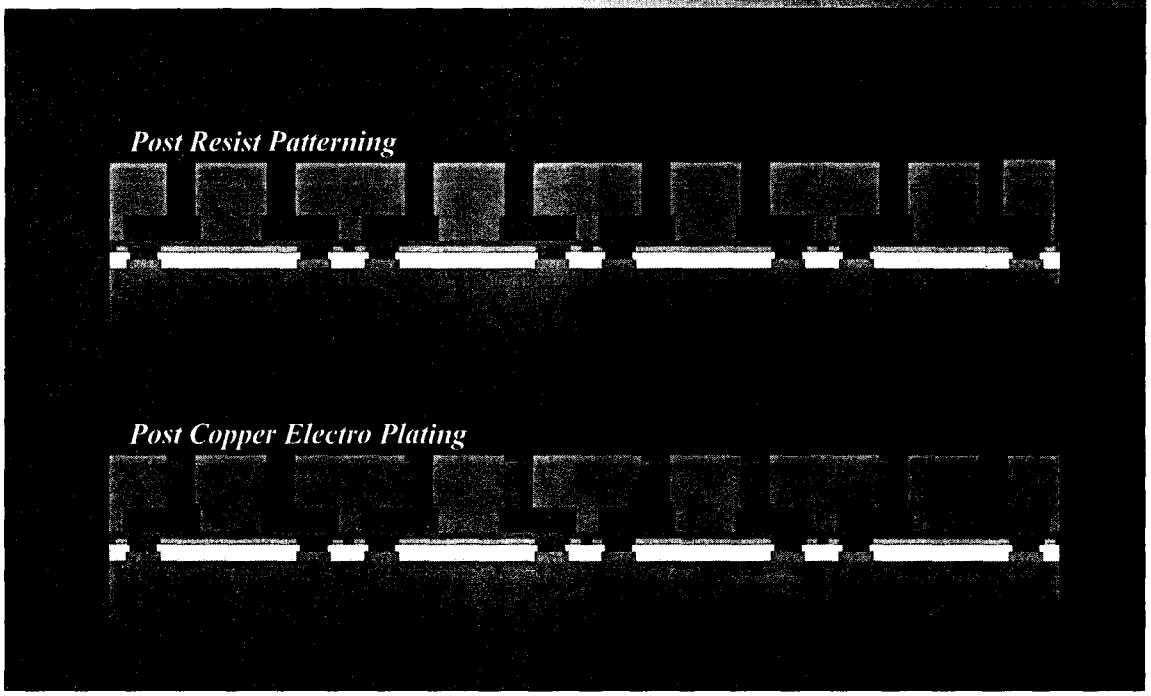
Page 6



CASIO.

WLP Process Flow "Copper Post"

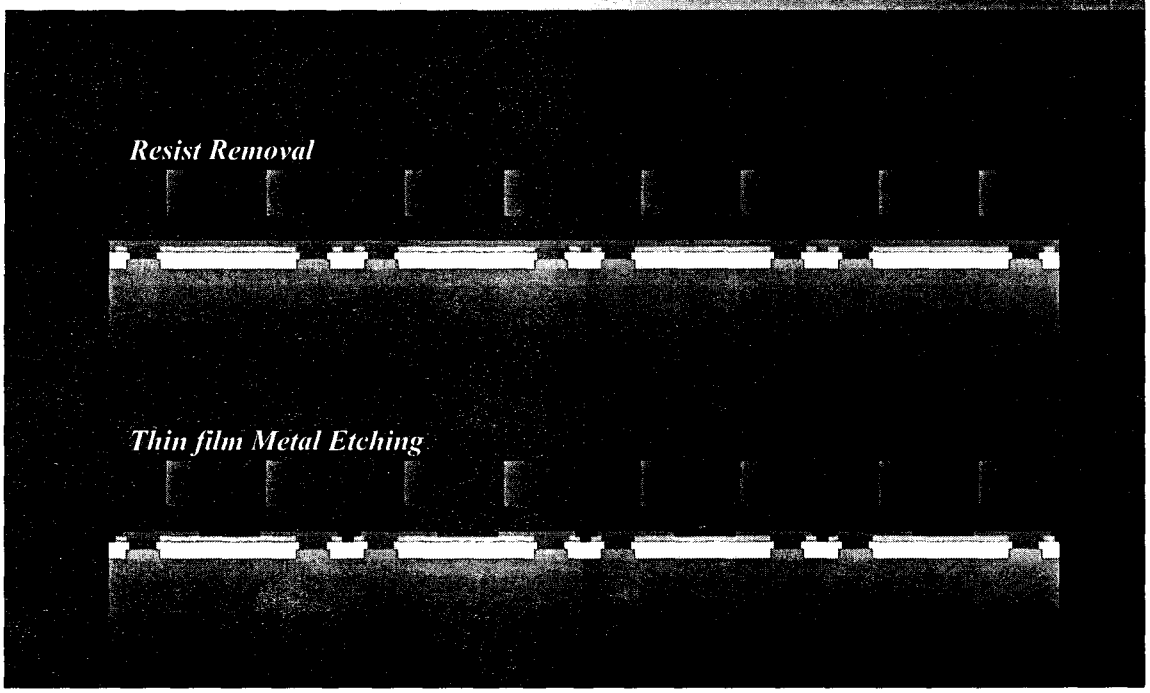
Page 7



CASIO.

WLP Process Flow "Copper Post"

Page 8



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WLP Process Flow "Encapsulation"

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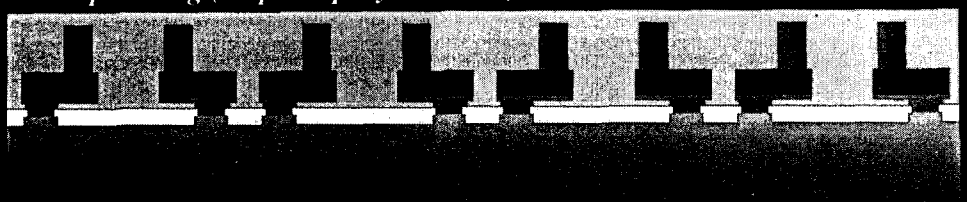
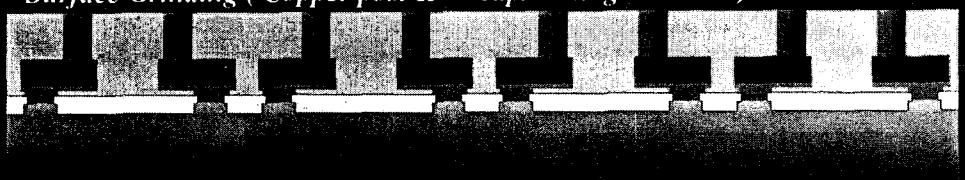
Encapsulating (Liquid Epoxy Material)



Surface Grinding (Copper post & Encapsulating Material)



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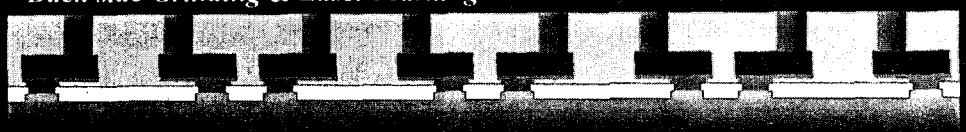
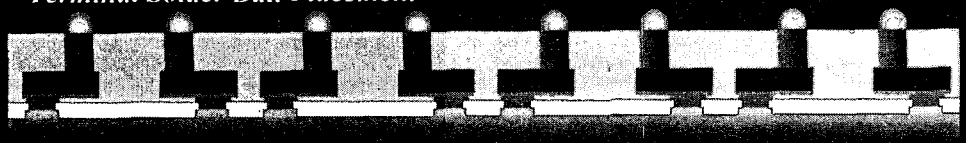
WLP Process Flow "Solder Ball & Dicing"

Page 10

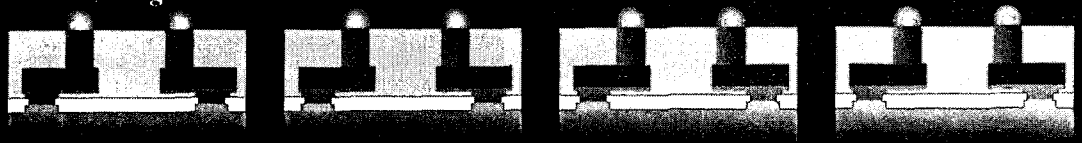
Back side Grinding & Laser Marking



Terminal Solder Ball Placement



Dicing



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Solder Ball Placement Technology

- Transfer using Vacuum Plate
- Ball drop using Metal Mask
- Ball drop in Liquid Condition
  - Direct Drop using Temp. Mask
  - Transfer

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Reliability Data

Moisture Sensitivity	JEDEC Level 1@260℃ 85℃/85%RH/168hours, 10 times
Temp Cycle	-65℃/+150℃, 2000 cycles
High Temp Storage	150℃, 2000 hours
Temp Humidity Bias	85℃/85%RH/10V,L/S=10/10um, 2000 hours
HAST	130℃/85%RH/10V,L/S=10/10um, 168 hours
PCT	121℃/2atm, 500 hours
Temp Cycle on PCB	-25℃/+125℃, 900 cycles (7x7 array, 0.5mmpitch, 0.1% failure)

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Advantages of CASIO's WLP

Page 14

- Basic Characteristic WLP
  - High Yield, Performance and Reliability
  - High Productivity and Low Cost
  - Easy to use
  - 300mm Wafer Processing
  - Advanced Encapsulating Process (US PAT.) & Material
- Low Cost Solution for Test Process
  - Handling Cost
  - Wafer Level B/I
- EWLP® Technology Solution
  - High Performance Module
- Stress Buffer (Leading-Edge Semiconductor)
  - 90nm, 65nm, 45nm
  - Low/High-k Materials

Perfect Protection
SMT Compatible
High Productivity

Reliable Low Cost Contact
Protect against Mechanical Damage

High Performance System
Solder Less Module

High Performance Device Solution

CASIO.

WLP Structure & Process (Simple Ball vs. Copper Post)

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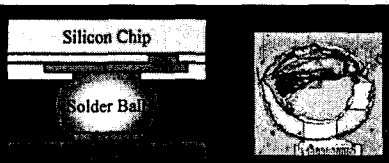
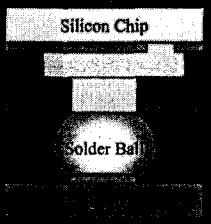




1. First dielectric layer
2. Photo pattern
3. Sputter UBM
4. Photo resist pattern
5. Etch to form trace and pad
6. Second dielectric layer
7. Photo pattern
8. Attach pre-formed solder ball
9. Reflow solder

1. First dielectric layer
2. Photo pattern
3. Sputter UBM
4. Photo resist pattern
5. Copper electroplate
6. Resist pattern
7. Copper electroplate
8. Etch UBM
9. Encapsulate
10. Grind
11. Attach pre-formed solder ball
12. Reflow solder

Mechanical stress from ?
- ✓ Package probe test, B/I
- ✓ Handling, Taping
- ✓ SMT Pick and Place
- ✓ Under fill, Cure
- ✓ Case Assembly
- ✓ Product in Use
  - Operation
  - Vibration
  - Drop

High current distribute

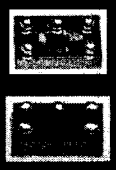
Mechanical protect

CASIO

Shock Resistant Evaluation Result (Customer Test)

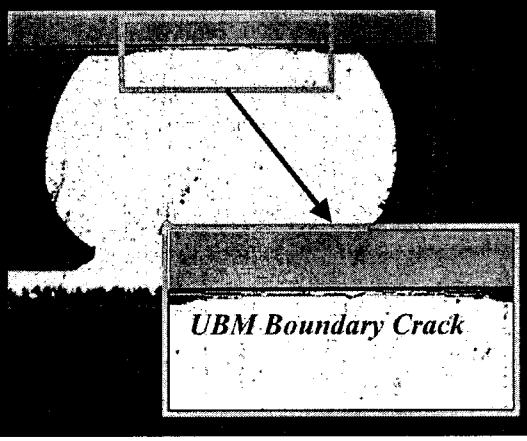
- Shock (PCB Assembly without Underfill): 24,000 G
- No. of Sample — Open Failure
  - Solder Ball Type : 10 — 4
  - Casio's WLP : 10 — 0

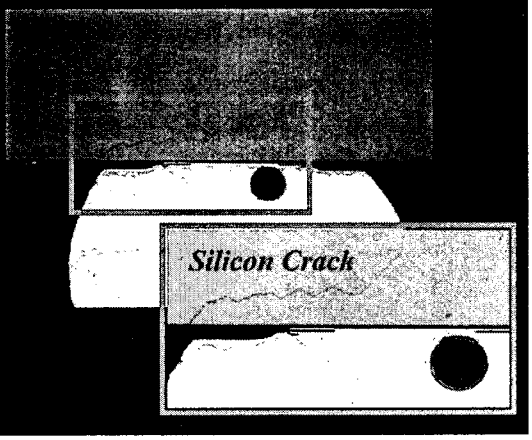
(Same Size Daisy chain Sample)



SN**********

1.4 x 0.9 mm
0.5 mm pitch
5 Balls





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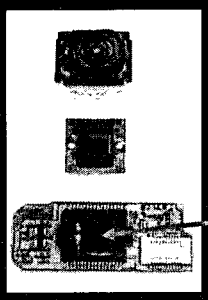
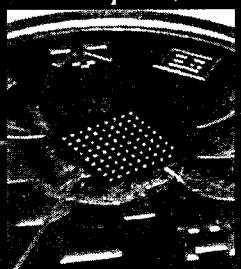
CMOS Camera Module in Cellular

Digital Signal Processor
WLP (4.24mm x 4.24mm)
0.4 mm pitch, 80 balls

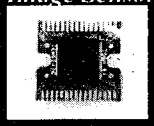


Module Structure



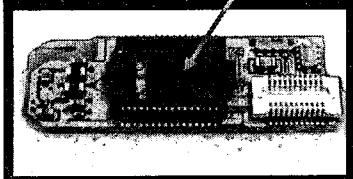
CMOS Image Sensor

Lenz Unit

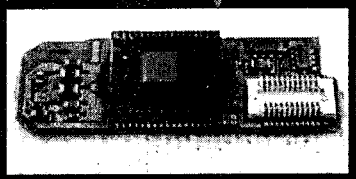


Back Side

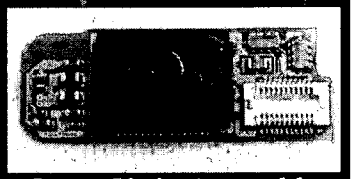
Back Side



DSP Assembly



CMOS Sensor Assembly



Lenz Unit Assembly

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A5406CA / au by CASIO

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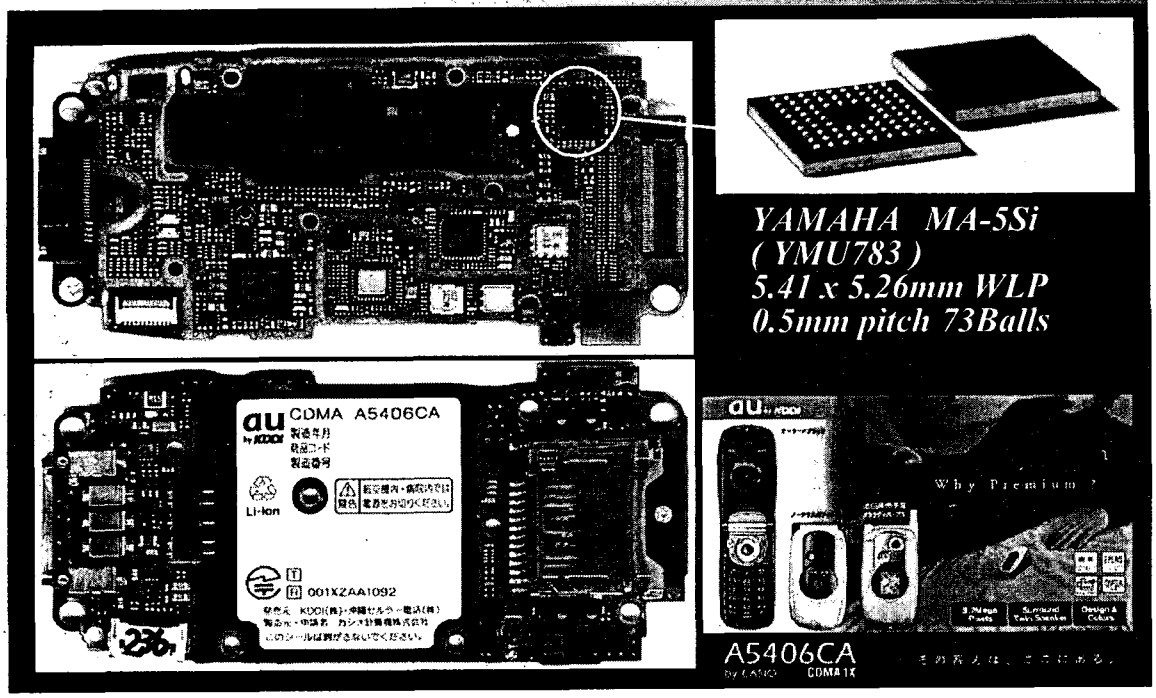

YAMAHA MA-5Si
(YMU783)
5.41 x 5.26mm WLP
0.5mm pitch 73Balls

CASIO.

DSC Application : CASIO "Exilim Z4"

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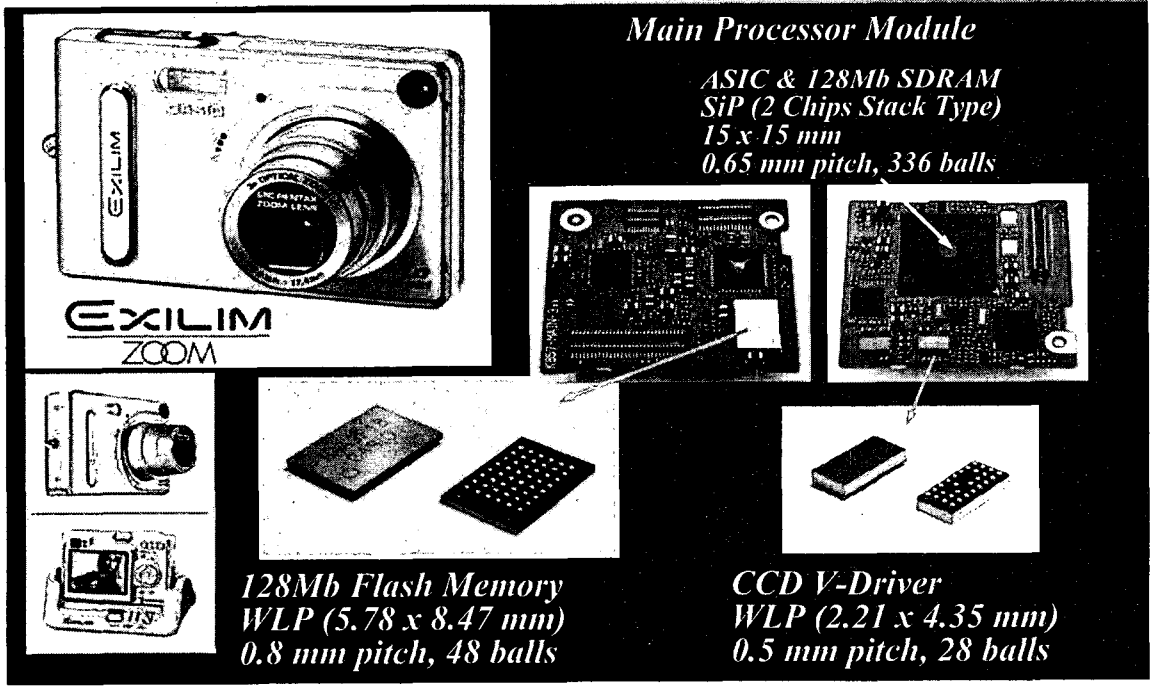

Main Processor Module

ASIC & 128Mb SDRAM
SiP (2 Chips Stack Type)
15 x 15 mm
0.65 mm pitch, 336 balls

128Mb Flash Memory
WLP (5.78 x 8.47 mm)
0.8 mm pitch, 48 balls

CCD V-Driver
WLP (2.21 x 4.35 mm)
0.5 mm pitch, 28 balls

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WLP Technology (Post Passivation Process)

- Function of Electroplated Copper Line
  - Re-distribution Terminal
  - Inductor, Transformer
  - High Electric Current Line
  - High Speed Signal Line
  - Antenna
- Thick Encapsulated Layer for Protection
  - Protection against Mechanical Stress
  - Embed into Organic Substrate
  - Stress Buffer for Low-k Materials

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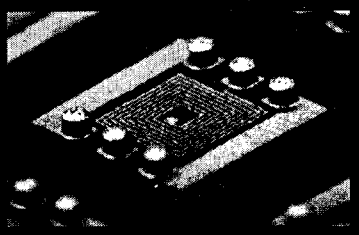
II Inductor and Transformer

- Structure and Technology
  - Spiral Inductor by Electroplated Copper (Thickness: 5um-20um)
  - 1 layer or 2 layers structure



- Purpose
  - Higher Q-factor than Thin Film Integrated Inductor
  - Smaller than Individual Inductor Device
- Application
  - Integration in RF chip
  - Power Device (DC-DC Converter)
- CASIO's Patent

CASIO.

Ⅳ High Speed Signal Line

- Structure and Technology
  - High Speed Signal Line by Electroplated Copper (Thickness: 5um-10um)
  - 1 layer or 2layers structure : Depend on Net Numbers
- Purpose
  - High Speed Line (Clock, Signal)
  - Wide Band Bus Line
  - Power and Ground Line (Reduce Voltage Noise)
  - Global Electrical Connection between IP Block in Large System Chip

Super Connect

- Application
  - High Performance System LSI, CPU, GPU

CASIO.

Ⅶ Stress Buffer for Low-k Materials

- Structure and Technology
  - Electroplated Copper Post and Encapsulation by Epoxy Material with Filler
  - Thickness: 30-90um
  - Re-distribution
  - Thickness: 5-20um
- Purpose
  - Low-k, High-k Material Protection against Mechanical Stress
  - Mechanical, Thermal Change
    - Test Contact
    - General Reflow Process in Flip Chip Assembly
- Application
  - The Leading Edge Semiconductor Chip Assembly

CASIO.

Die Size, Number of Balls and Ball Pitch

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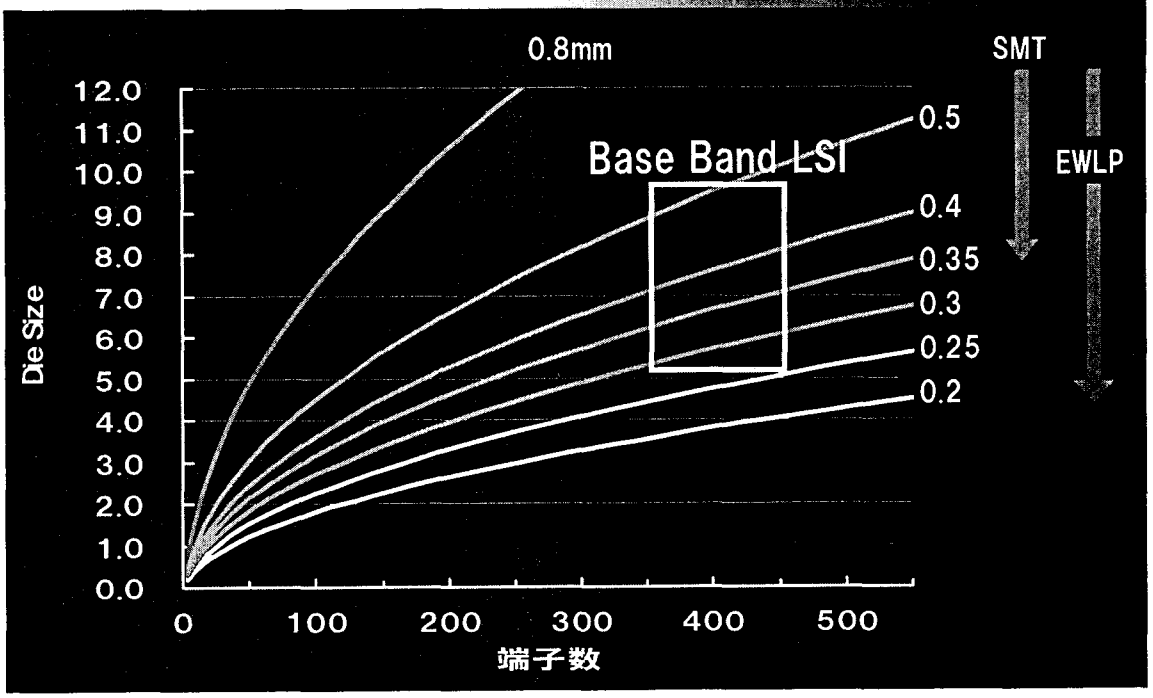

CASIO.

Basic Structure of WLP for "EWLP®"

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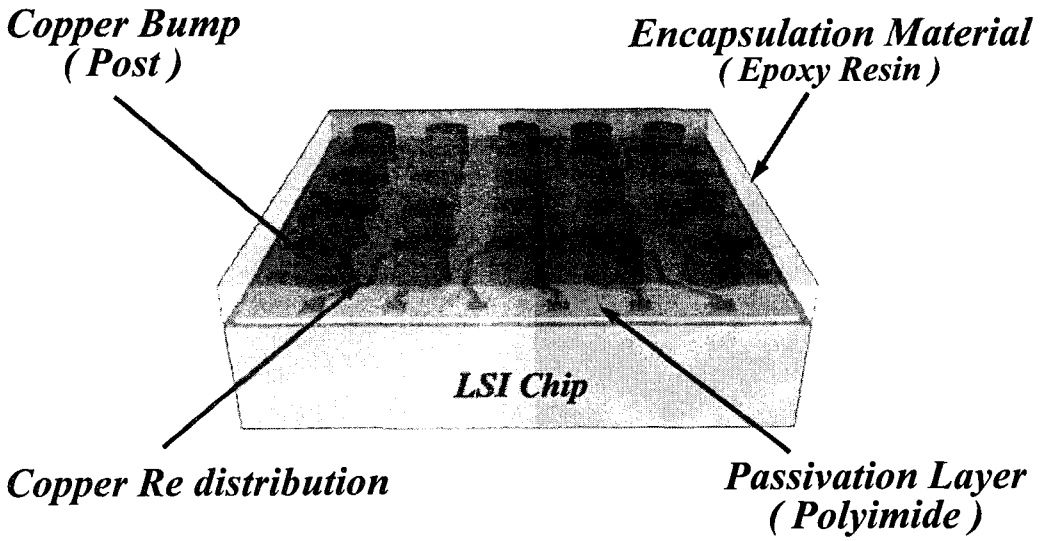
No Solder Ball !



CASIO.

EWLP® Process Concept

Preparing WLP Devices

WLP Placement

Laminate (Hot press Process)

Laser Via Drilling

CASIO.

EWLP® Process Concept

Subtractive Process

Electro less Copper Plating

Electro Copper Plating

Copper Pattern Photolithography

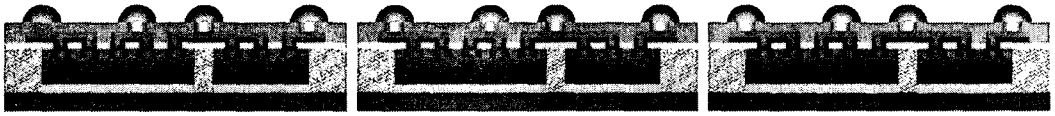
CASIO.

EWLP® Process Concept

Solder Resist

Terminal Finish (Solder Ball Placement)

Dicing



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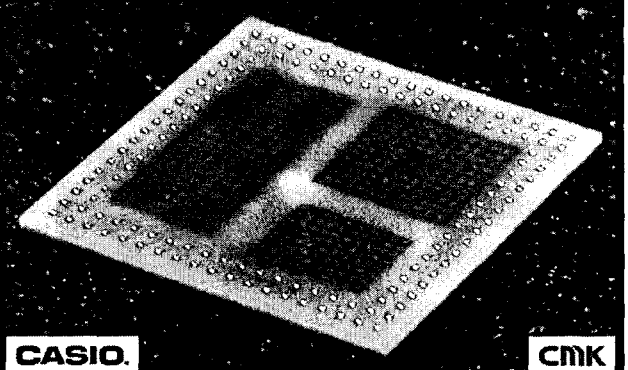
EWLP® Module (Multi WLP)

- *High Performance Digital Processor Module*
  - *High Speed Signal*
  - *Bus Line*
- *Equivalent to System LSI*
  - *Small Form Factor*
  - *Plane Structure*
- *Copper Interconnect*
  - *High Performance*
  - *Solder Free*

Large System Module Structure

EWLP® Module (EWLP® Structure)



CASIO. CMK

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Prototype Sample

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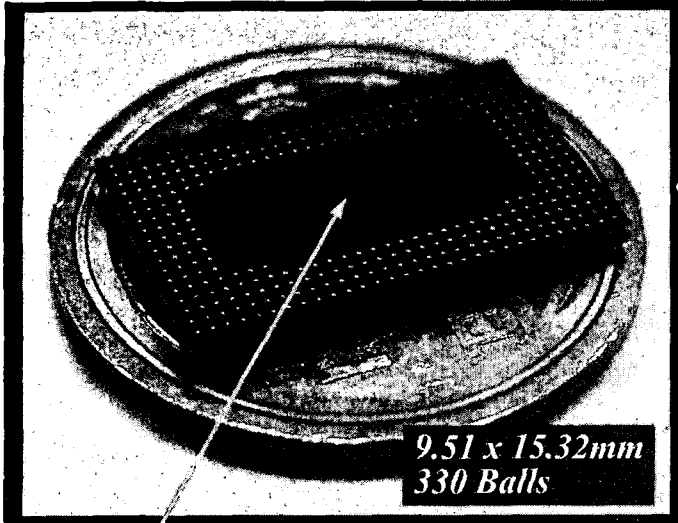
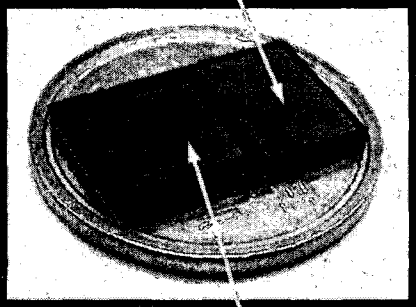


128 M bit Flash Memory
8.51 x 5.75mm, 48 Balls WLP



System LSI
5.75 x 5.75 mm, 0.2 mm pitch, 312Pad WLP

Embedded WLP

128 M bit Mobile DRAM
7.02 x 7.09 mm, 54 Balls, WLP

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EWLP, WLP & Passive Integrated Module

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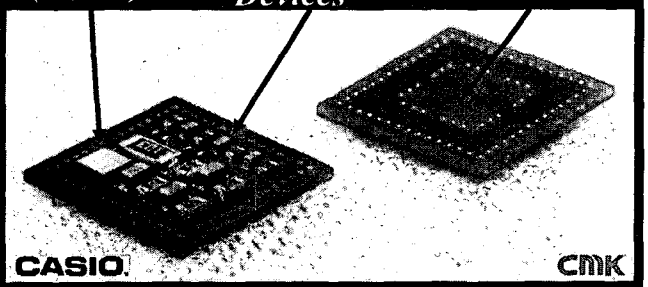
Passives are mounted on EWLP Terminal Side or the other Side

- *By Conventional SMT*
- *EWLP®, WLP and Passive*
- *Flexibility of Mounting Passives Devices*
  - *Analog, RF*
- *RF Module Application*
  - *GSM, Cdma*
  - *Bluetooth, RF LAN*
  - *GPS*
  - *Digital TV Tuner*

RF Module Mechanical Sample

WLP (SMT) *Passive Devices* *EWLP*



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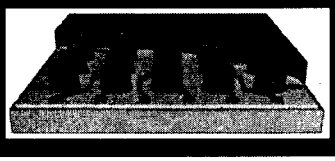
Bare Die vs. WLP for Embedded Process

Bare Die Issue

- *KGD Issue (Good Die)*
- *Finer Pad Pitch*
- *Thin film Pad Material*
- *Difficulty of PCB Process Technology*
- *Imperfect Reliability*

Advantages of WLP Embedded

- *+ Easy Test and Wafer Level B/I*
- *+ Design Flexibility from WLP Re-distribution*
- *+ Copper Terminal Finish*
- *+ Perfect Protection*
- *+ High Reliability*



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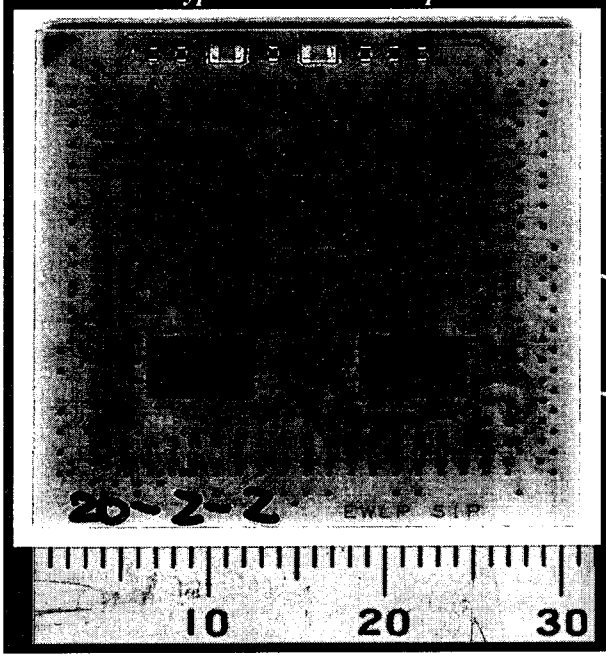
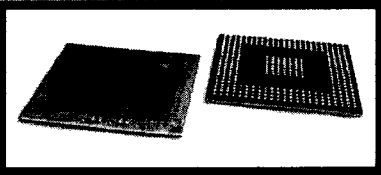
CPU EWLP® Module (RENESAS, CASIO, CMK)

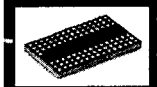
Prototype Evaluation Sample





CPU(SH4/200MHz)/WLP
6.43 x 6.43 mm
246+77 copper pads
0.2, 0.5 mm pitch

64Mbit SDRAM/WLP
- 3.876 x 6.15 mm
- 91 copper pads (58)
- 0.4 mm pitch



Bus Speed : 100 MHz
EWLP® Module Board
- Size : 31 x 31 mm
- Layer : 2-2-2 Build Up
- L/S : 35/35 --- 50/50 um

CASIO.

FCBGA, WLPBGA & EWLP®

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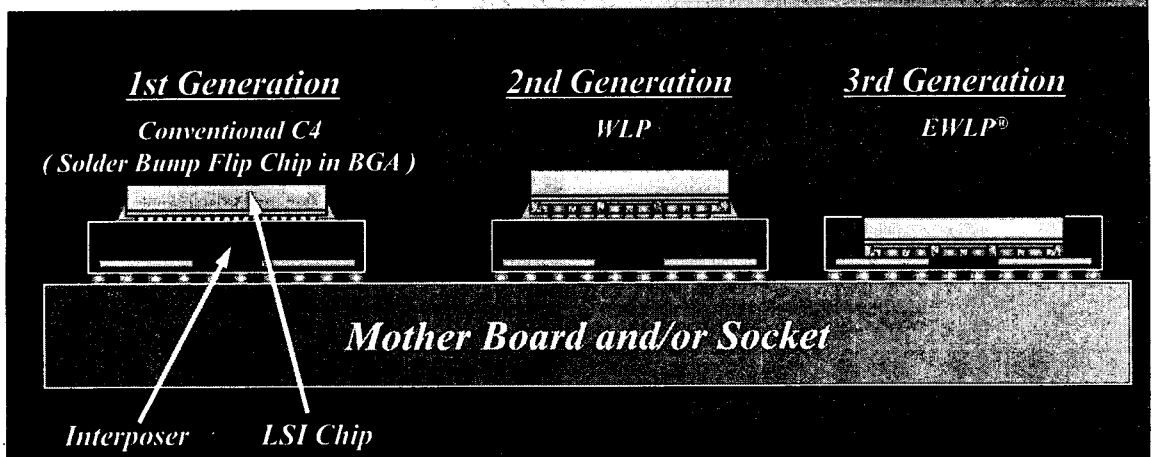

- Fine Solder Bump
- Fine Pitch Interconnect
- T/C Reliability
- Low-k Protection
- Fine Pitch Interposer

WLP Technology Solution
for High Performance
Device

CASIO.

Conclusion (CASIO's WLP & EWLP® Technology)

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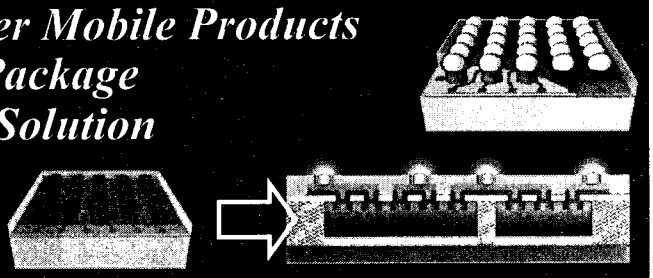
- Package for Consumer Mobile Products
  - Smaller, Thinner Package
  - Advanced Module Solution



- EWLP® for High Performance Products
  - Copper Distribution on Chip
  - Low-k Packaging Solution
  - "Lead Free!"
    - Solder Less Interconnect for High Performance & Reliability