Packaging Technologies for Semiconductor Memories

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Packaging Technologies for Semiconductor Memory

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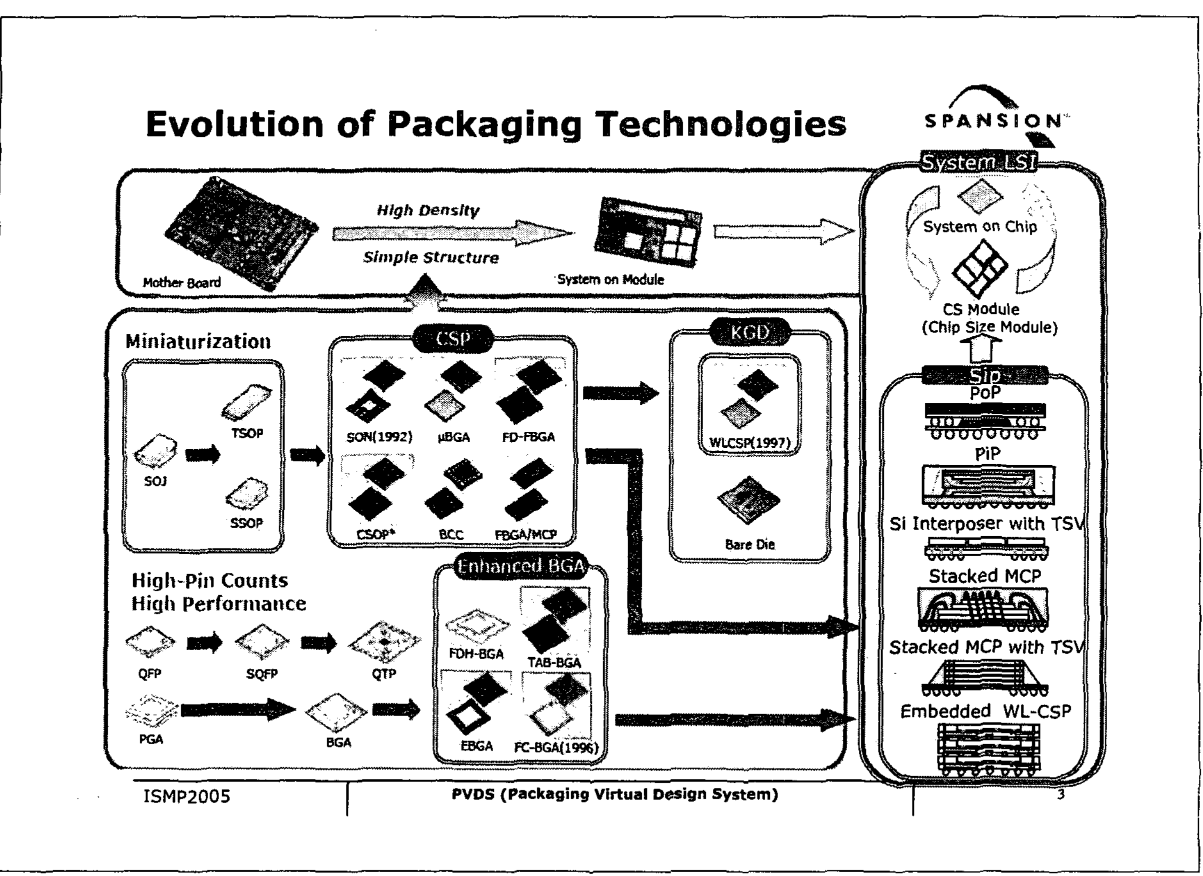
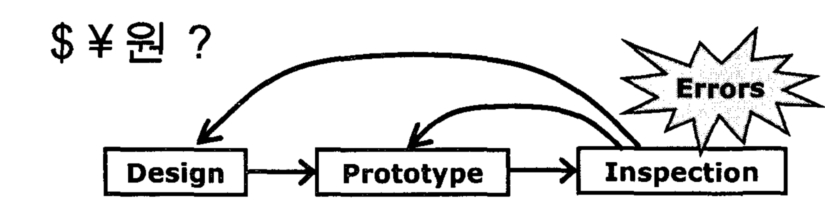


Strategy of "Yoshinoya"

Serve delicious and inexpensive food quickly.
The same applies to memory package development.

Why Distasteful, Expensive and Delayed?

Conventional Packaging Design Flow



- **Cause of Distasteful**

  Design quality is not stable because design accuracy depends on designer's skill.

- **Cause of Expensive**

  Package design became difficult and frequency of trial making increased because 3D structured package was increasing.

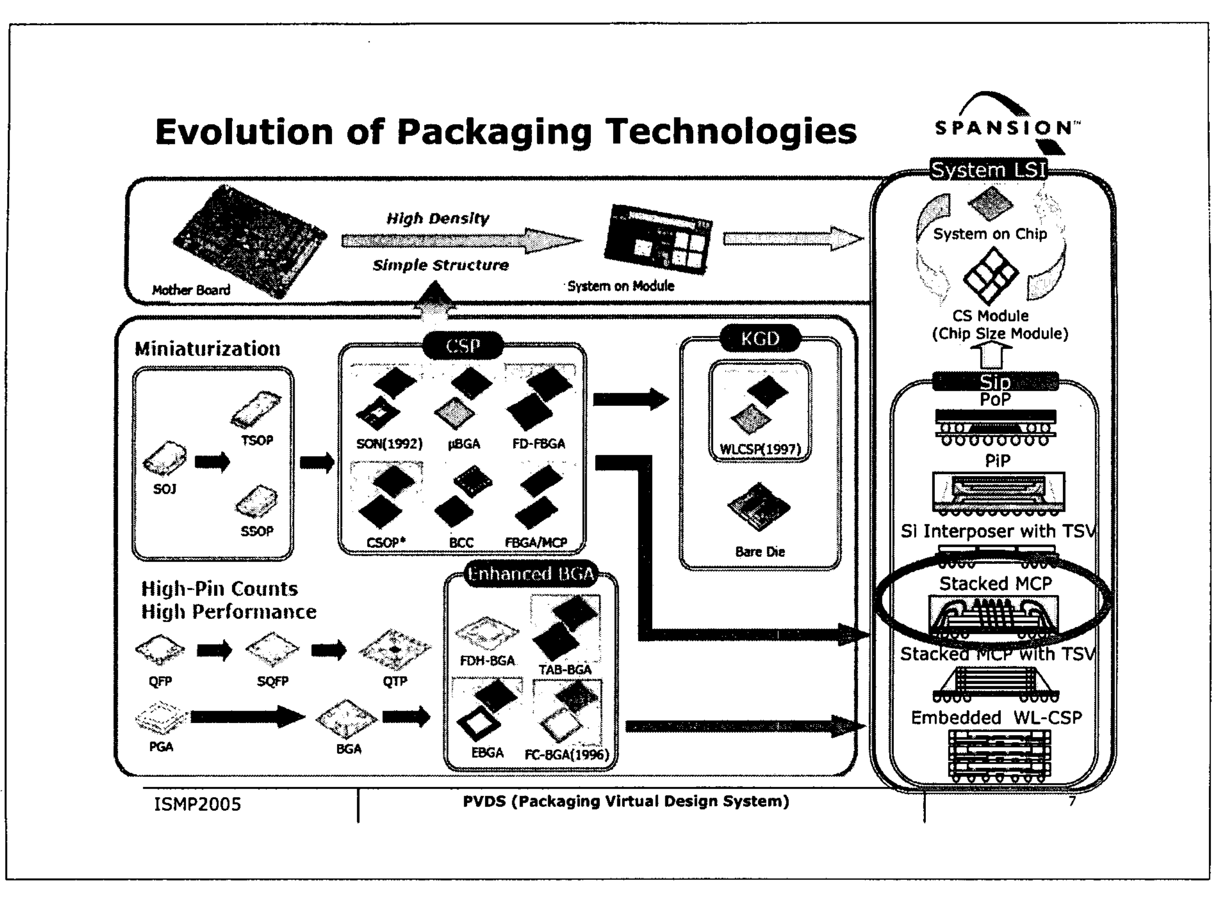
- **Cause of Delay**

  Increased complicated package with 3D structure and therefore takes long time to design.

Solution

System for realize "High Quality", "Low Cost" & "Short TAT" package development

PVDS (Packaging Virtual Design System)


Evolution of Packaging Technologies
SPANSION
Mother Board
High Density
Simple Structure
System on Module
System LSI
System on Chip
CS Module
(Chip Size Module)
Miniaturization
CSP
KGD
SOJ
TSOP
SSOP
SON(1992)
μBGA
FD-FBGA
CSOP*
BCC
FBGA/MCP
WLCSP(1997)
Bare Die
SiP
PoP
PiP
Si Interposer with TSV
Stacked MCP
Stacked MCP with TSV
Embedded WL-CSP
High-Pin Counts
High Performance
Enhanced BGA
QFP
SQFP
QTP
FDH-BGA
TAB-BGA
PGA
BGA
EBGA
FC-BGA(1996)
ISMP2005
PVDS (Packaging Virtual Design System)
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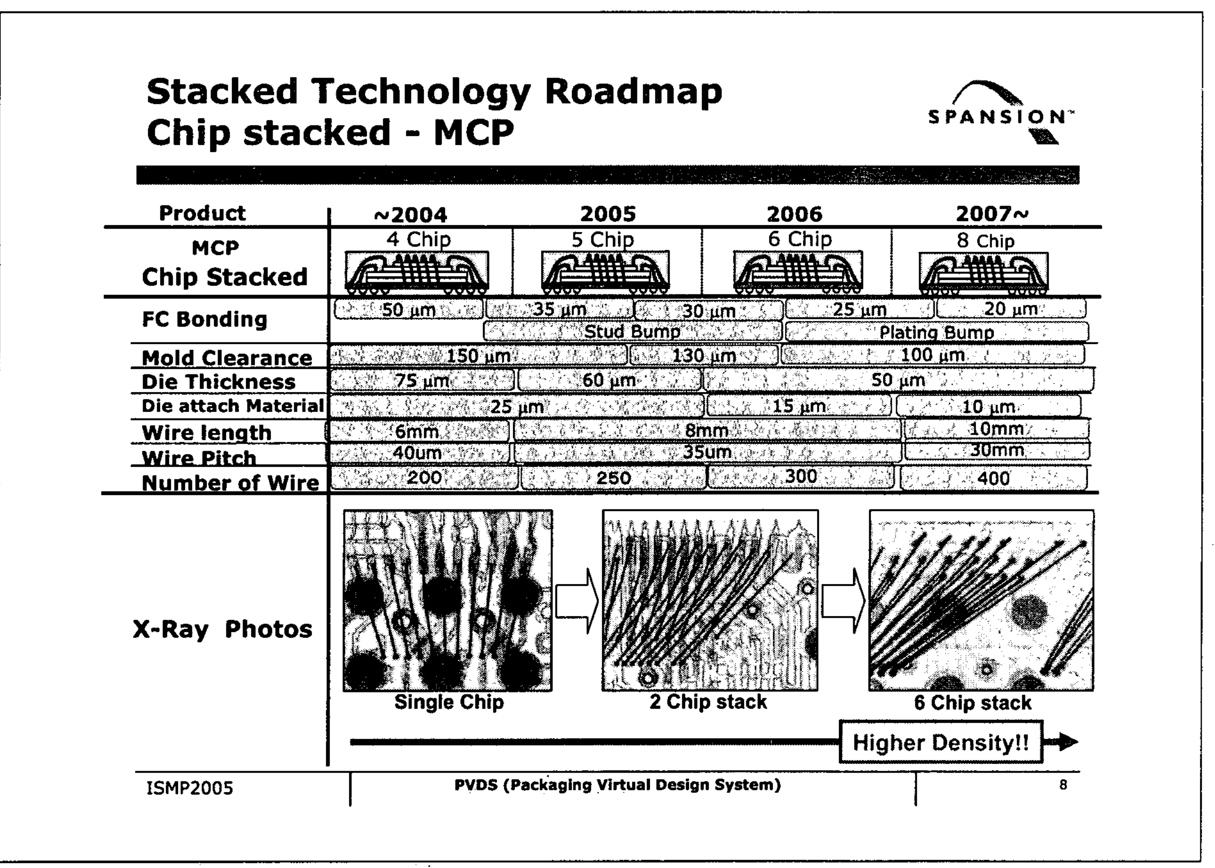
Stacked Technology Roadmap
Chip stacked - MCP
SPANSION
Product ~2004 2005 2006 2007~
MCP Chip Stacked: 4 Chip, 5 Chip, 6 Chip, 8 Chip
FC Bonding: 50 μm, 35 μm, 30 μm, 25 μm, 20 μm
Stud Bump, Plating Bump
Mold Clearance: 150 μm, 130 μm, 100 μm
Die Thickness: 75 μm, 60 μm, 50 μm
Die attach Material: 25 μm, 15 μm, 10 μm
Wire length: 6mm, 8mm, 10mm
Wire Pitch: 40um, 35um, 30mm
Number of Wire: 200, 250, 300, 400
X-Ray Photos
Single Chip
2 Chip stack
6 Chip stack
Higher Density!!
ISMP2005
PVDS (Packaging Virtual Design System)
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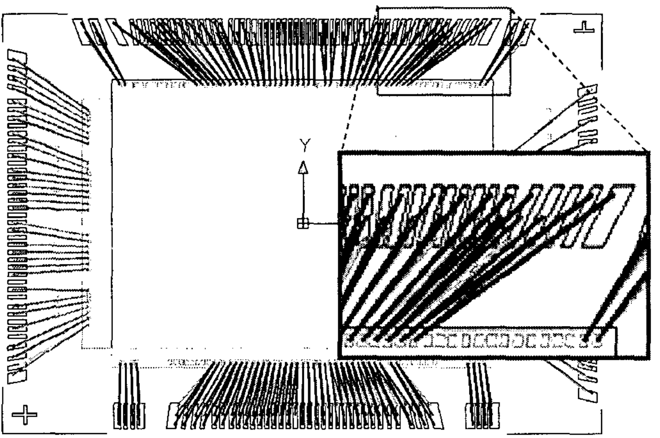
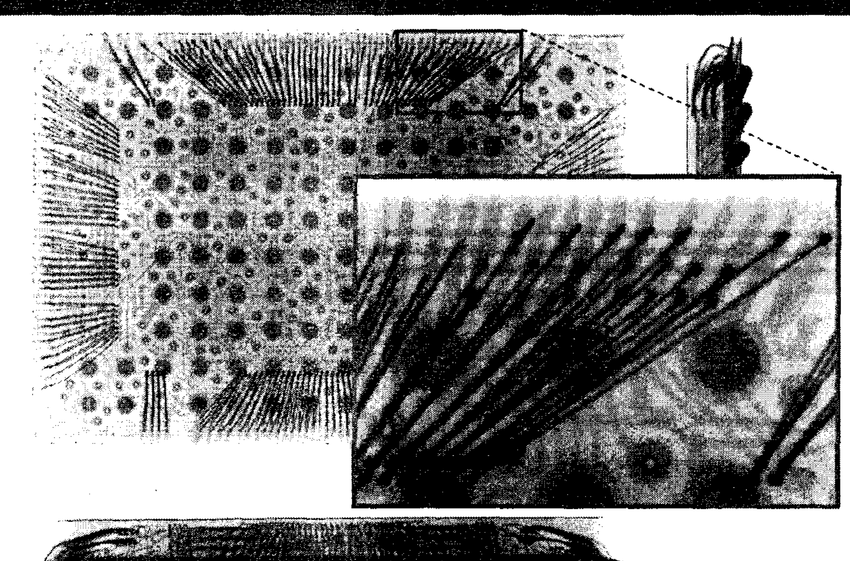
Example of 6-stacked die MCP Design

Wire shape verification by 2D design environment is difficult.



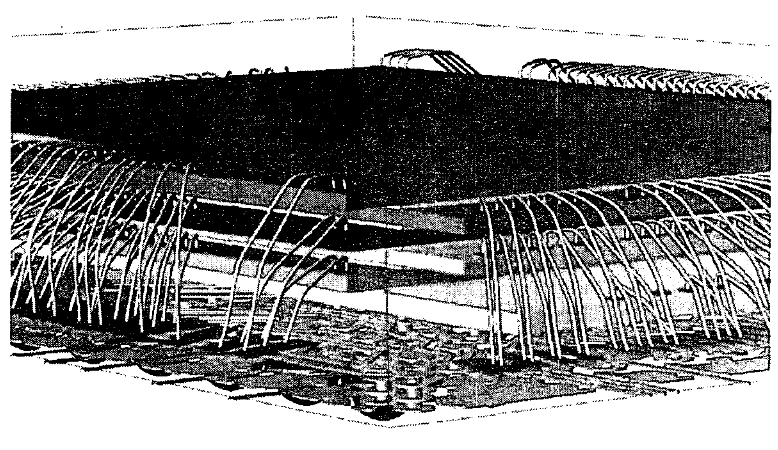
Typical 2D layout tool view of a stacked die package

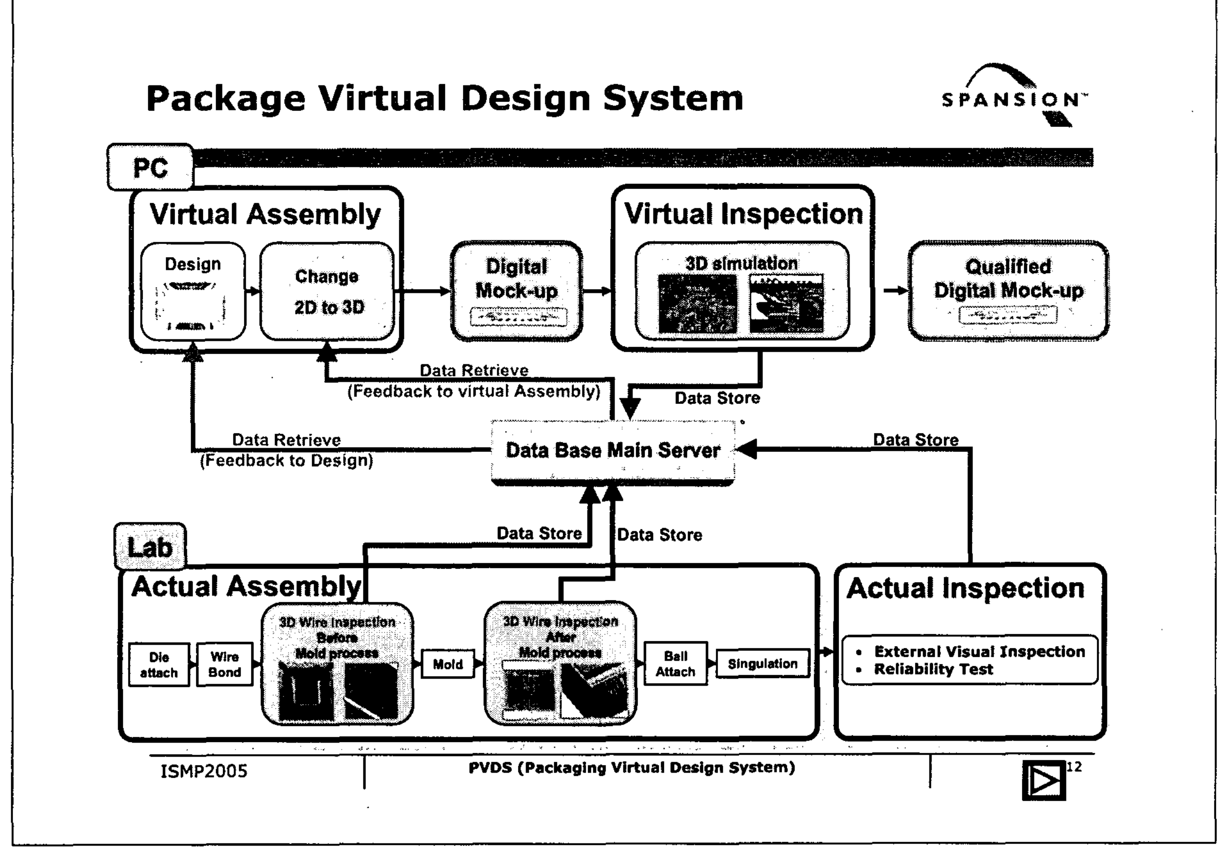
2D X-Ray Inspection of 6-stacked Die MCP



What should we do ?

Digital Mock-up





Virtual Assembly

SPANSION

Data base

2. Input parameters
- Thickness info
- Wire Profile
- Material Information

etc・・

2D CAD Data

1. Input data
- Design know-how
- Inspection data

etc・・

3. Make 3D-data from 2D-Data by automatic operation.

Digital Mock-up

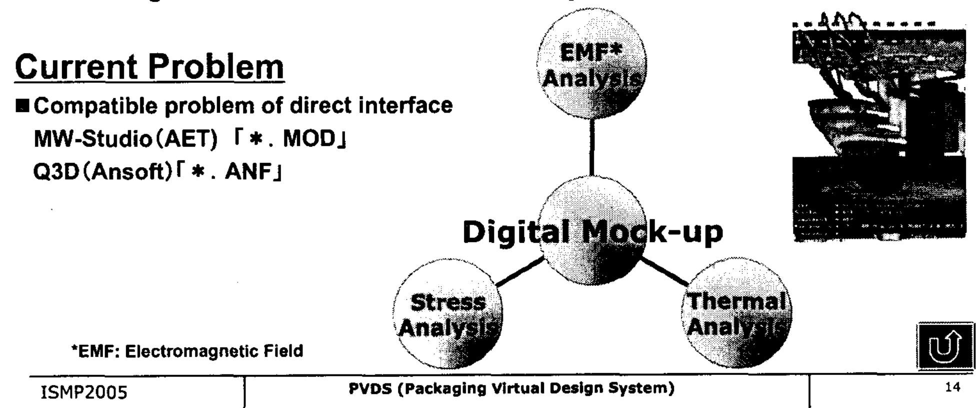
3D Simulation

Effect of Simulation

- Because evaluation is made in the design stage, frequency of trial making decreases and therefore contributes to quality improvement.
- Produce high-accuracy digital mock-up.
- Development period shortens by accumulating simulation result in the data base, and feeding back information when it is necessary.

Current Problem

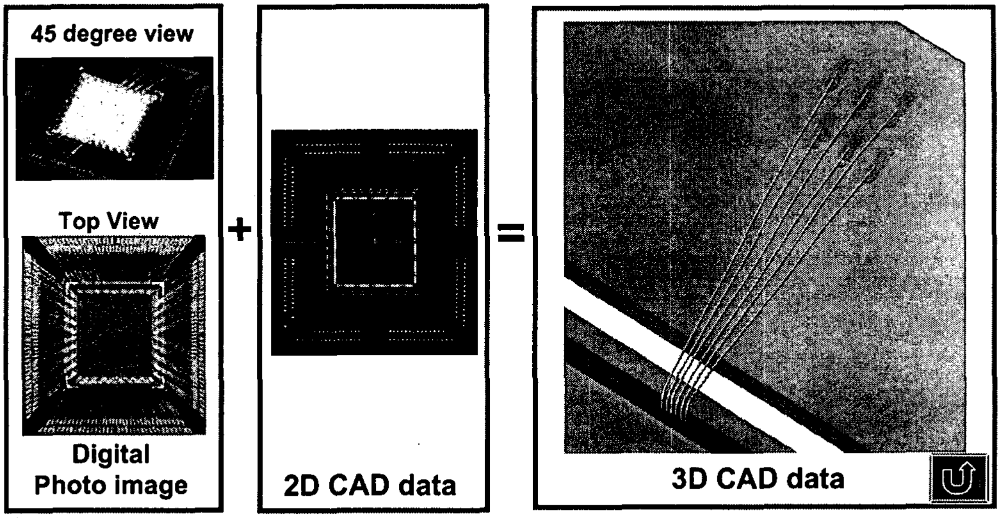
- Compatible problem of direct interface
  MW-Studio(AET) 「＊. MOD」
  Q3D(Ansoft)「＊. ANF」



*EMF: Electromagnetic Field

3D Wire Inspection before Mold Process
(Under development)

Provides real 3D wire shape on 3D CAD from digital photos and 2D CAD data.



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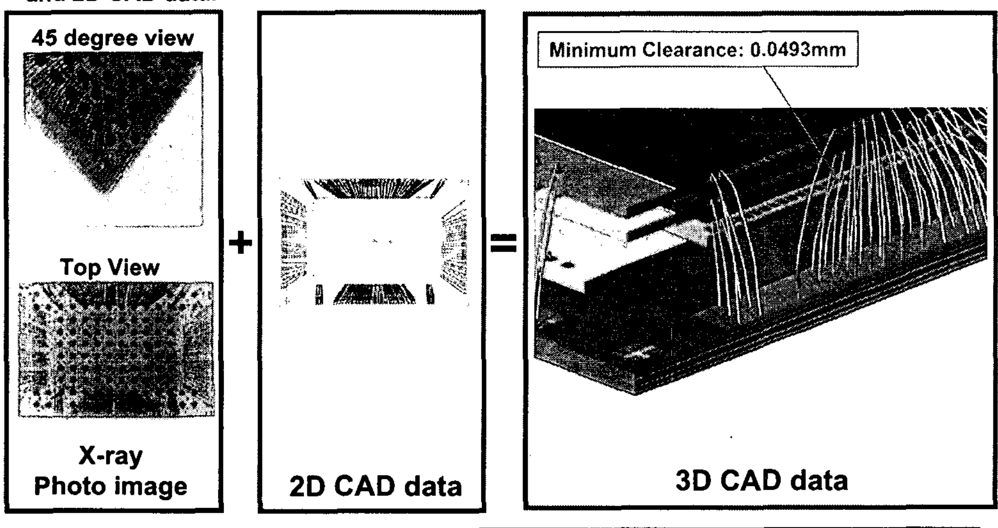
3D Wire Inspection after Mold Process

Provides real 3D wire shape on 3D CAD from X-ray photos (45 degree view & Top view) and 2D CAD data.



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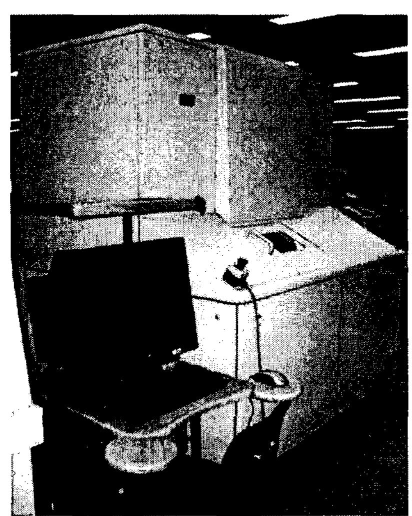
X-ray Machine System

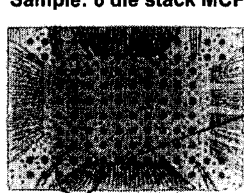
- Conventional X-ray equipment was purposed to penetrate package body for quality test after trial making.
- Newly developed prototype machine because we had needed system that the measurement value of a product was obtained from the photo taken with X-ray and the data is reflected in virtual mock-up.

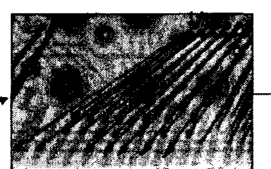


X-Ray Machine

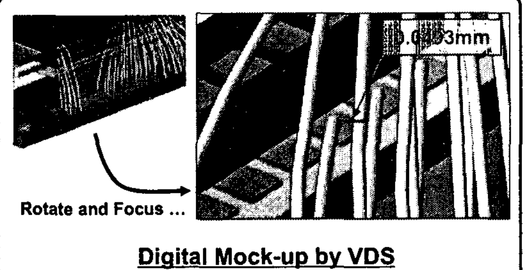
Comparison of Actual Mock-up vs Digital Mock-up

Sample: 6 die stack MCP



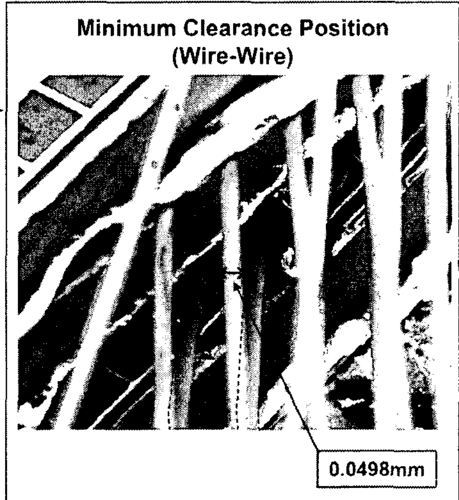


X-ray Photo image (TOP VIEW)

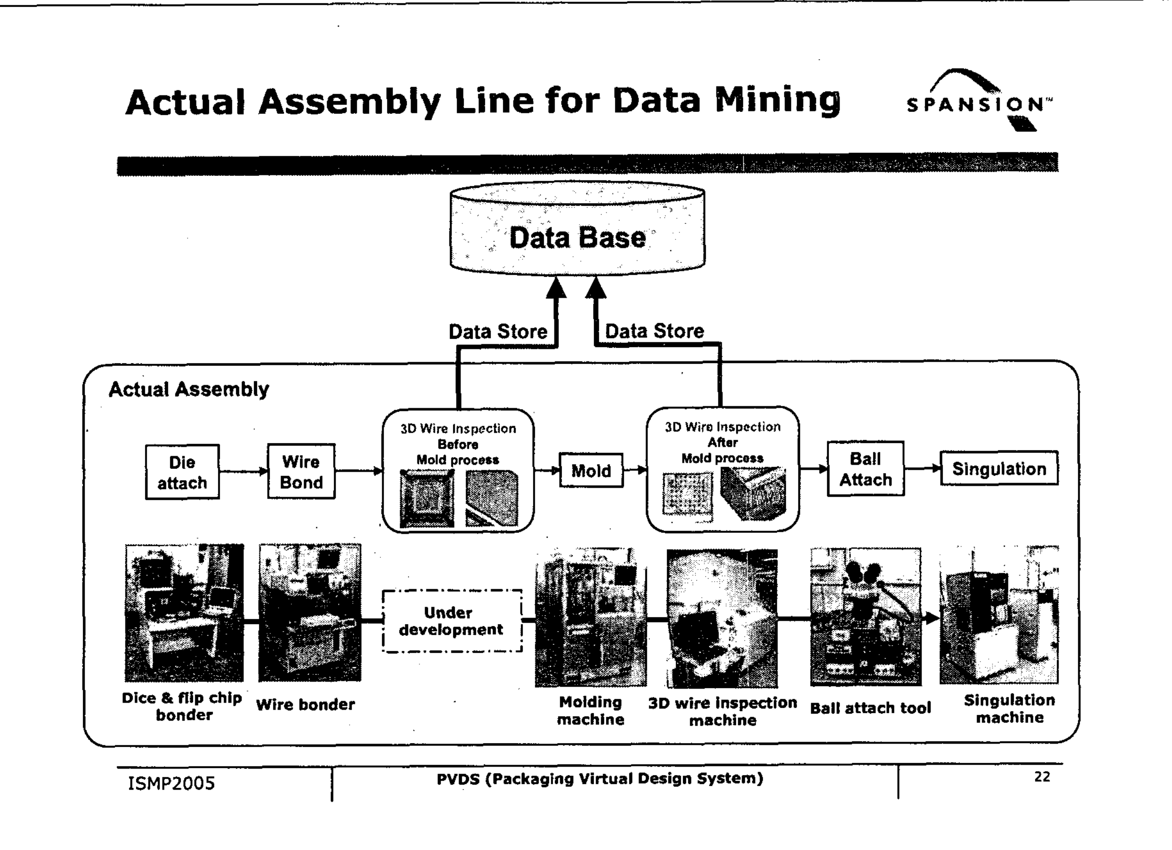


Digital Mock-up by VDS

Minimum Clearance Position (Wire-Wire)



Actual Wire Image (after Decap)



Actual Assembly Line for Data Mining
SPANSION
Data Base
Data Store
Data Store
Actual Assembly
Die attach
Wire Bond
3D Wire Inspection Before Mold process
Mold
3D Wire Inspection After Mold process
Ball Attach
Singulation
Under development
Dice & flip chip bonder
Wire bonder
Molding machine
3D wire inspection machine
Ball attach tool
Singulation machine
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PVDS (Packaging Virtual Design System)
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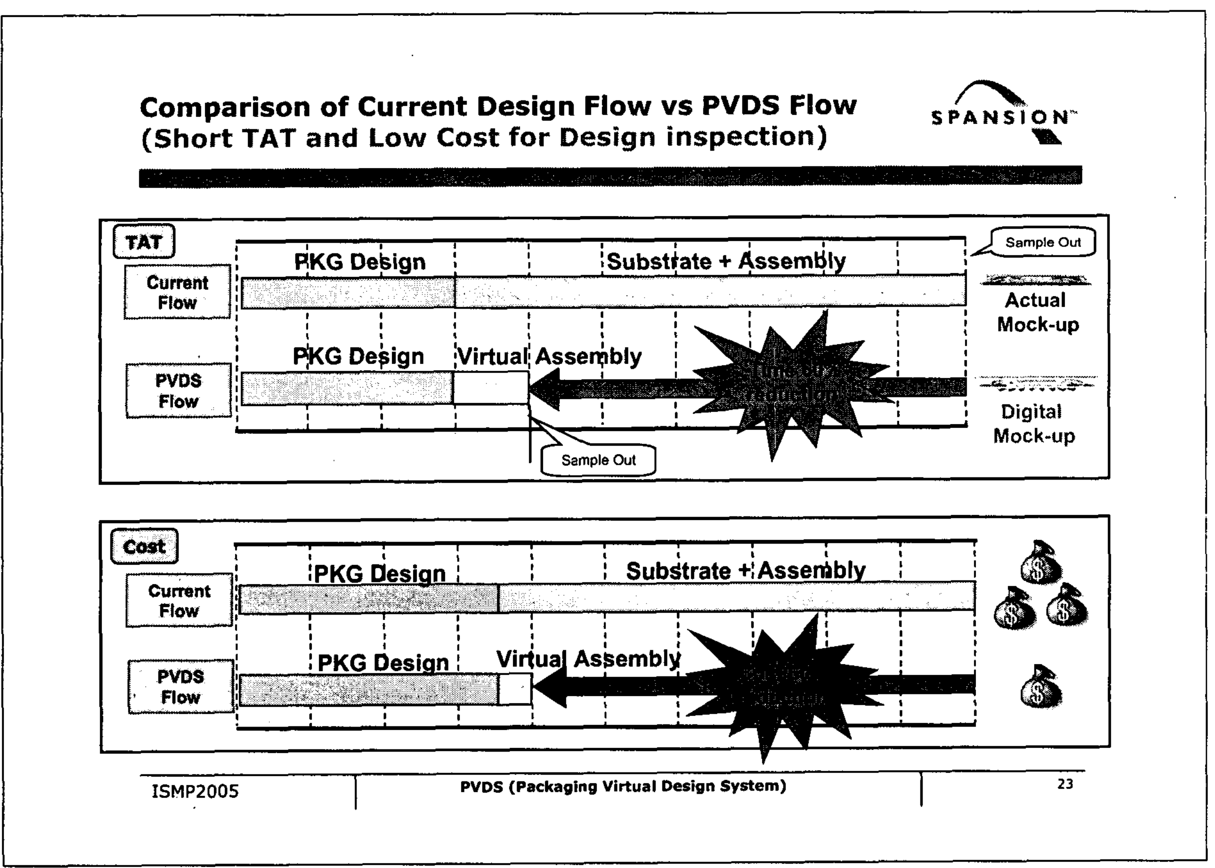

Comparison of Current Design Flow vs PVDS Flow
(Short TAT and Low Cost for Design inspection)
SPANSION
TAT
Current Flow
PKG Design
Substrate + Assembly
Sample Out
Actual Mock-up
PVDS Flow
PKG Design
Virtual Assembly
Digital Mock-up
Sample Out
Cost
Current Flow
PKG Design
Substrate + Assembly
PVDS Flow
PKG Design
Virtual Assembly
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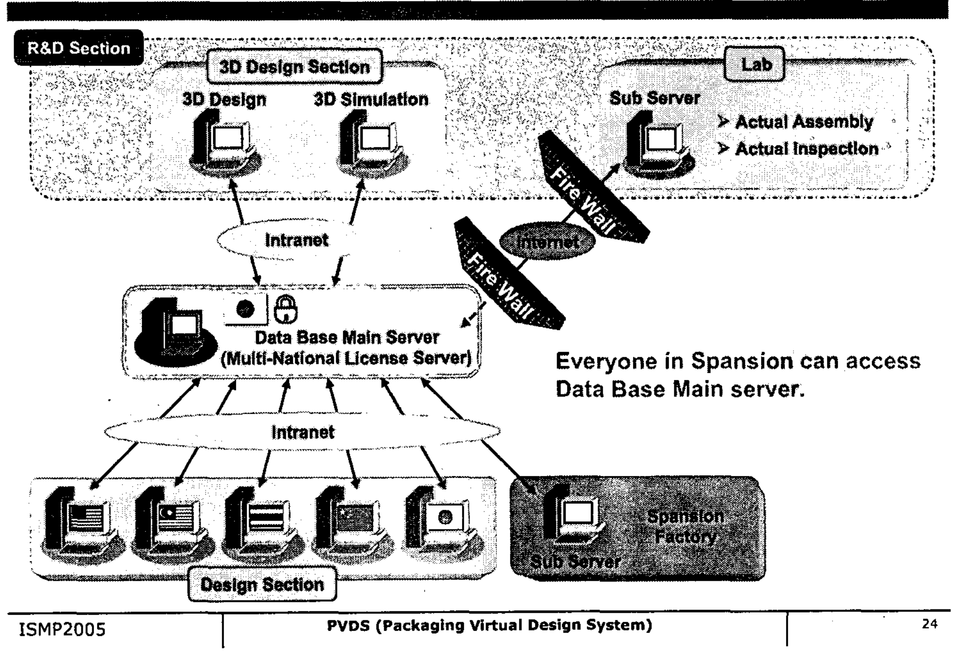
PVDS Network Integration (Future Vision)



Everyone in Spansion can access Data Base Main server.

Summary

- 3D verification of design value before trial making became possible visually by creating digital mock-up.
- Developed X-ray evaluation equipment to create prototype digitalized from an X-ray image to 3D.
- 3D of the prototype digitalization was done, and virtual mock-up of high accuracy was made.

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