A New Smart Stacking Technology for 3D-LSIs

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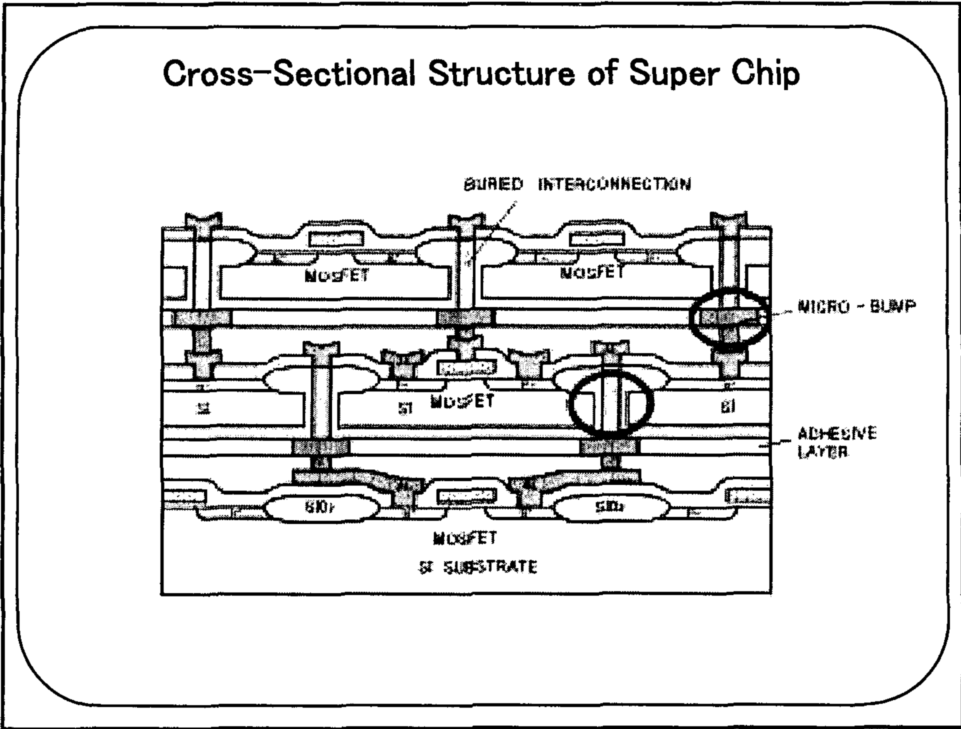
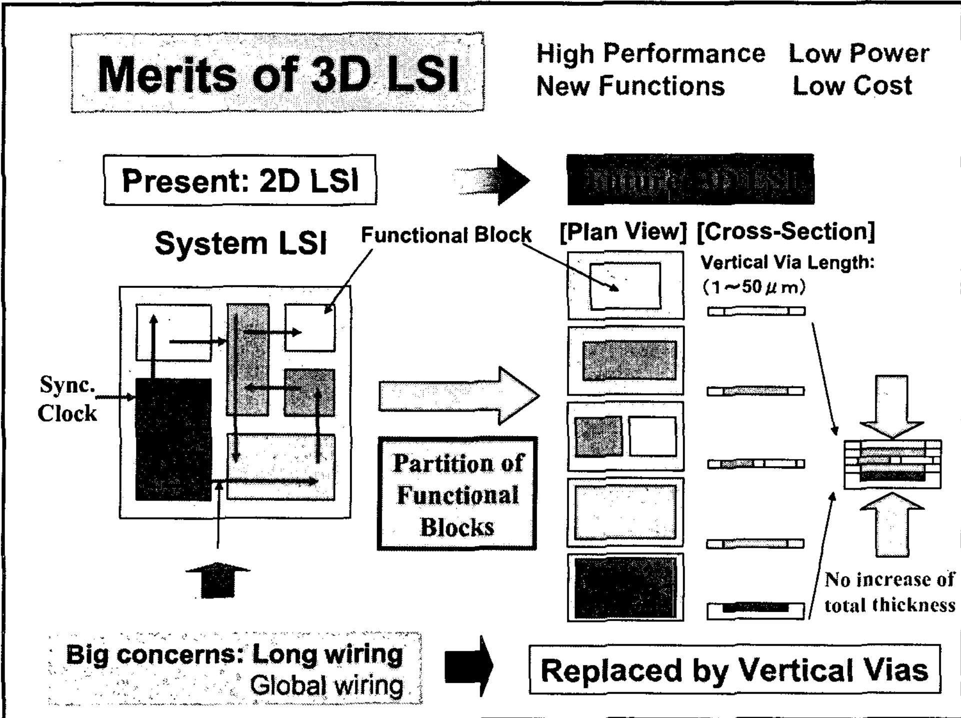
Outline

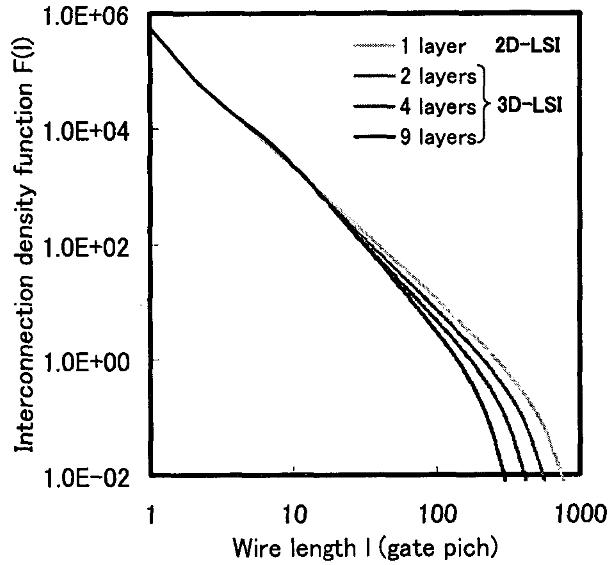
1. Introduction
2. Advantages of 3D LSI
3. Smart-Stack 3D Integration Technology
4. Fabrication and Evaluation 3D LSI Test Chips
5. Applications of Fabricated 3D LSI Chips
6. Summary


Cross-Sectional Structure of Super Chip
BURIED INTERCONNECTION
MOSFET
MOSFET
MICRO - BUMP
MOSFET
ADHESIVE LAYER
MOSFET
SI SUBSTRATE

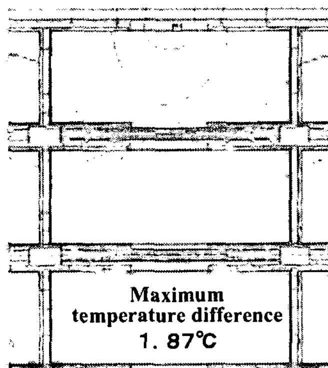

Merits of 3D LSI
High Performance
Low Power
New Functions
Low Cost
Present: 2D LSI
System LSI
Functional Block
[Plan View] [Cross-Section]
Vertical Via Length:
(1~50μm)
Sync. Clock
Partition of Functional Blocks
No increase of total thickness
Big concerns: Long wiring
Global wiring
Replaced by Vertical Vias

Interconnection Length Distribution in LSIs

(Vertical interconnection relative length d=5)

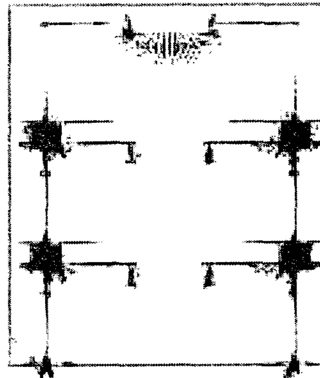


Simulated Heat Flow in 3D Structure



(a) Contour map of isothermal lines

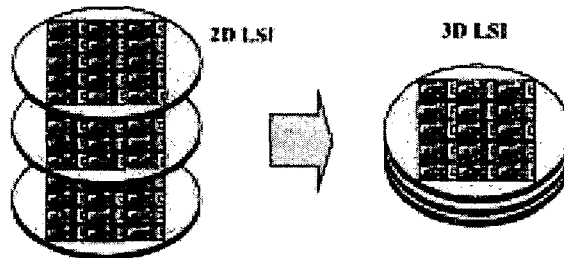
Power of heat provided to heat source: 58.5 mW
Temperature at the bottom: 0°C



(b) Heat flow distribution

Distance between heat source and buried interconnection: 31.9 μm
Micro-bump size : 10 μm × 10 μm
Diameter of buried interconnection: 2.5 μm
Si thickness : 30 μm

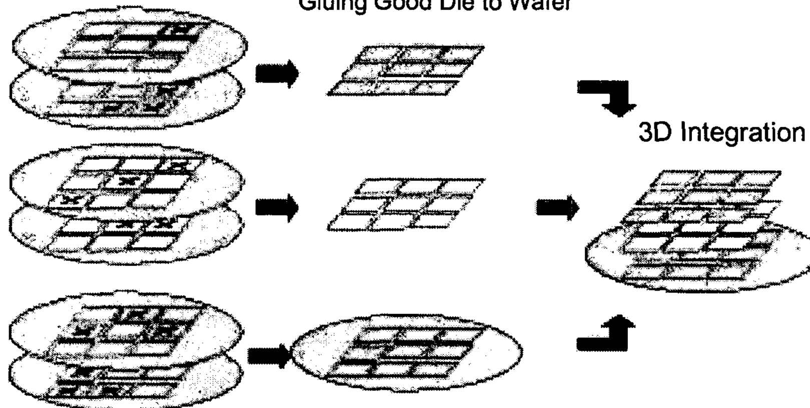
A new 3D integration technology using a novel wafer level stacking method



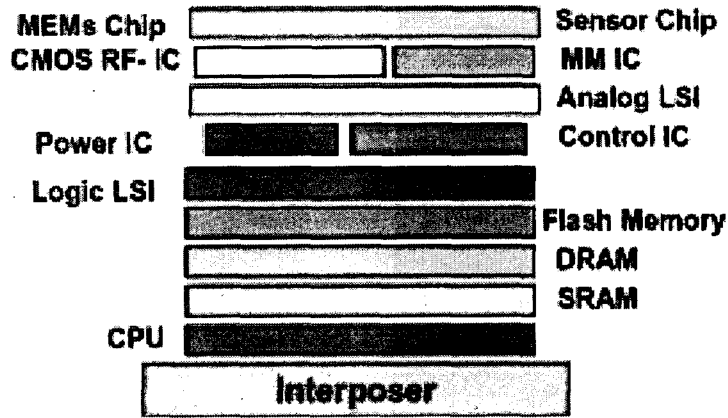
Advantages of our 3D Integration Technology

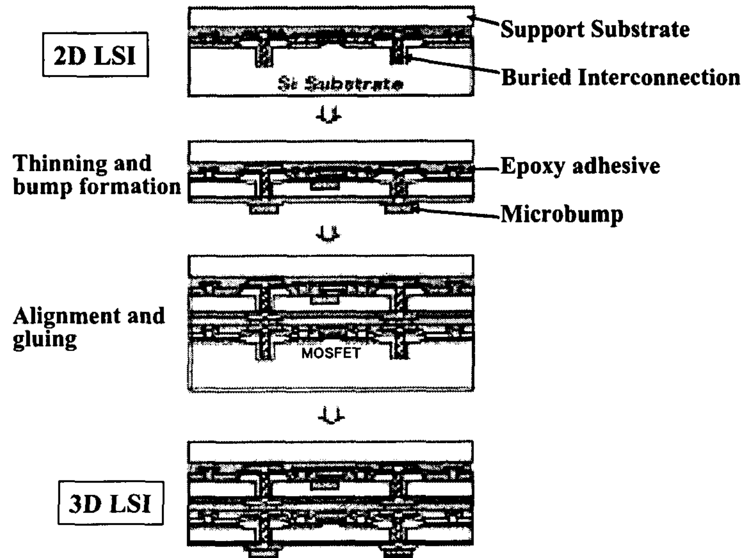
- **Different LSI wafers, which were independently fabricated are vertically stacked to form 3D LSI.**
  Decreasing of total process time
- **Compatible with normal LSI process.**
  No needing an excessive increase of processing step and complexity
- **High density short interconnection can be formed.**
  - Increasing system performance (Parallel Processing)

Fabrication Method for Super Chip Using Smart-Stack Technology

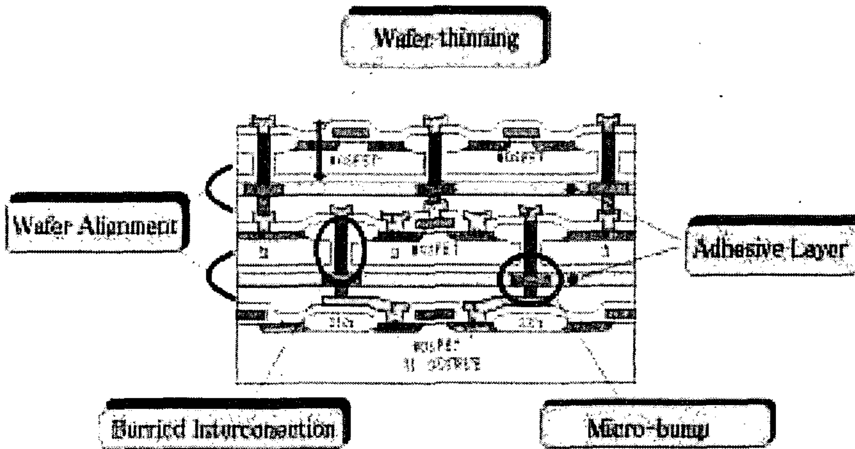


Semi-Fabless™ **Super Smart Stack (SSS) Technology™**

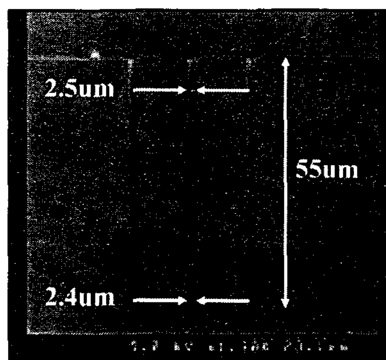

Super Chip with 3D Stacked Structure
MEMs Chip
CMOS RF- IC
Power IC
Logic LSI
CPU
Sensor Chip
MM IC
Analog LSI
Control IC
Flash Memory
DRAM
SRAM
Interposer


Fabrication Sequence of 3D LSI
2D LSI
Support Substrate
Buried Interconnection
Si Substrate
Thinning and
bump formation
Epoxy adhesive
Microbump
Alignment and
gluing
MOSFET
3D LSI

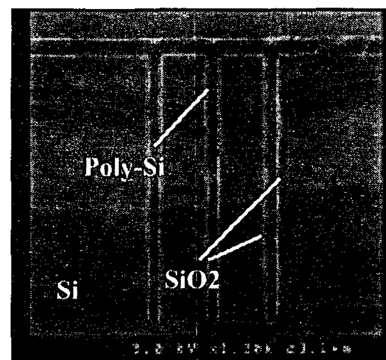
Key Technology for 3D LSI



SEM Cross Section of Buried Interconnection



(a) Si deep trench etching



(b) Filling with Poly-Si

SEM Cross-Sectional View of W Buried Vertical Interconnection

1μm

50μm

W

Si

930nm

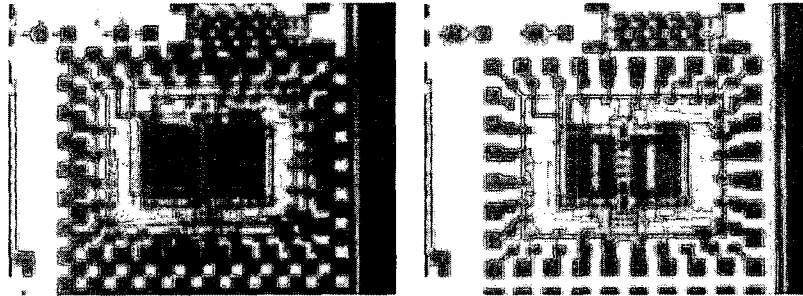
W

Poly-Si (500nm)

SiO_2 (600nm)

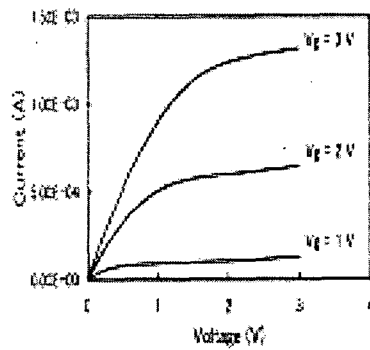
Photograph of 3D Wafer Aligner

Infrared Images of 3D Test Chip Before and After Alignment

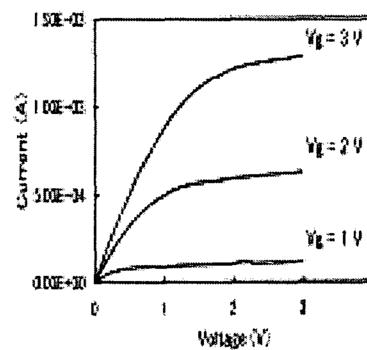


Before alignment **After alignment**

I_d-V_d Characteristics of NMOSFET(L_g=1.5mm) Before and After Stacking



Before stacking(2D LSI chip)

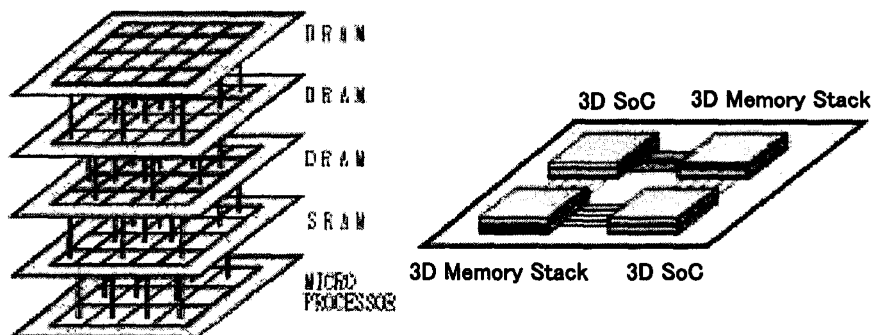


After stacking(3D LSI chip)

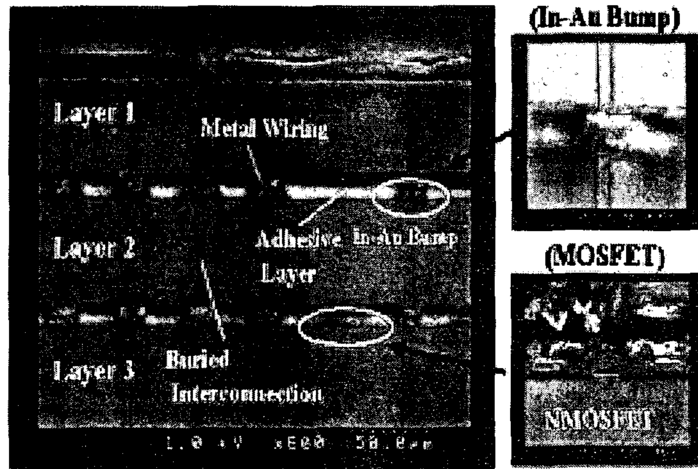
Publications of Fabricated 3D IC Chips

- 3-layer stacked image sensor chip (Mitsubishi)
  Laser recrystallization (IEDM, 1986)
- 3-layer stacked image sensor chip (Tohoku Univ.) (IEDM, 1999)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked memory chip (Tohoku Univ.) (IEDM, 2000)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 2-layer stacked image sensor chip (MIT) (ISSCC, 2001)
  SOI wafer bonding
- 3-layer stacked artificial retina chip (Tohoku Univ.) (ISSCC, 2001)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 3-layer stacked microprocessor chip (Tohoku Univ.) (**Cool Chips**, 2002)
  Wafer bonding (Wafer non-transfer, Buried interconnection)
- 2-layer stacked image sensor chip (MIT) (ISSCC, 2005)
  SOI wafer bonding

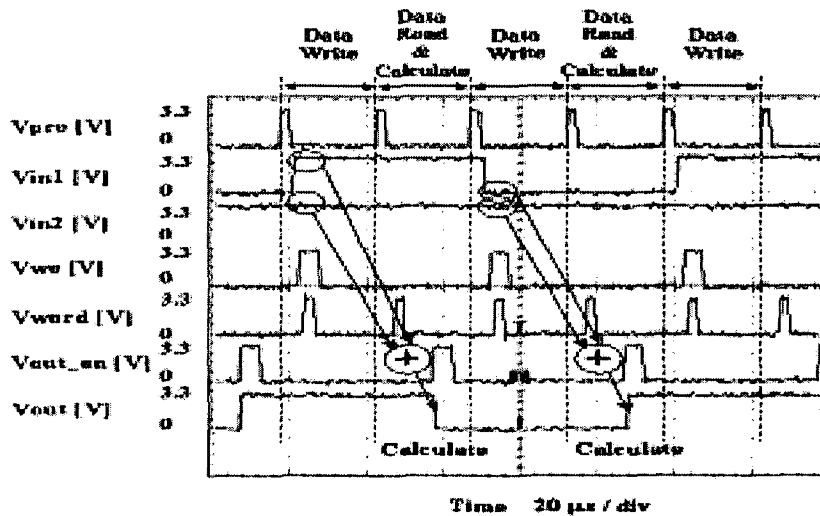
3D Computer Chip and 3D Multi-chip Module



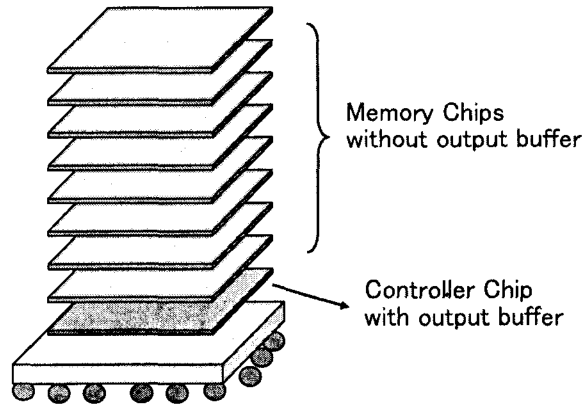
SEM Cross-Section of 3D Computer Test Chip



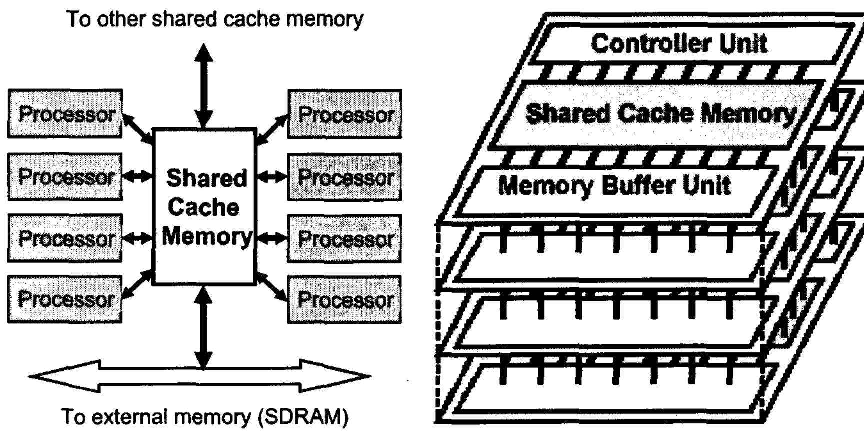
Measured Waveforms of 3D Computer Test Chip (SRAM layer: 3.3V, Processor layer: 2.5V)



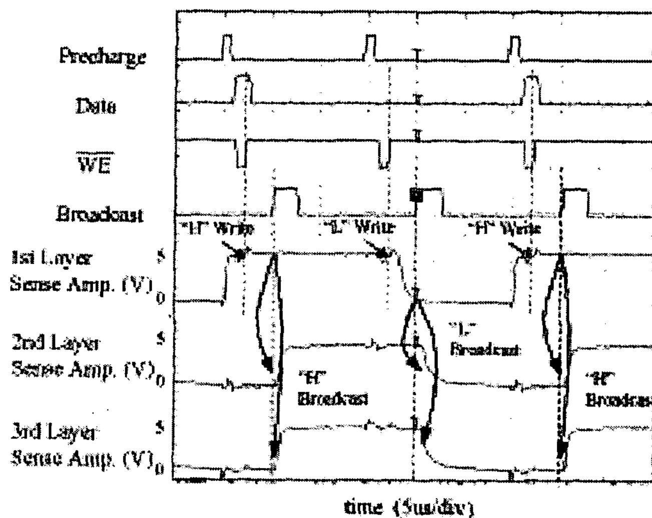
High Density, High Speed 3D Memory Chip



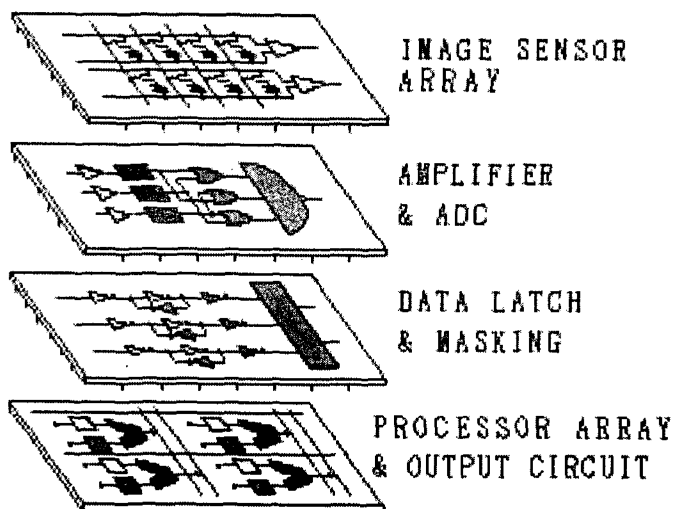
Shared Cache Memory with 3D Structure



Measured Waveforms in Broadcast Operation of 3D Shared Cache Memory

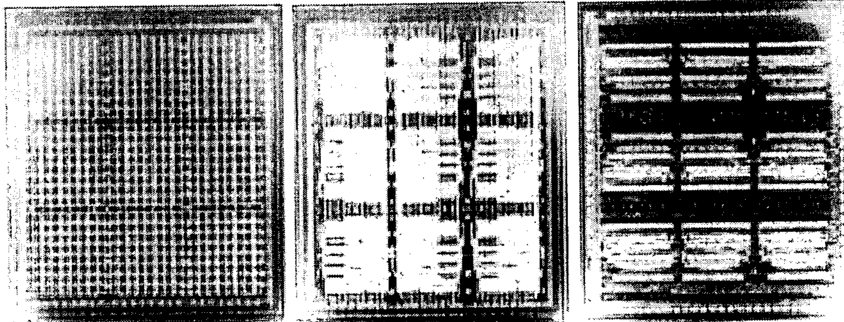


Real-Time Image Processing System with 3D Stacked Structure



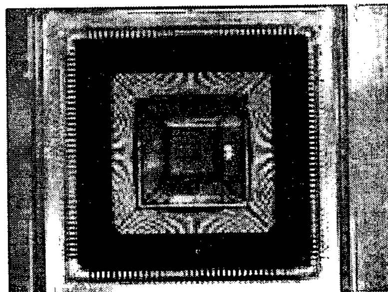
Photograph of respective chip in 3D stacked image sensor chip with three stacked layers

1st Layer (Photosensor circuit) | 2nd Layer (Register circuit) | 3rd Layer (ADC & ALU circuit)

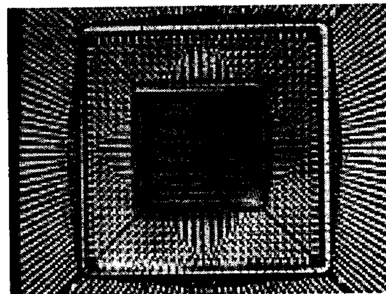


(Chip size : 6 mm x 6 mm, 112 pins)

Photograph of 3D Stacked Image Sensor Chip with Three Stacked Layers

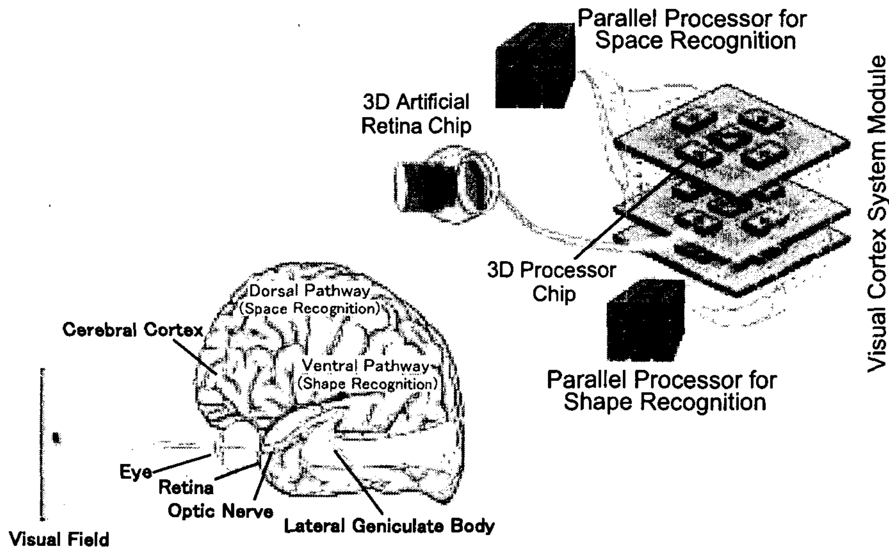


(a)

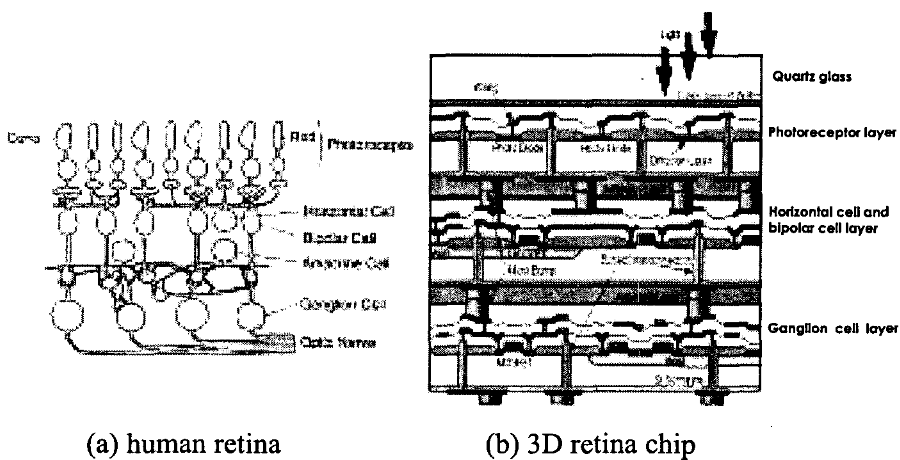


(b)

Brain-Type Information Processing System

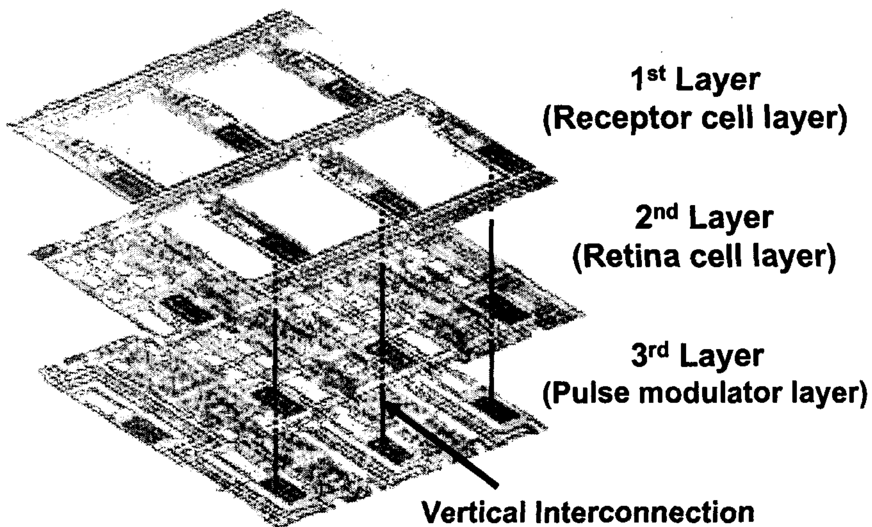


Cross-Sectional Structures of Human Retina and 3D Artificial Retina Chip



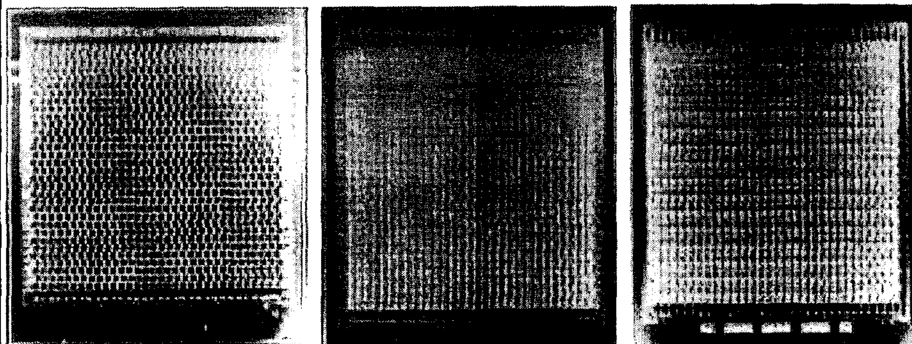
(a) human retina (b) 3D retina chip

Photograph of 3D Artificial Retina Chip



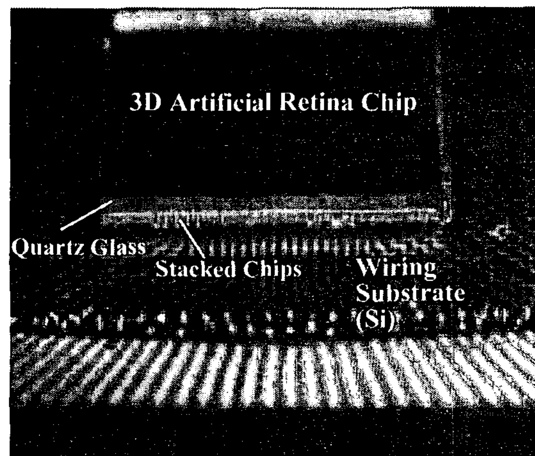
Photograph of Respective Chip in 3D Artificial Retina Chip with Three Stacked Layers

1st Layer	2nd Layer	3rd Layer
(Photoreceptor cell array)	(Bipolar, Horizontal, Ganglion cells array)	(Pulse modulator cell array)



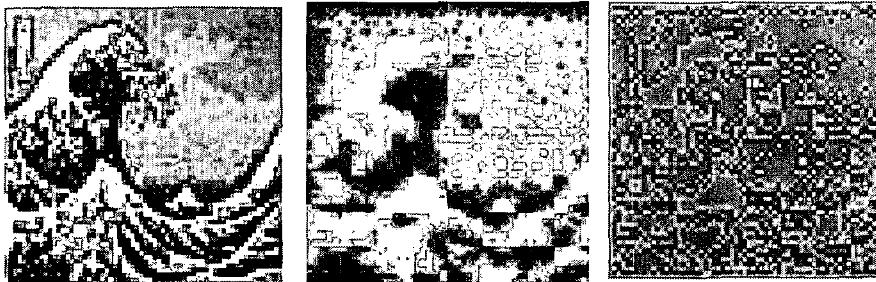
(Chip size : 6 mm x 6 mm, 112 pins)

Photomicrograph of 3D Artificial Retina Chip



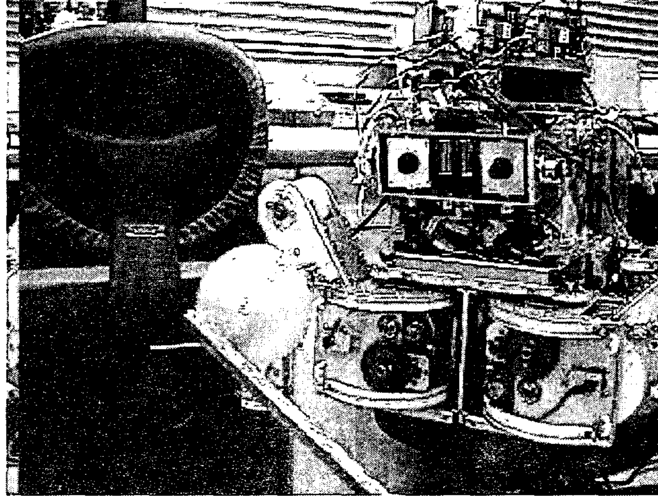
Visual Information Processing Using 3D Artificial Retina Chip

(64 × 64 photo receptor cells)



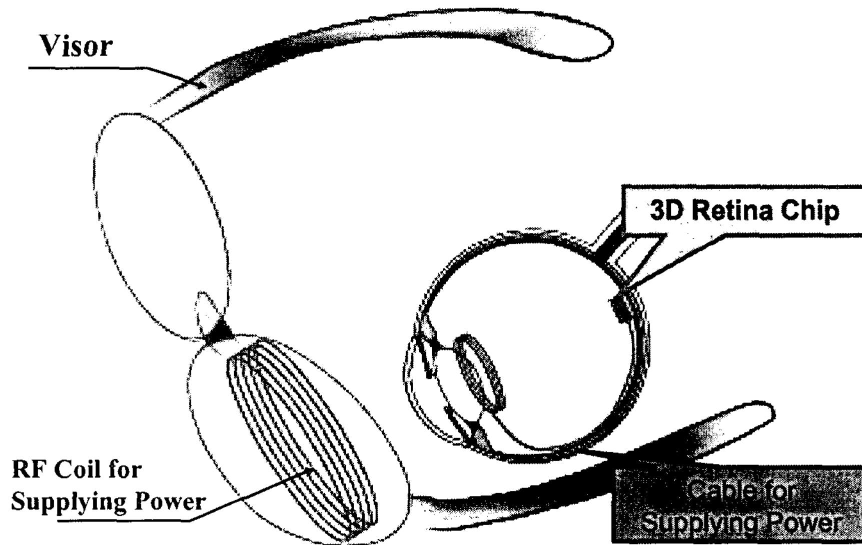
(a) Input pattern (b) Output pattern from photo circuit (c) Output pattern from Ganglion cell circuit

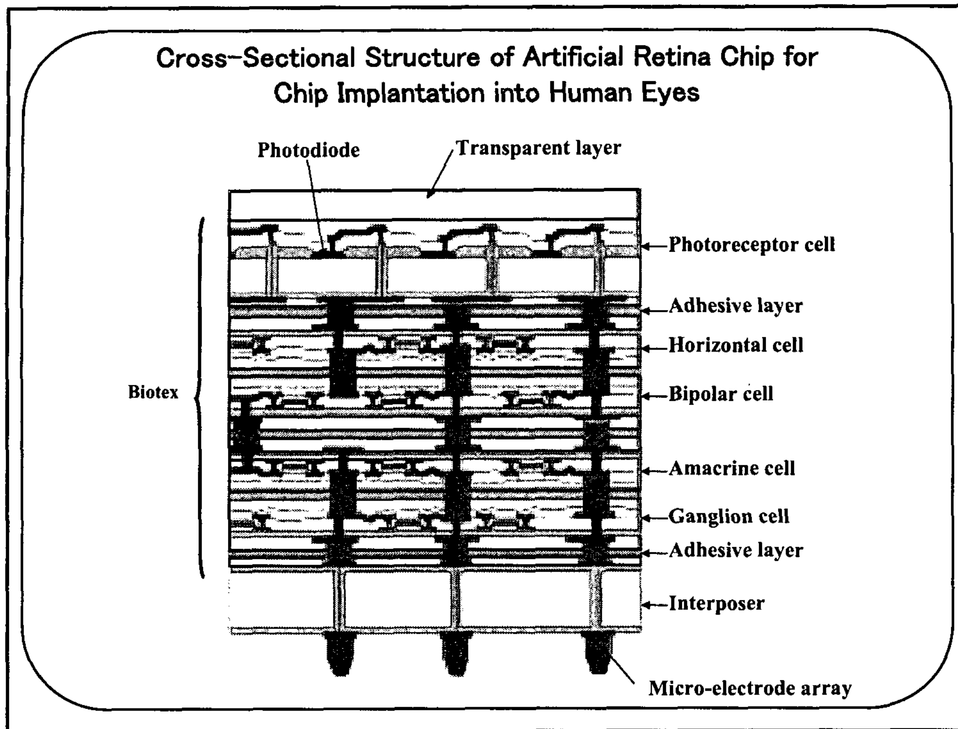
Robot Eyes with Smooth Pursuit Function Using Vision Chip

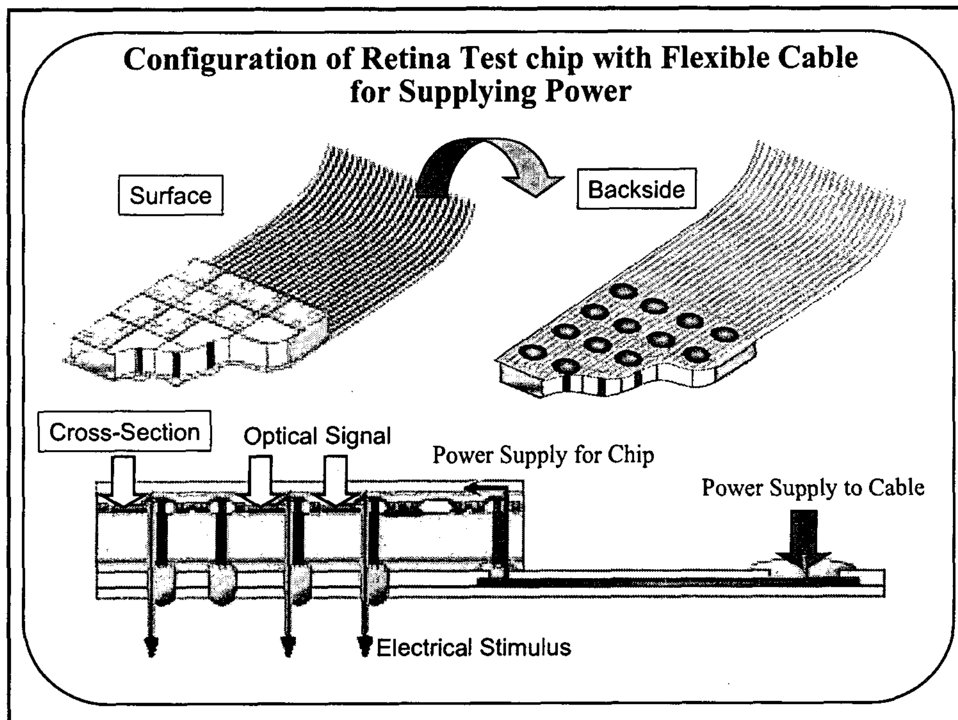


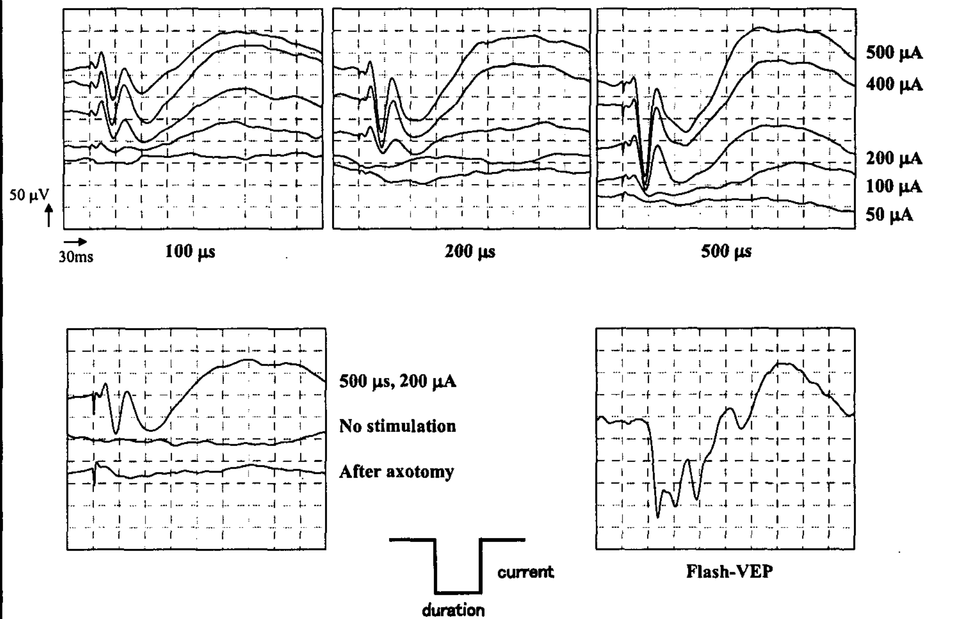
By courtesy of Prof. Konno (Dept. of Aerospace Engineering, Tohoku University)

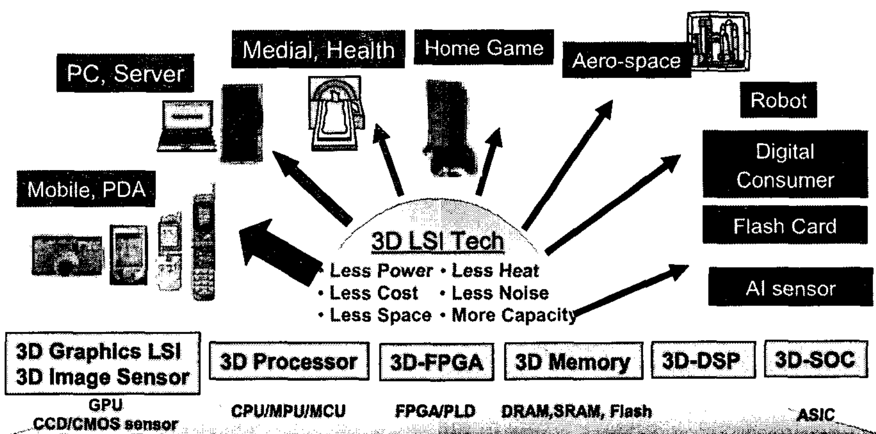
3D Retina Chip Implantation into Human Eye




Cross-Sectional Structure of Artificial Retina Chip for
Chip Implantation into Human Eyes
Photodiode
Transparent layer
Photoreceptor cell
Adhesive layer
Horizontal cell
Biotex
Bipolar cell
Amacrine cell
Ganglion cell
Adhesive layer
Interposer
Micro-electrode array


Configuration of Retina Test chip with Flexible Cable
for Supplying Power
Surface
Backside
Cross-Section
Optical Signal
Power Supply for Chip
Power Supply to Cable
Electrical Stimulus


EEP (Electrically Evoked Potential) Signals Observed in Brain
After Electrical Current Pulse Stimulation of Retina Cells
500 μA
400 μA
200 μA
100 μA
50 μA
50 μV
30ms
100 μs
200 μs
500 μs
500 μs, 200 μA
No stimulation
After axotomy
current
duration
Flash-VEP


Application of 3D LSI Technology
PC, Server
Medial, Health
Home Game
Aero-space
Robot
Digital Consumer
Flash Card
AI sensor
Mobile, PDA
3D LSI Tech
• Less Power • Less Heat
• Less Cost • Less Noise
• Less Space • More Capacity
3D Graphics LSI
3D Image Sensor
3D Processor
3D-FPGA
3D Memory
3D-DSP
3D-SOC
GPU
CCD/CMOS sensor
CPU/MPU/MCU
FPGA/PLD
DRAM,SRAM, Flash
ASIC

Summary

- A new 3D integration technology using wafer-to-wafer and chip-to-wafer stacking method was described.
- It was demonstrated that 3D microprocessor, 3D shared memory, 3D image processing chip and 3D artificial retina chip fabricated using 3D integration technology were successfully operated.
- The possibility of applying 3D image processing chip and 3D artificial retina chip to Robot's eye was investigated.
- The possibility of implanting 3D artificial retina chip into human eye was investigated.