Optimization for Chip Stack in 3D Packaging

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(Seiko Epson/Japan)

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ISMP 2005

Optimization of terminal structure for chip stack in 3D packaging

September 28, 2005

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Advanced Technology Development Department
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1. Introduction

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Advantages of 3D packages with Through-Silicon Vias

1. Extremely small
2. Reduction of the number of parts
3. Good electrical transmission characteristics
4. Possibility of wafer level production
5. Cost reduction

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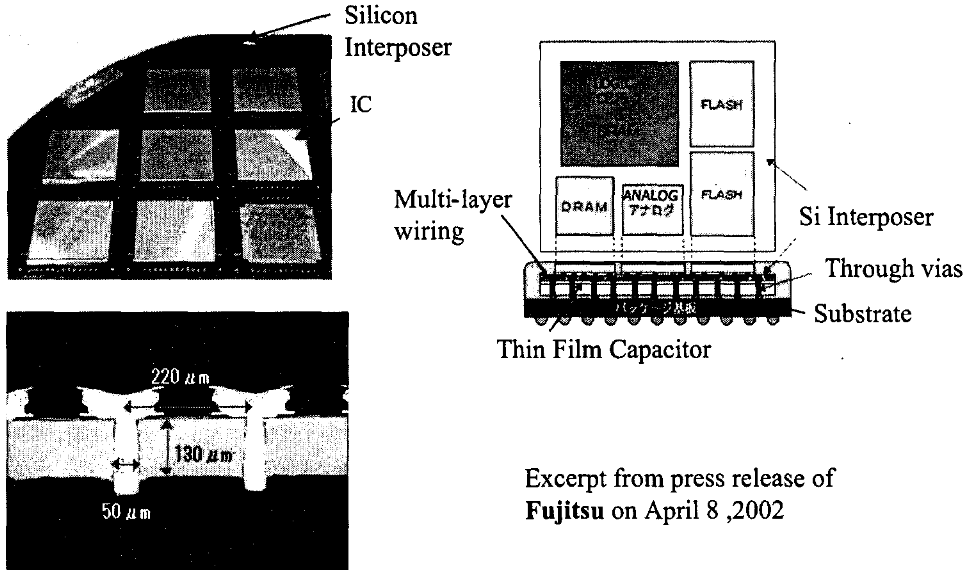
Applications of the Technology

(1) Silicon Interposer module



Excerpt from press release of
Fujitsu on April 8 ,2002

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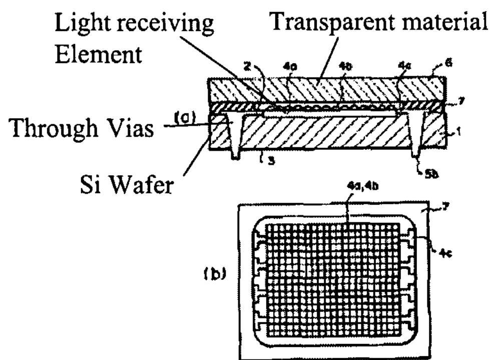
Applications of the Technology

(2) CCD Module



2001-351997
(Patent application laid-open
disclosure number)

Canon

Except from press release of
ASET on Feb 18, 2004

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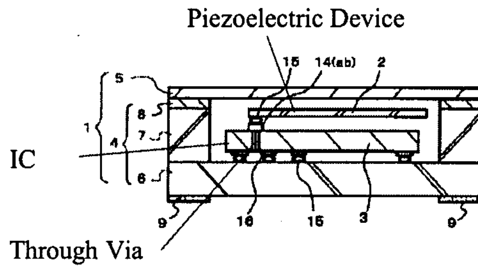
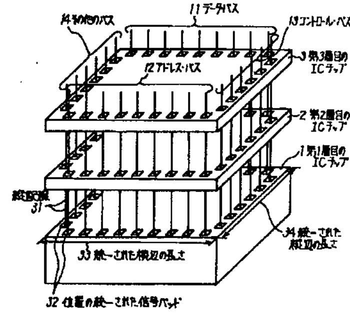
Applications of the Technology

(3) MEMS complex



JP3634676
Nihon Dempa Kogyo Co., Ltd

(4) Memory stack



JP2605968
NEC

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2. Model and Process Flow

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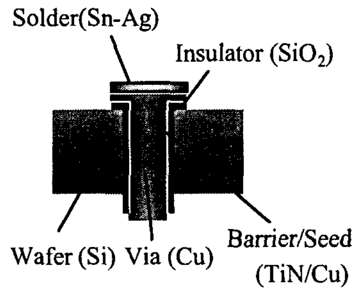
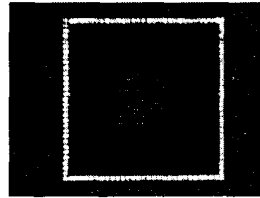
Model

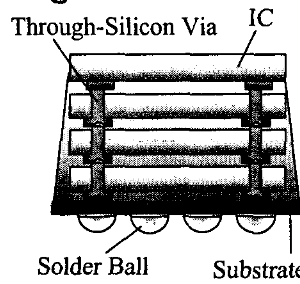
Through-Silicon via



Chip



Package



Specification

Size	5mm x 5mm
Thickness	45 μm
I/O Count	120
Pitch	150μm
Pad size	120μm
Diameter of via	35μm x 35μm

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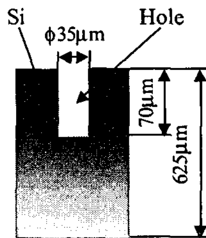
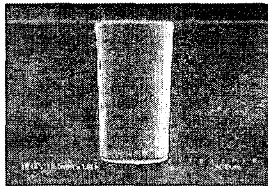
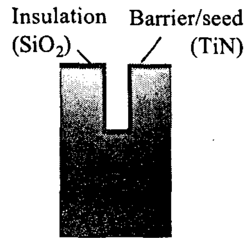
Process Flow

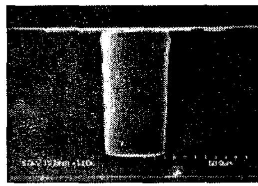
(1) Hole opening



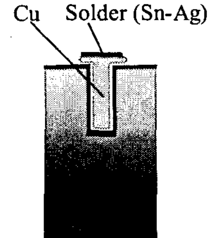


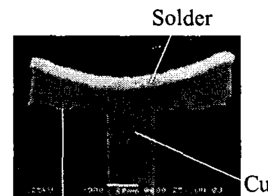
(2) Layer forming





(3) Cu Filling





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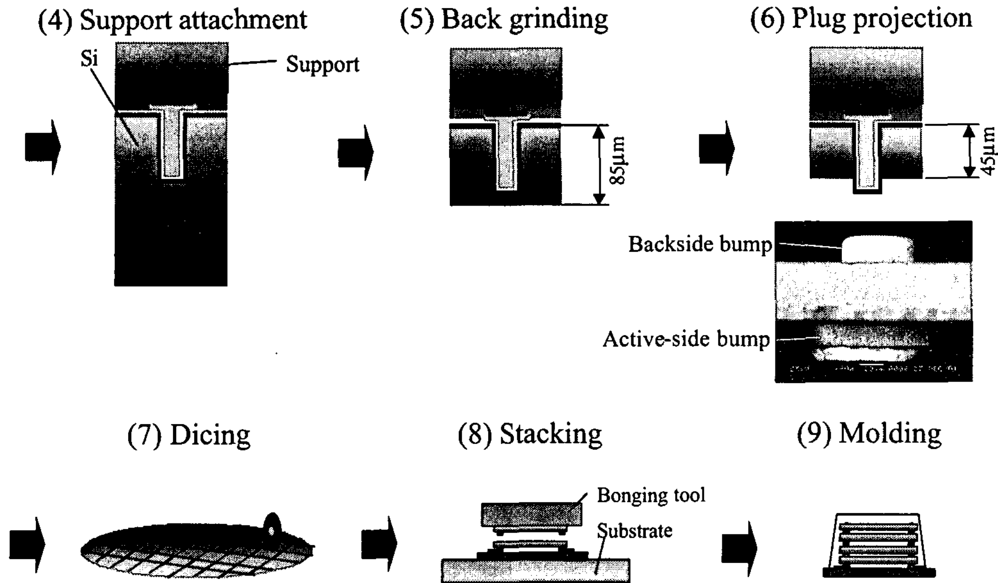
Process Flow



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Features

- No flattening process for active-side terminals
- No insulation layer on the backside of wafer
- Simple process
- Cost reduction

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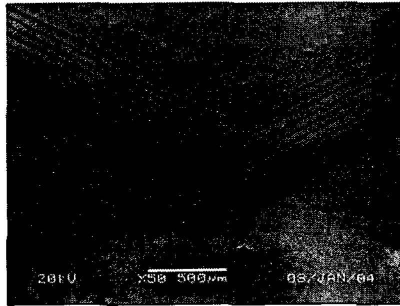
3. Optimization for interconnection



10-layer chip stack

Specification

Package
Thickness 810µm
IC
Size 5mm x 5mm
I/O Count 120
Pitch 150µm

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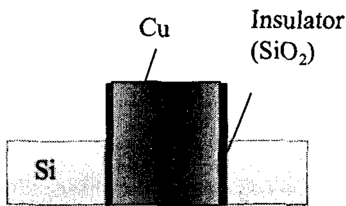
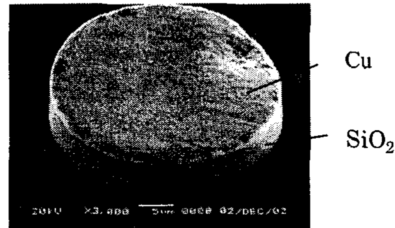
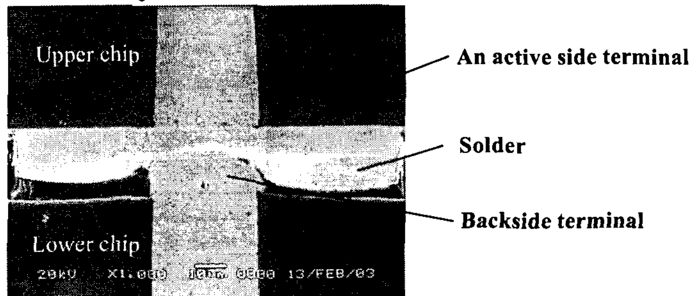
Solder Drop

Initial structure of backside terminals





Solder drop at solder joints



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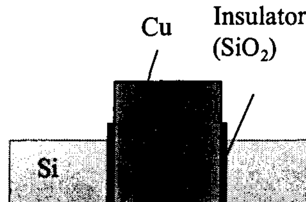
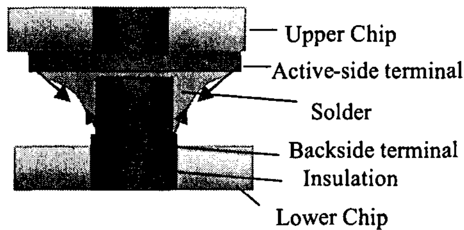
Modification

The modified structure of backside terminals



Verification using test chips

Solder shape and directions of surface tensions



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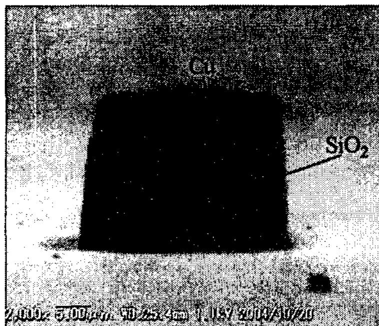
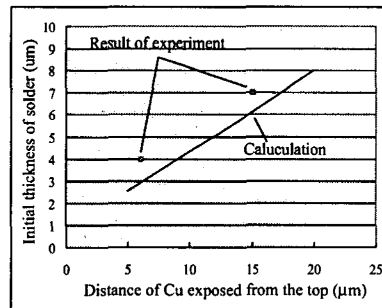
Result of the Modification

Modified backside terminal

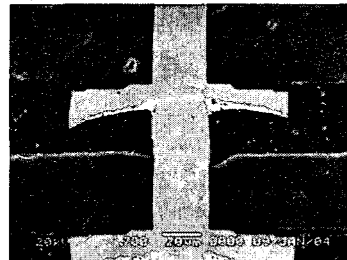


Estimation of the amount of solder



Specification of modified terminals	
Height	25μm
Distance of Cu exposure	7μm
Initial thickness of solder	4μm

Solder Joint



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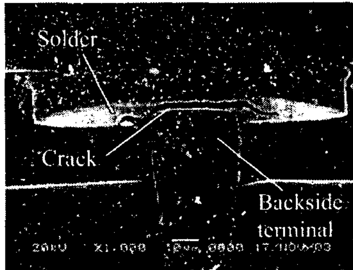
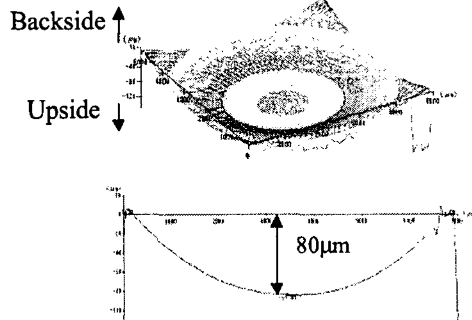
Crack of Solder Joints

Crack of solder joint



Cause

Warpage of the chip



Height change along a diagonal line of the chip

The result of 3-Dimensional measurement

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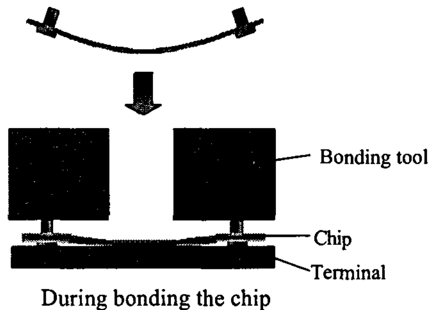
The cause of warpage

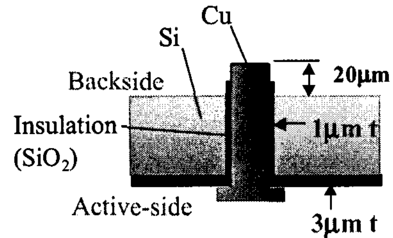
Why the crack occurred?



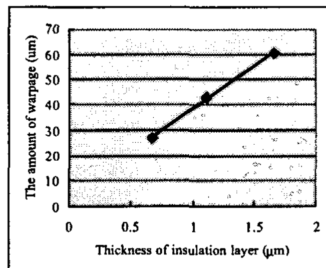
After bonding the chip

A force caused by the reaction of the deformation

Insulation on the surface of the chip



Relation between insulation thickness and warpage



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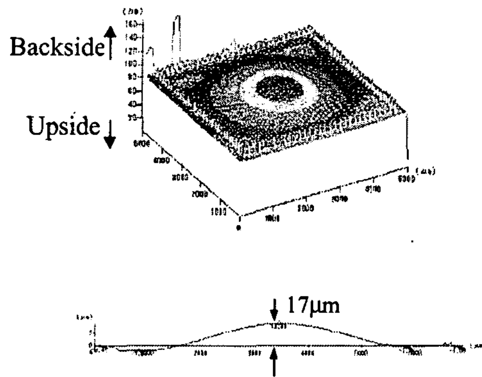
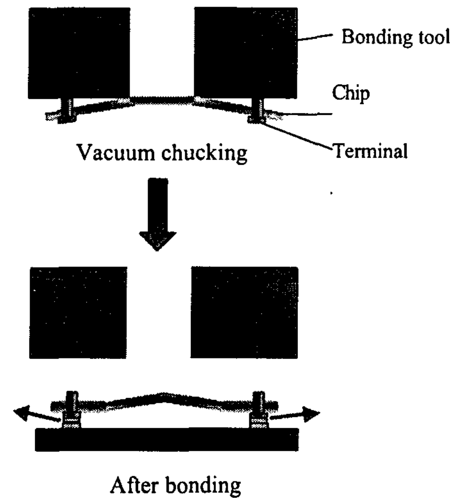
Effect of Vacuum Chucking

Warpage of bonded chips **Effect of vacuum chucking**





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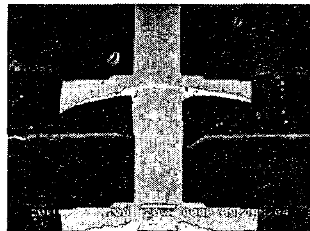
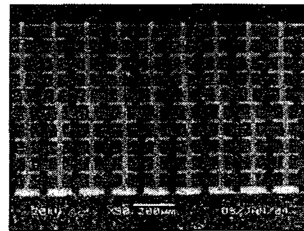
Summary of the Section





Problems	Causes	Measures
Solder Drop	Shortage of constraints of melting solder	Cu exposition on on the sidewall of the backside bumps
Crack of solder joints	Warpage of chips	Reduction of thickness of insulation on the surface
	Vacuum Chucking	Elimination of vacuum chucking during bonding

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4. Performance

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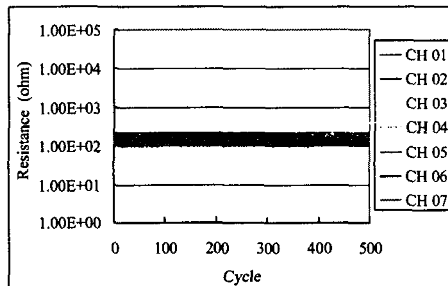
Thermal Cycle Test

Test Condition	-55↔125degrees
	Period 40 min
Result	No failures after 500cycles (n=14)

Specimen

Package	
The number of layer	4
Material of Substrate	Ceramics
The number of specimens	7
2 types of resin evaluated	

Transition of resistance



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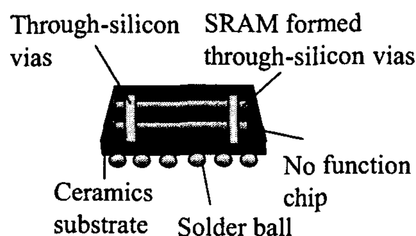
Verification of Normal Operation

SRAM Package

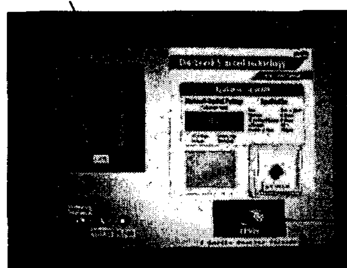


Specification

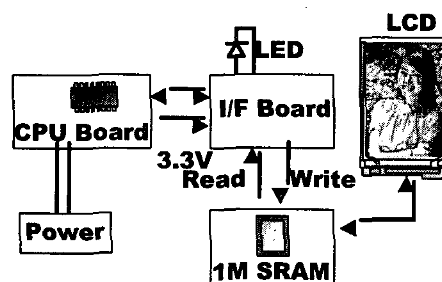
Package	
Size	7mm x 8mm
I/O Count	48
Ball pitch	0.75mm
Number of layer	2
IC	
Size	6mm x 7mm
I/O Count	48
Thickness	0.05mm

Apparatus

LCD



SRAM



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5. Conclusions

- Simple process flow was realized with the modification of structure of back side terminals.
- Cu exposure on the sidewall of backside terminals was essential to prevent solder from dropping.
- Decreasing the deformation of chips during bonding was essential. Following measures are effective.
  Reduction of the thickness of insulation layer
  Eliminating vacuum chucking during bonding
- Good thermal cycle performance was verified.
- Normal operation was confirmed by using SRAM where through –Si vias were formed.

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Thank you for your attention