Novel Packaging Technologies for System in Package Devices

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ISMP 2005

Novel Packaging Technologies for System in Package Devices

Nagano Institute of Technology
IMAPS Japan
IMAPS Asia

S.Denda

Sept. 28, 2005 in Seoul

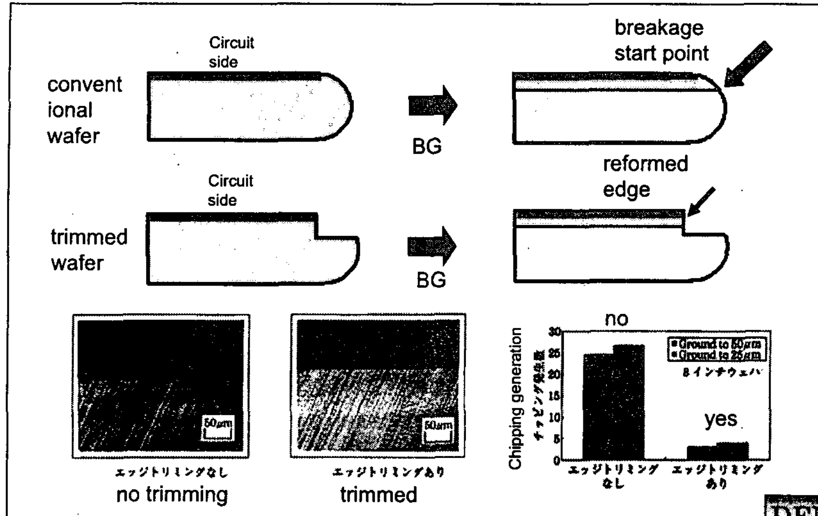
Recent Technological Topics for SiP developed in Japan

- Thin silicon wafer and chip technologies
  Dicing, Die pickup, Die bonding, Die bond film, Wire bonding
- Silicon substrate through hole technology
- Ink jet printer with nanopaste for wiring and stack substrate
- Simultaneous stacking multilayer substrate
- Device embedded substrates
- High dielectric constant ceramic film forming
- Surface flatness obtained by bump milling

Edge Trimming for thin wafers

Wafer edge protection at backgrinding

Disco

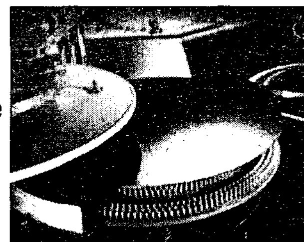


DENDA PRESENTATION

Removal of damaged layer (stress relief) by mechanical polishing

> Stress relief by plasma and wet etching are expensive
> Chips down to 50 μ thick, polishing may be a solution

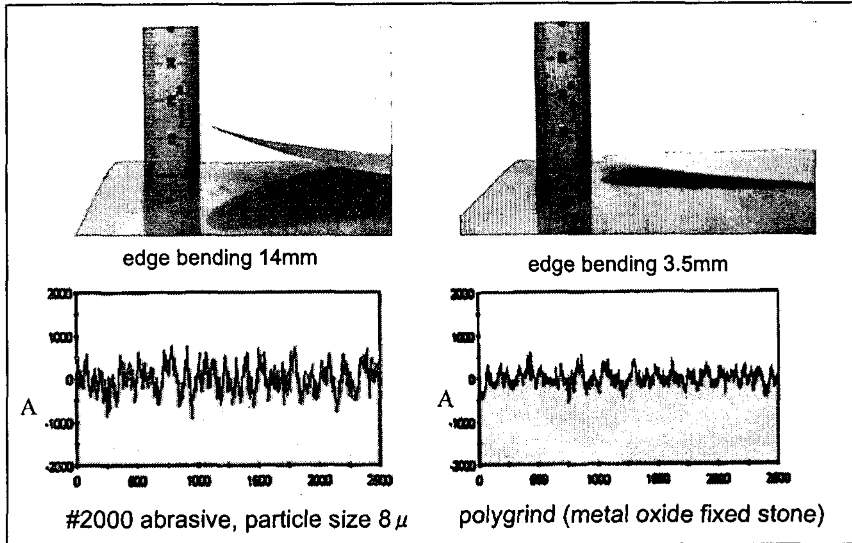
- O Dry polishing with ultra fine dry abrasive powder (Disco)
- O Polish grinder in wet system (Tokyo Seimitsu)
- O Polygrind by fixed abrasive stone (Disco)
- O Chemical-mechanical polishing (CMP), (Okamoto)
- O Step grinding, (Nippei)



(Disco)

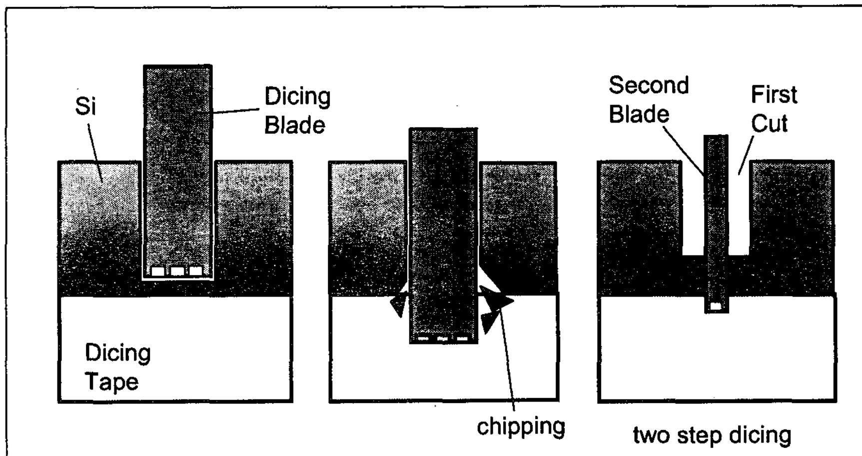
DENDA PRESENTATION

Polygrind by fixed abrasive (Disco)



Stepcut dicing to reduce chipping

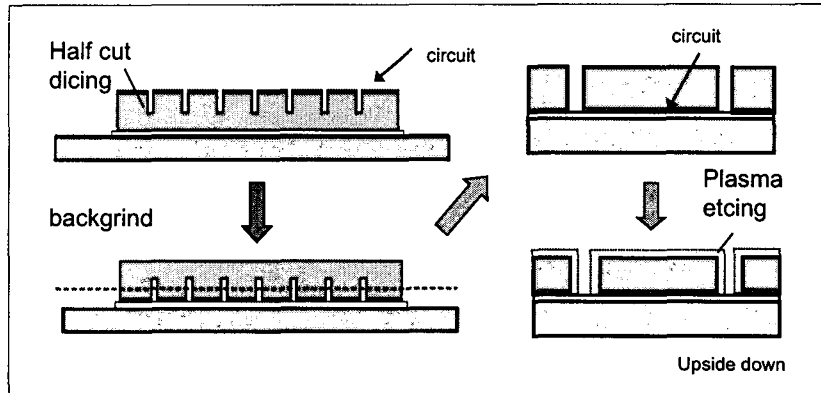
Disco



Higher cutting rate and larger residual stress will make more chippings

Dicing before grinding (DBG) with plasma

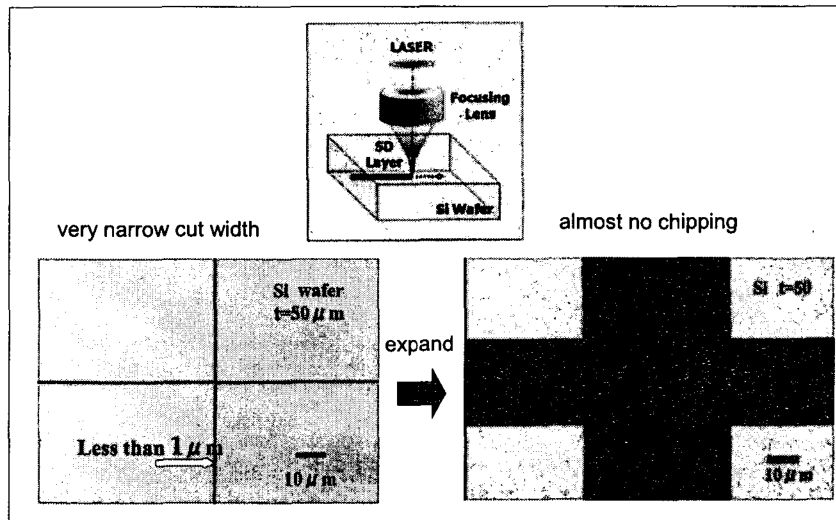
Chip side wall can be etched off by plasma (Toshiba-Disco-Lintec)



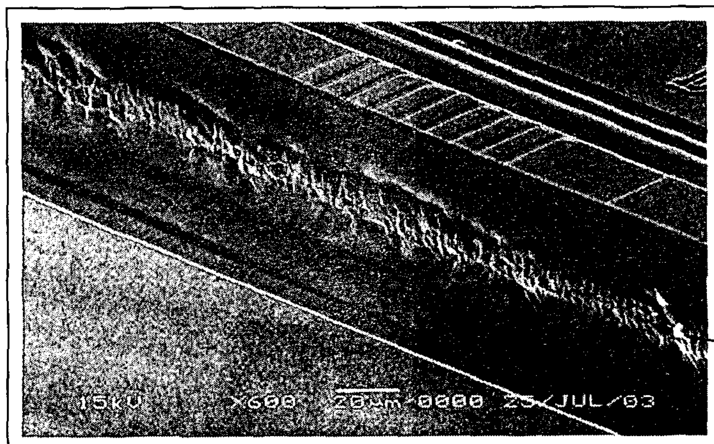
Simultaneous cutting DAF ?

Laser breaking (stealth dicing)

Hamamatsu and Tokyo Seimitsu

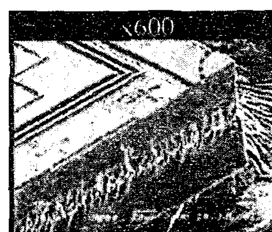


Laser broken chip cross section

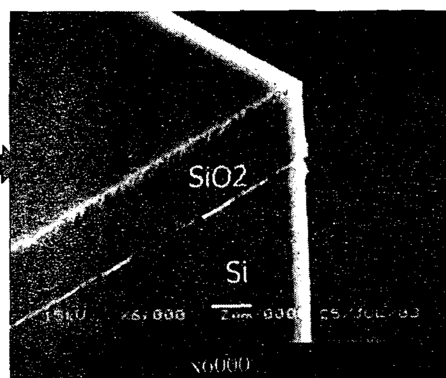


modified layer

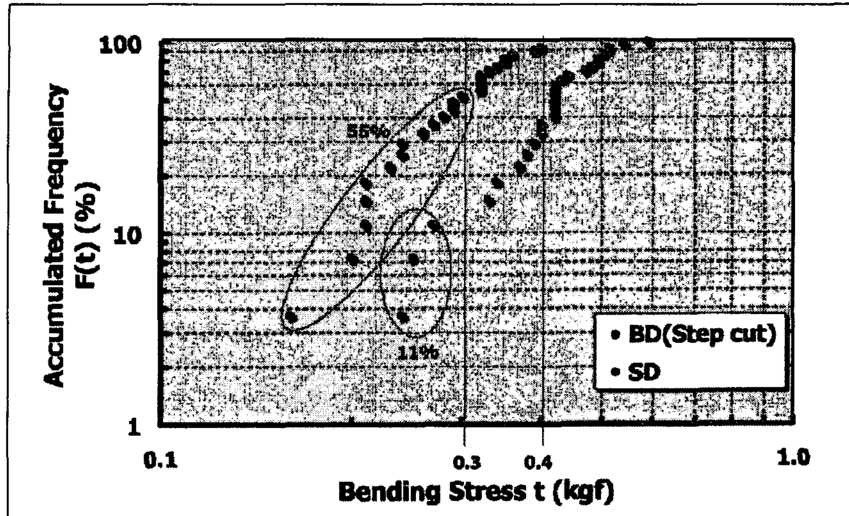
Surface SiO2 in laser break



Low-K films is also cut

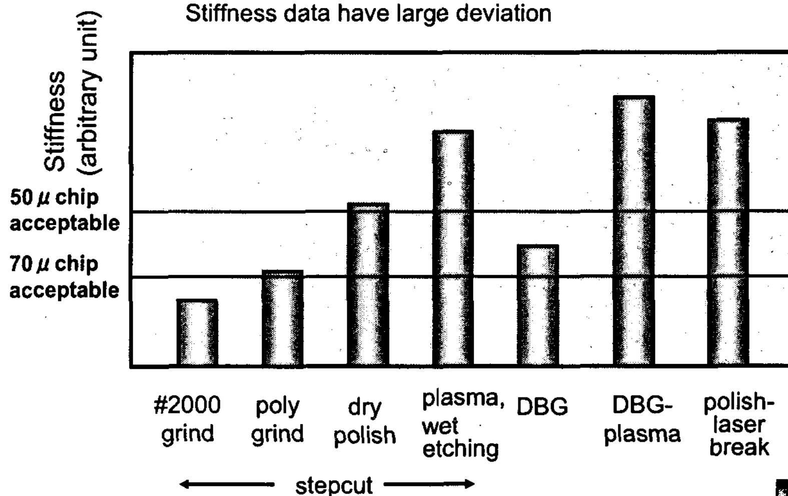


Chip stiffness comparison, blade dicing and laser break



Qualitative chip stiffness by various treatment

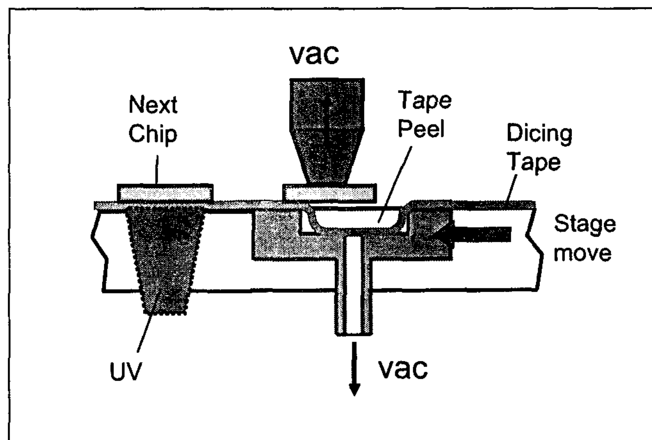
Chip stiffness measurement by 3 point method
Stiffness data have large deviation



Needleless thin die pickup

NEC Machinery

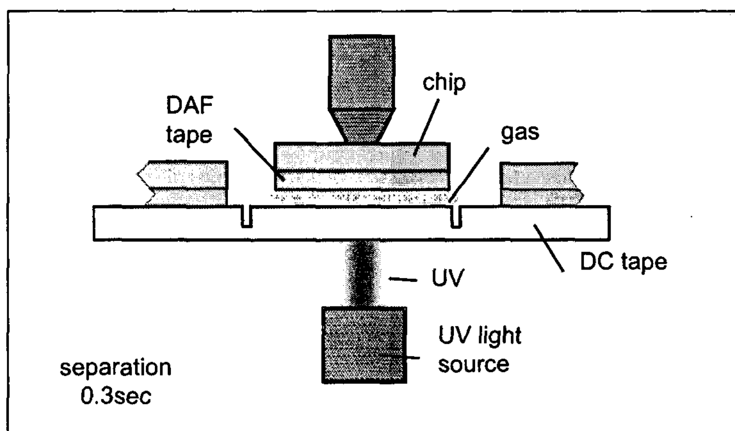
Vacuum suction, tape peel off



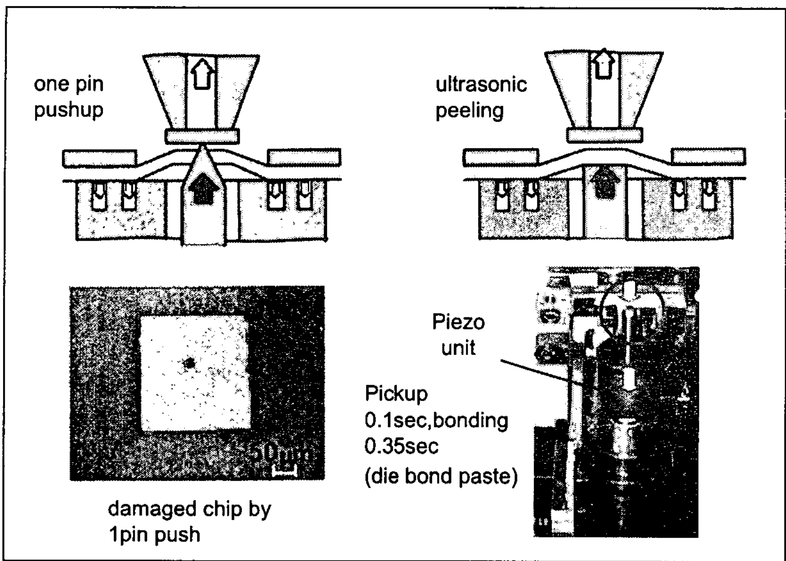
20 μ thick chip possible, 0.39 sec/chip

Chip float by gas generation with UV

Sekisui

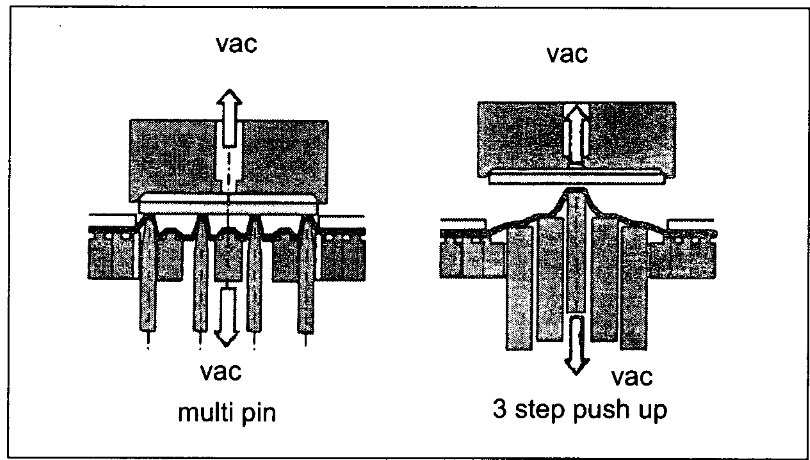


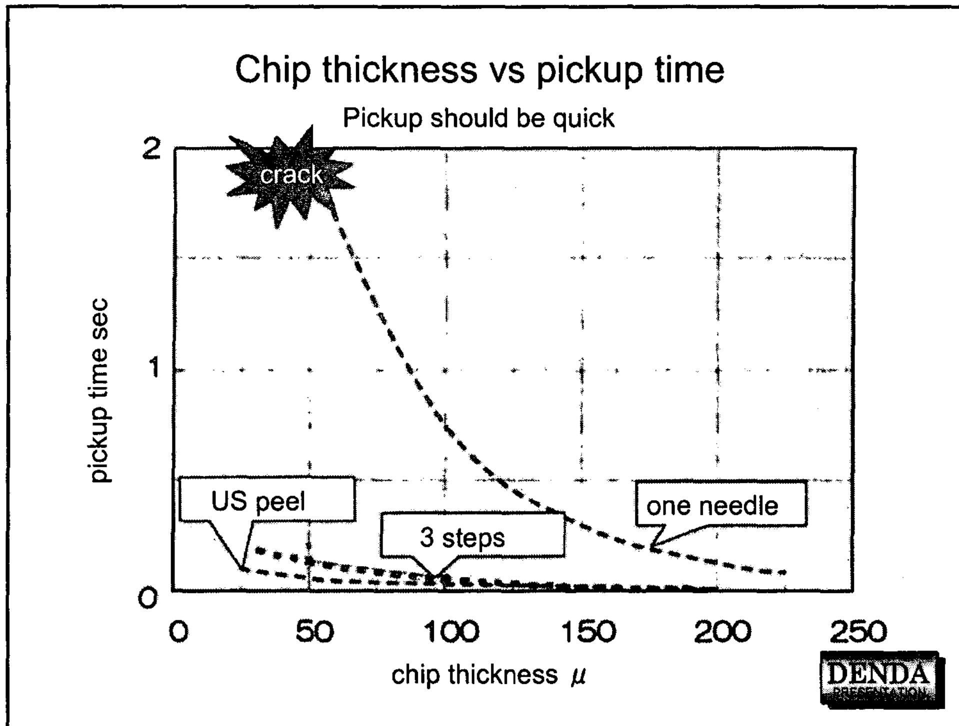
DC Tape remove by ultrasonic (Renesas)

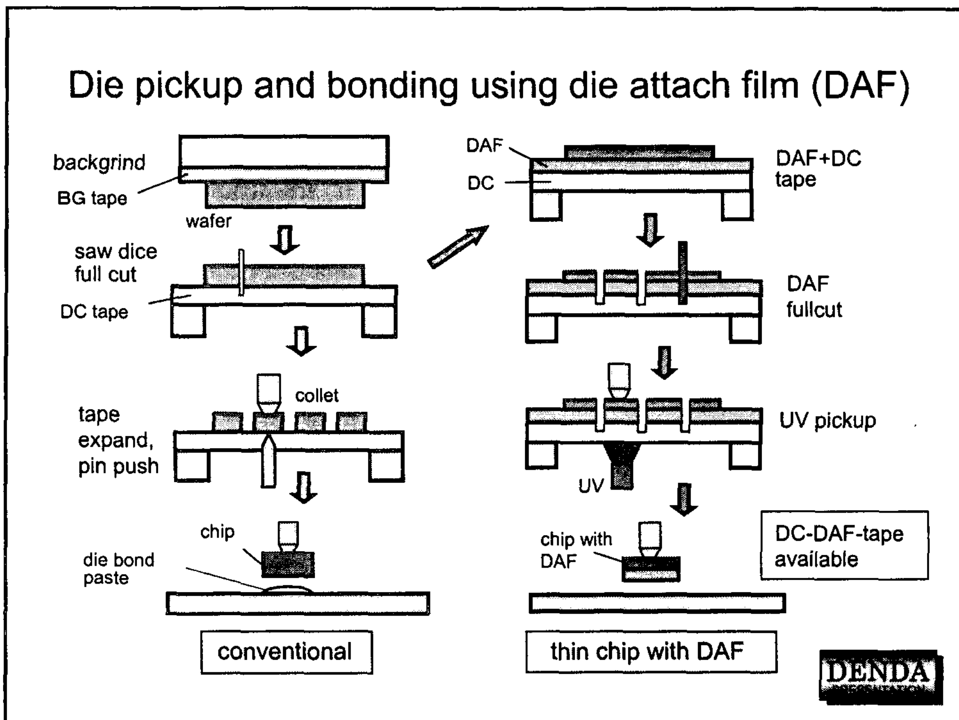


Multi-pin push in die pickup

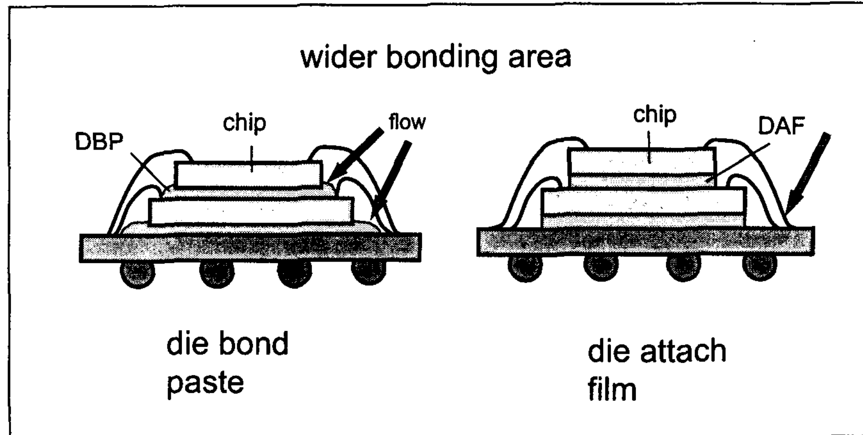
Renesas




Chip thickness vs pickup time
Pickup should be quick
crack
pickup time sec
2
1
0
US peel
3 steps
one needle
0
50
100
150
200
250
chip thickness μ
DENDA


Die pickup and bonding using die attach film (DAF)
backgrind
BG tape
wafer
saw dice
full cut
DC tape
tape
expand,
pin push
collet
chip
die bond
paste
conventional
DAF
DC
DAF+DC
tape
DAF
fullcut
UV pickup
UV
chip with
DAF
DC-DAF-tape
available
thin chip with DAF
DENDA

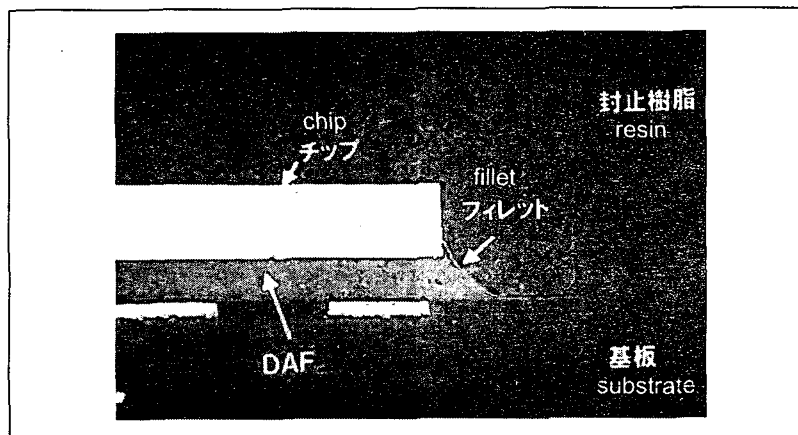
DAF advantage for chip stack devices



DENDA PRESENTATION

Better DAF for bottom chip bonding

need of adhesion strength and controlled flow Sekisui

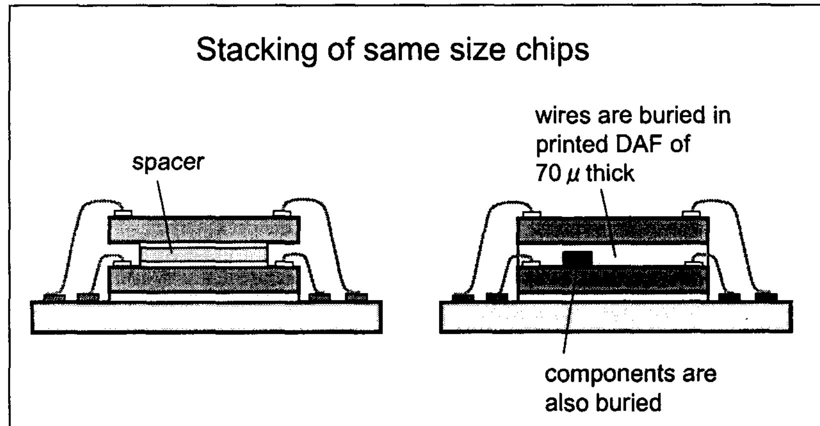


Temp and pressure must be controlled for good fillet shape

DENDA PRESENTATION

Components and wires buried in soft DAF, VSP

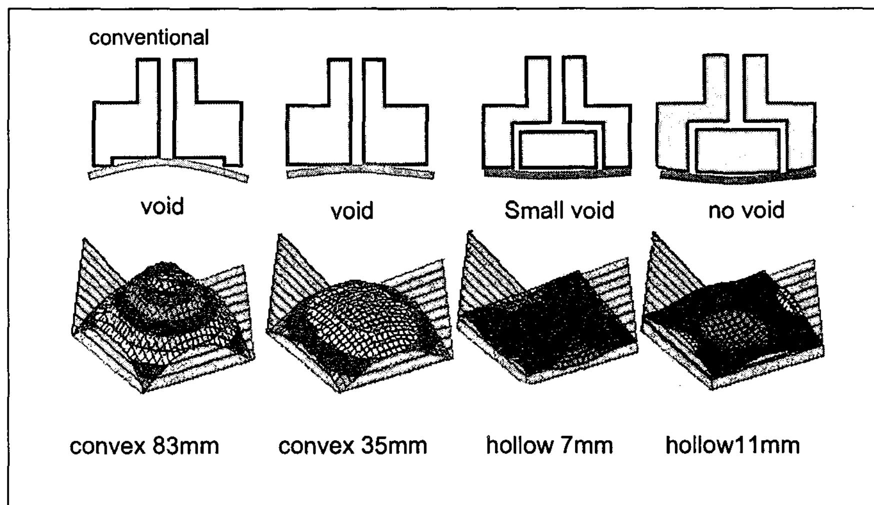
(SiP Conthortium, Hitachi Chemical)



SiPF 2005

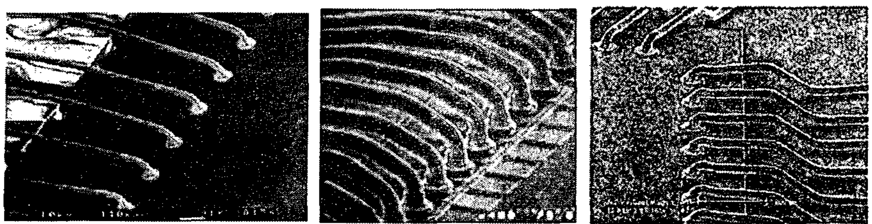
Void formation depending on collet shape

Simulation



NEC machinery, Semicon 2004

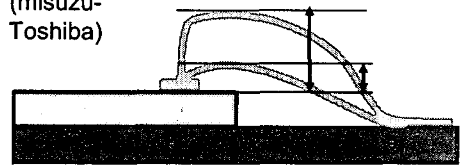
Low loop wire bonding



110 μ loop (misuzu-Toshiba)

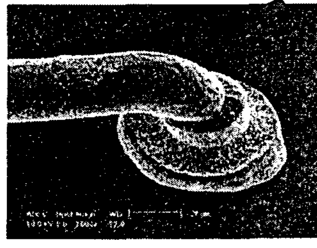
90 μ (Renesus)

Shinko



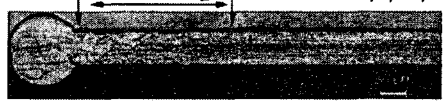
Conventional 300 μ

Strengthened Au bonding wire

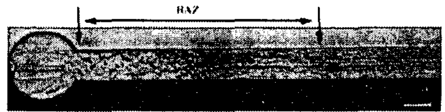


recrystallized zone at neck, stress accumulated

heat annealed zone, 25 μ ,50 μ ball



high strength

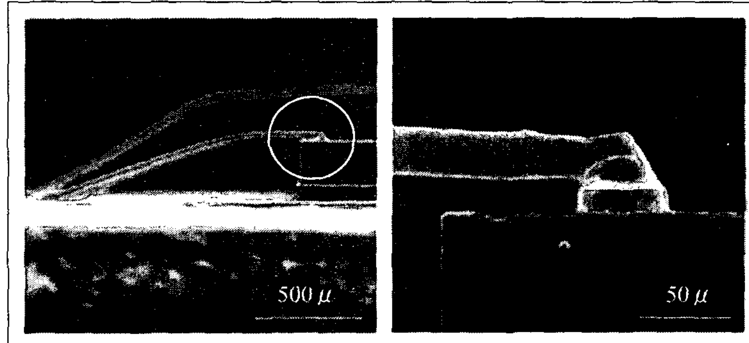


conventional

0.01% metal added to increase hardness

Very low loop wire bonding, 50 μ

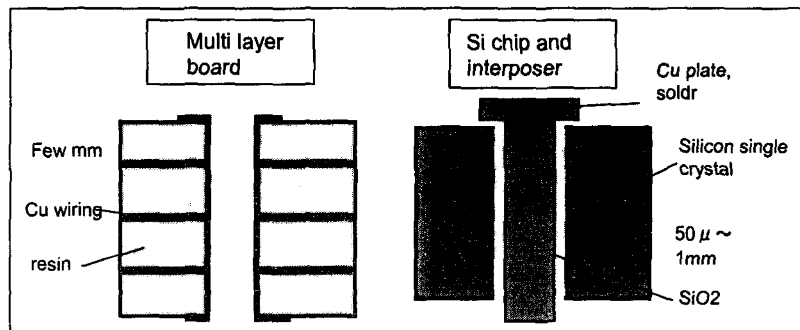
Shinkawa



forward bonding (reverse bonding, long TAT)

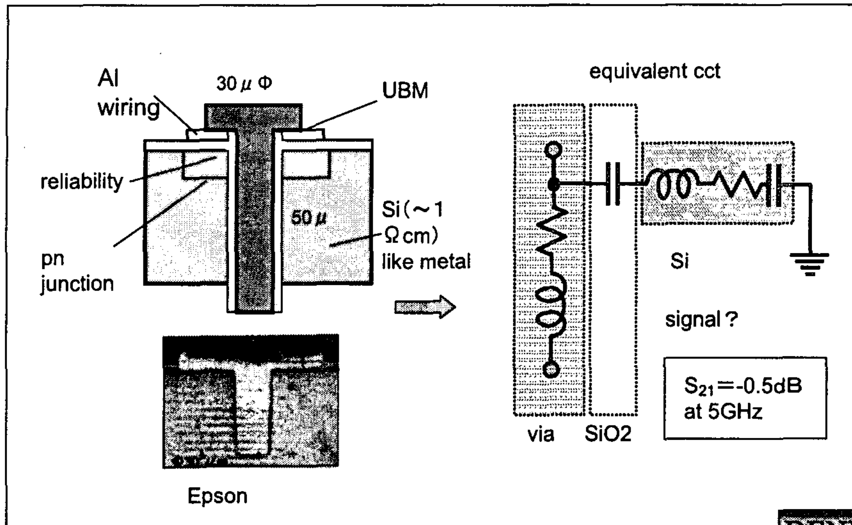
EJ 2005-3

Silicon through hole-basic concept



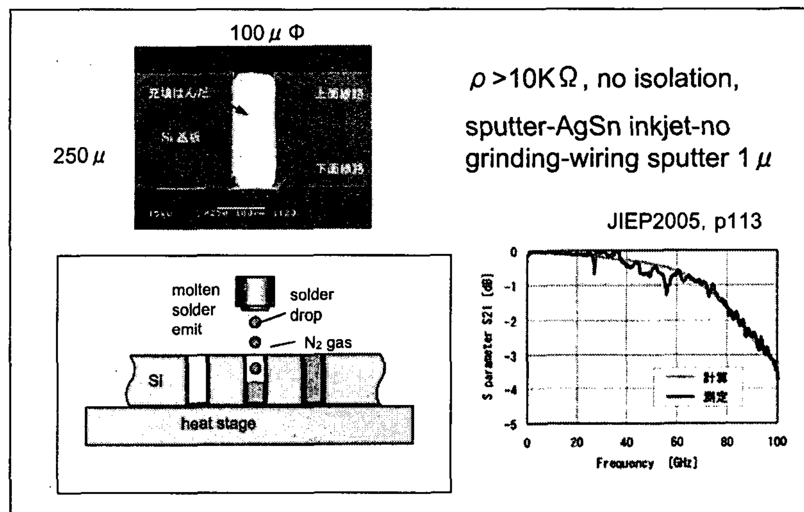
Silicon through hole	temperature-400℃ low thermal expansion, Si, 4ppm insulation SiO_2, few MΩ machinability 5 μ small size 50 μ good for HF, low L

Problems of through hole in working silicon

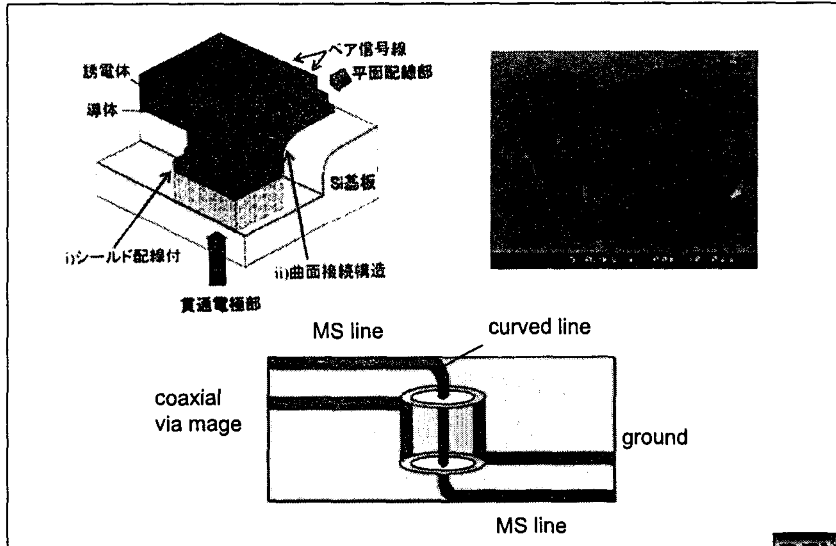


Solder filled silicon interposer with high resistivity Si

Mitsubishi

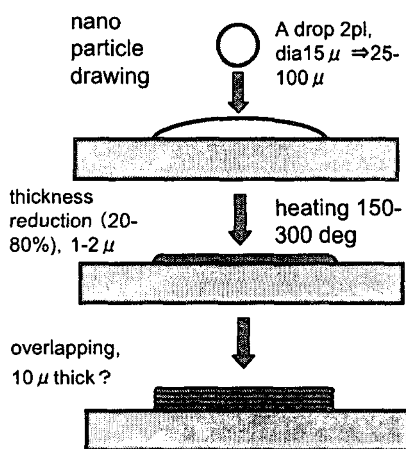


Coaxial silicon via (Sharp, Tohoku U)



JIEP 2005, p117

Width and thickness of metal wiring made by ink jet printing



consideration

- Nano particles (Ag,Au) 5nm-15nm
- Nono particle concentration:30-62%
- Ink viscosity:5-20mPa.s
- Industrial piezo IJ printer:
- Diameter depends on surface treatment

typical 15-30μ dia, 1-9μ thick

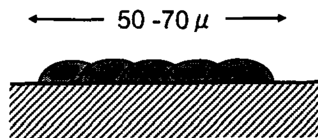
Multi-dot wiring on organic substrate

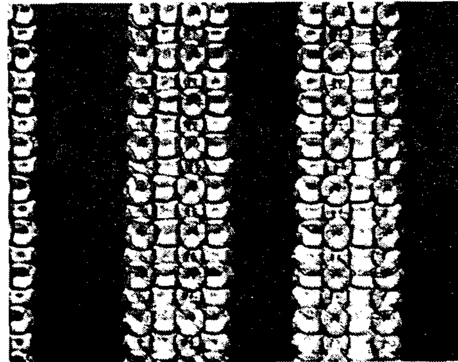
(Harima)

Au,Ag nano particles are 3-7 μ

multi-dot printing widen line width

line thickness 1-2 μ,



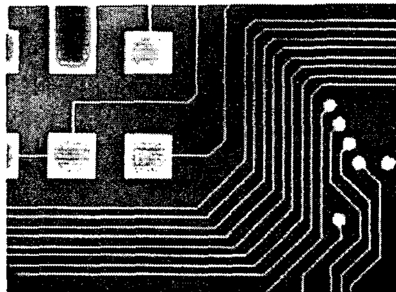


Width 70 μ, single dot 18 μ ?

MES 2004, p189

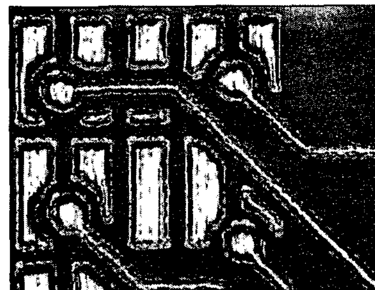
Circuit patterns by inkjet printing

multidot



Harima, width 70 μ, ρ =3 Ω cm

singledot

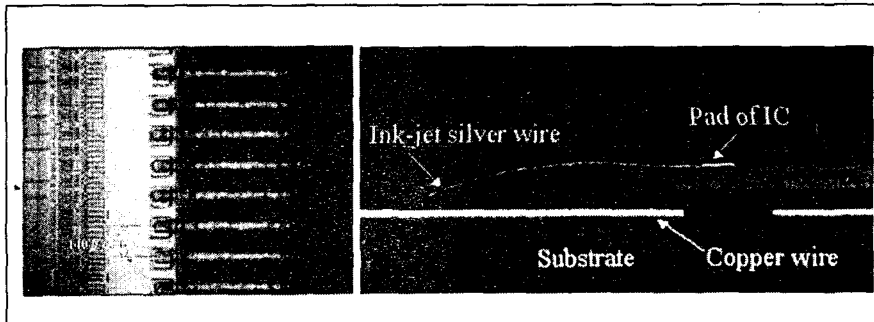


Epson, width min 30 μ, 1-9 μ thick

MES2004, MJF2005

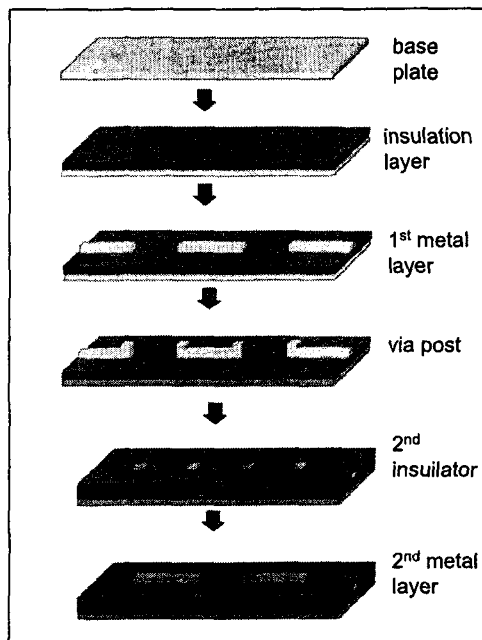
Chip electrodes sloped connection by inkjet printing

Epson



ICEP 2005, NJF2005

Chip 60 μ thick, slope is coated by IJ epoxy, IJ Ag wiring between electrodes (10 μ Ωcm) are made



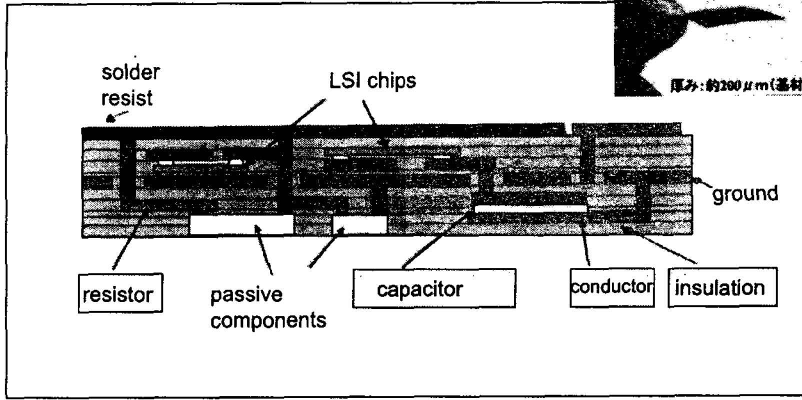
Multilayer stacking substrate made by Inkjet technology

Epson

Proposed all inkjet multilayer SiP

Epson

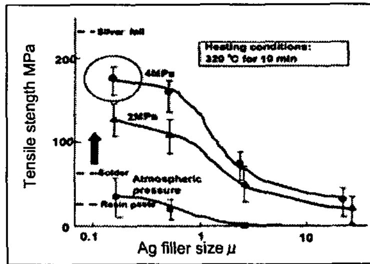
Conductor, insulator, resistors are made by inkjet technology, 20 layers in 20 μ thick



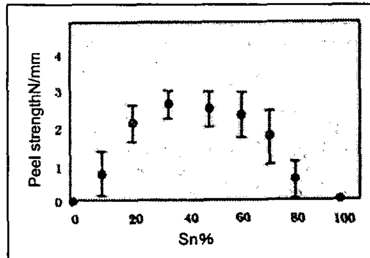
NJF2005

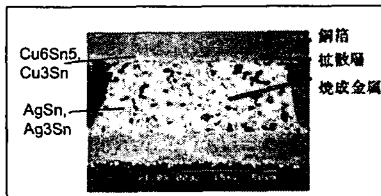
Simultaneous stacking substrate with low temp solid diffusion junction

Denso, Mitsubishi



PEEK thermoplastic with inorganic filler, 260deg.
Laser via, Ag-Snpaste
320deg. 4MPa, 10min.hotpress
All IVH
Short TAT, good HF characteristic

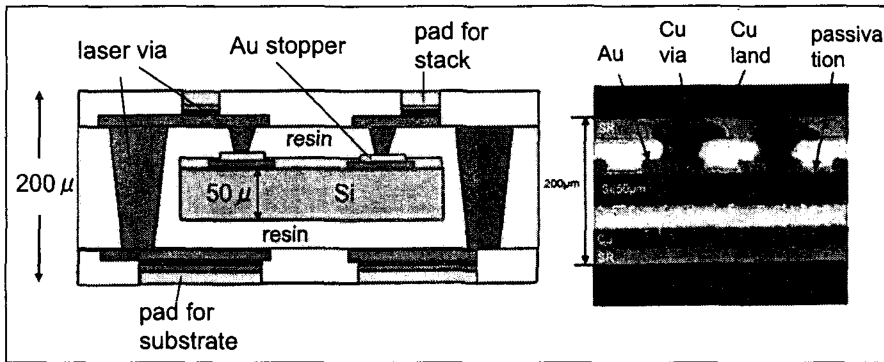




JIEP2005, JPCA2005,MES2004,

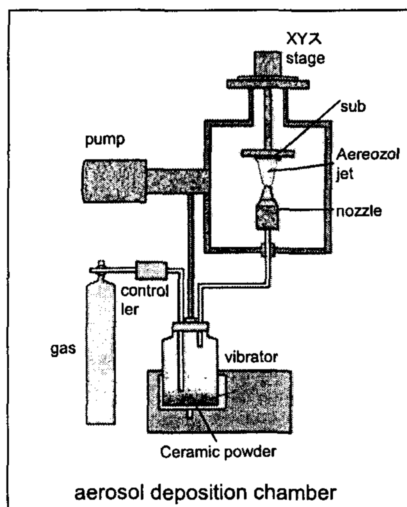
Device embedded thin substrate

Shinko



Aerosol deposition method for high ε ceramic material

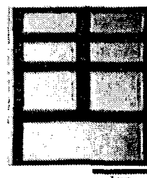
Fujitsu, AIST

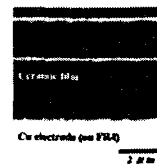


aerosol deposition chamber

- Impact solidification of ceramic film
- Reduced pressure (O_2) (300Pa)
- BaTiO3 size 0.05-2μ
- 100-1000m/s acceleration
- 1-5μ on FR-4
- Ε=400, density 300nF/cm2
- Cr-Cu electrodes
- For embedded capacitor

Plastic ε ~50 TF~100

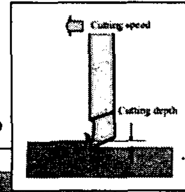


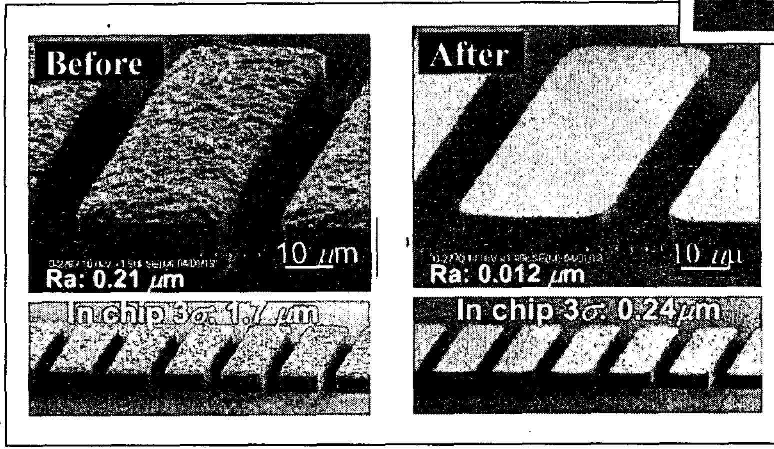


JIEP 2005,p193

Planerization of Au bumps by mechanical milling

Fujitsu-Disco





Planerized bump bonding with low pressure and at low temperature