

Development of an RSFQ 4-bit ALU

J. Y. Kim^{*,a}, S. H. Baek^a, S. H. Kim^a, K. R. Jung^b,
H. Y. Lim^b, J. H. Park^b, J. H. Kang^a, T. S. Han^b

^a *University of Incheon, Incheon, Korea*

^b *Korea Photonics Technology Institute, Kwangju, Korea*

We have developed and tested an RSFQ 4-bit Arithmetic Logic Unit (ALU) based on half adder cells and dc switches. ALU is a core element of a computer processor that performs arithmetic and logic operations on the operands in computer instruction words. The designed ALU had limited operation functions of OR, AND, XOR, and ADD. It had a pipeline structure. We have simulated the circuit by using Josephson circuit simulation tools in order to reduce the timing problem, and confirmed the correct operation of the designed ALU. We used simulation tools of XIC, WRSPICE, and Julia. The fabricated 4-bit ALU circuit had a size of $3000\mu\text{m} \times 1500\mu\text{m}$, and test chip size was $5\text{mm} \times 5\text{mm}$. The test bandwidth was 100 kHz and 5 GHz. For high-speed tests, we used an eye-diagram technique. Our 4-bit ALU operated correctly up to 5GHz clock frequency. The chip was tested at the liquid-helium temperature.

keywords : single, flux, quantum, arithmetic, logic, superconductivity, digital