An Operating Frequency Independent Energy Measurement Technique for High Speed Microprocessors

Krerkchai Thongnoo*, and Kusumal Changtong**

*Department of Electrical Engineering, Faculty of Engineering
Prince of Songkla University, Hat Yai, Songkla, Thailand 90112
(Tel : 66-7421-2894; E-mail: krerk@ratree.psu.ac.th)
**Department of Electrical Engineering, Faculty of Engineering
Prince of Songkla University, Hat Yai, Songkla, Thailand 90112
(Tel : 66-7421-2894; E-mail: chkusuma@ratree.psu.ac.th)

Abstract: This paper proposes a more accurate task level energy measurement technique for high speed microprocessors. The technique is based on the relationship of the amount of current consumed by the microprocessor and the pulse width of the power supply controller chip, employed in the synchronous buck DC-DC converter in the microprocessor's power supply. The accuracy of the measurement is accomplished by measuring variation in pulse width in each power supply cycle. The major advantage of this technique is that its accuracy does not depend on the operating frequency of the microprocessor.

To prove the proposed technique, we implemented the measurement unit of the microprocessor energy meter using an FPGA chip operating at 50 MHz. Both static and dynamic load measurement are tested in order to obtain some behaviours. Moreover, various commercially available mainboards which employ synchronous buck regulators at 200 KHz switching frequency, were measured. The results agree with previous works with better accuracy at higher operating frequency.

Keywords: task-level energy profiler, energy measurement, synchronous buck regulator, FPGA

1. INTRODUCTION

Advancement in microelectronics has stimulated the production of high performance microprocessors which consist of millions of transistors, and operating at speed over 2 GHz. At full speed of operation the microprocessors consume large amount of electrical power depending on operating frequency and operating voltage. For low computing demand, the power consumption can be reduced by lowering operating frequency and operating voltage. Combination of these frequencies and voltages leads to power states where the energy to the microprocessors is controlled. In order to set the microprocessors into different power states, the energy profile of each task must be known.

In previous works, the amount of energy consumed by any task is either simulated or measured in various ways. For direct measurement [1], microprocessor current is measured and the energy is calculated with an assumption that the microprocessor supply voltage is fixed. On the other hand, indirect measurement relies on some microprocessor's activity counters. Bellosa [2] proposed energy accounting using CPU specific performance counters. These counters count number of microprocessor's main activities which somewhat consume energy. The amount of energy in this case is formulated from these counter values. However, the actual energy must be calibrated with the direct measurement technique. In practice, current measurement is getting harder as new microprocessors operate at higher frequency and draw higher current.

Flinn et al. [3] measured the power consumption using read values from high precision digital multimeter, HP3458a. There are limitations on both the inadequate sampling rate and the small integration time of the instrument used. These limitations will lead to low accuracy power measurement when processors operate at higher frequencies. The energy consumption was measured in [4] by integrating the current sensed from a small resistor. The accuracy of this measurement technique relies on the frequency response of voltage to current converter and an RC integrator. Thus both methods face the same limitations when processors operate at high frequencies.

In this paper, a more accurate task level energy measurement technique for high speed microprocessors with operating frequency independence is proposed. The equations showing the relationship between amount of current consumed by the microprocessor and pulse width of the power supply controller chip is illustrated in section 2. Moreover, the frequency independent of the processor is shown in the energy profile expression. In Section 3, an implemented measurement unit using an FPGA chip is explained. Test results of various loads and mainboards are finally shown in Section 4.

2. OPERATING FREQUENCY INDEPENDENT TECHNIQUE

2.1 Current Measurement

A basic buck converter shown in Figure 1 consists of an unregulated DC input voltage V_g, switch network S_1 and S_2, and an LC low-pass filter. A regulated DC output voltage supplies load current via R. The output voltage V is equal to the DC input voltage V_g when S_1 is turned on, and is equal to zero when S_2 is turned on. The duty ratio D is the faction of time that the switch S_1 turns on. The average output voltage V is equal to the duty ratio times the dc input voltage V_g

$$V = DV_g, \qquad (1)$$

Typically, S_1 is replaced by a MOS transistor while S_2 may be implemented using a free wheeling diode for a regular buck converter or a MOS transistor for a synchronous buck converter.

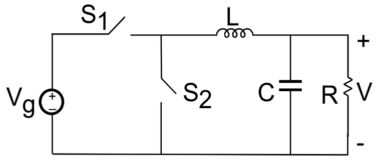

Figure 1 A basic buck converter

In Figure 2, for more accuracy of current measurement, a nonideal synchronous buck converter is considered including a R_L resistor in series with the inductor and R_{s1} and R_{s2} resistors when swtiching devices S_1 and S_2 turn on respectively. Figure 2(a) shows the equivalent circuit when S_1 conducts. The inductor voltage in this interval, by using small ripple approximation, is equal to $v_L(t) = V_g\text{-}V\text{-}I_LR_L\text{-}I_LR_{s1}$. Like wise, the capacitor current is equal to $i_c(t) = I_L\text{-}\ V/R_L$. When S_2 conducts, the equivalent circuit is illustrated in Figure 2(b). In this interval, the inductor voltage is approximately equal to $v_L(t) = \text{-}V\text{-}I_LR_L\text{-}I_LR_{s2}$ while the capacitor current is equal to $i_c(t) = I_L\text{-}\ V/R_L$.

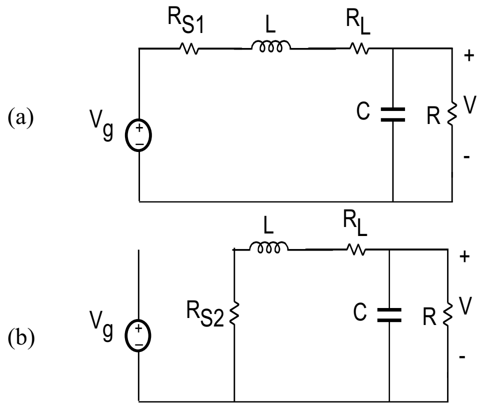

Figure 2 The equivalent circuit of a buck converter, (a) when S_1 conducts, (b) when S_2 conducts

After the inductor volt-second balance and capacitor charge balance are applied as well as the turn-on resistances of switching devices are assumed to be identical, the output voltage and the load current can be expressed as

$$V = DV_g\left[\frac{R}{R+R_L+R_S}\right], \qquad (2)$$

$$I_L = DV_g\left[\frac{1}{R+R_L+R_S}\right] \qquad (3)$$

A relationship between the duty ratio and the output current I_L is given as

$$D = \left[\frac{V+I_L(R_L+R_S)}{V_g}\right] \qquad (4)$$

2.2 Power Measurement and Energy Profile

The energy consumed by a microprocessor for an interval of interested is described as

$$E = \int^{T} Vi(t)dt \qquad (5)$$

With the assumption that V is controlled within an acceptable limit in each converter cycle, the energy consumption in (5) can be expressed as

$$E = KV\,((P_{w1}–P_{w0}) + \ldots.. + (P_{wn}–P_{w0})) \qquad (6)$$

Where P_{w0} is pulse width when $I_1 = 0$
P_{wn} is pulse with of n^{th} converter cycle
K is the conversion gain (A/s)

The energy measurement in (6) is based on the relationship of the amount of current consumed by the microprocessor and pulse width of the power supply controller chip, employed in the buck DC-DC converter in the microprocessor's power supply. Since the current is integrated during the converter cycle which may cover many microprocessor machine instructions, the energy measured is accurate over a wide operating frequency range of the microprocessor provided that a controller can regulate the output voltage and Vg from a PC power supply is fixed.

3. IMPLEMENTATION

To prove the proposed technique, we implemented the measurement unit of the microprocessor as shown in Figure 3. An FPGA chip operating at 50 MHz is used for the energy meter. It consists of the 8-bit power counter (PC), the 8-bit power register (PR), the 16-bit energy counter (EC), the 16-bit energy register (ER), and the interfacing circuitry for a PC's parallel port. At the beginning of a power supply cycle, when the signal across S_2 (Vx) is active, the PC starts to count the clock cycle. At the end of the on time of the power supply cycle, the content of the PC is transferred to PR, the PC is then reset. EC and ER work in the similar way except they are reset and transferred under program control. The content of PR is read by the monitoring computer every power supply cycle, while the content of ER is read at points of interest in the tested program.

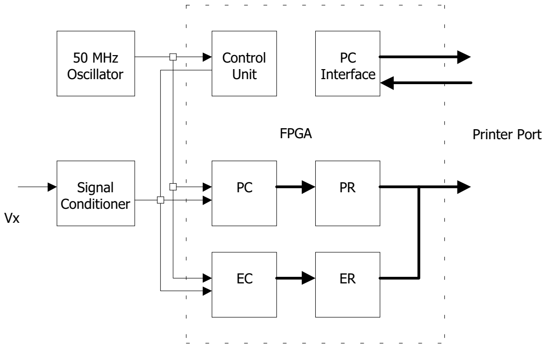

Figure 3 The simplified measurement unit

4. TEST RESULTS

In order to obtain some behaviours of this energy measurement technique, both static and dynamic load measurements were performed. For static measurement, the accuracy of this approach is comparable to the results obtained from a digital multimeter. However, the resolution is poorer due to the relatively low sampling rate of the implemented pulse measurement unit. Moreover, there is an offset measured current at no-load measurement, as shown in Figure 4, due to the DC-DC controller characteristic.

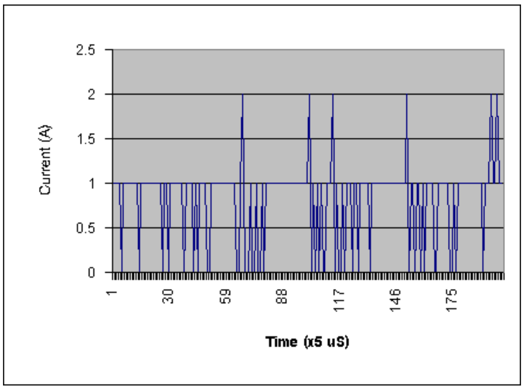

Figure 4 The no-load current profile

For a dynamic measurement, the resistive load switching was controlled to specified load patterns. Figure 5 shows the current profile of a staircase-like dynamic load. This current profile is similar but not identical compared to the current profile using a direct current measurement technique. The main reason of this difference is that the current measured using the proposed technique is the integration within the power supply cycle while the current measured using a conventional method is its instantaneous value.

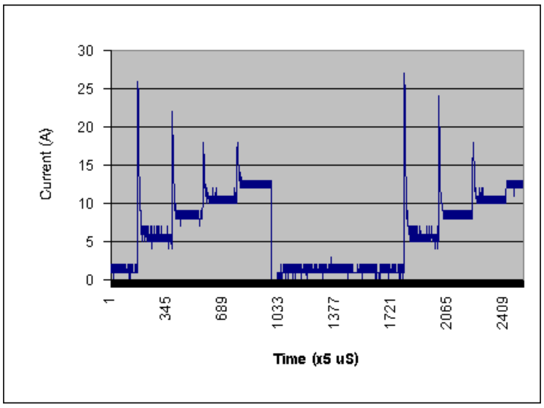

Figure 5 The current profile of a staircase load

In order to measure the abrupt change in load current similar to the load condition when a microprocessor is switched from a idle mode to an active mode, the load was programmed to switch from no load to a reasonable value as shown in Figure 6. As the switching rate of load is increased, the proposed technique is still capable of measuring the accurate profile. Moreover, various commercially available mainboards which employ synchronous buck regulators at switching frequency of 200 kHz, were measured for example AMD K6-2 at 400 MHz operating frequency. Figure 7 shows the current profile of a real-time application under uC/OS-II [5] when power saving feature was disabled. Figure 8 shows the current profile of the same program with the power saving was enabled. It is clearly seen from this profile that the significant amount of the energy is saved using the power saving feature of the uC/OS-II. However, high surge current was developed when the CPU switched from an idle mode to an active mode. Figure 9 shows the current profile of the CPU when the CPU performed disk scanning under Windows 98. The current profile is stable during some periods when the CPU was waiting the data from a hard disk.

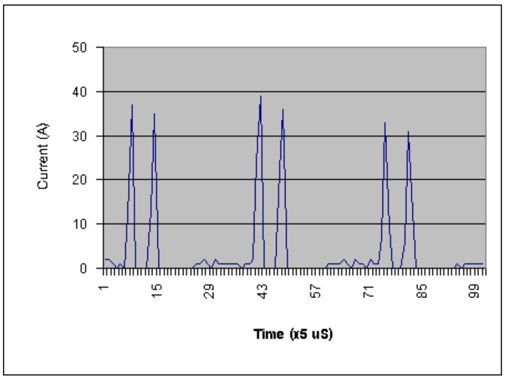

Figure 6 The current profile of abrupt change load

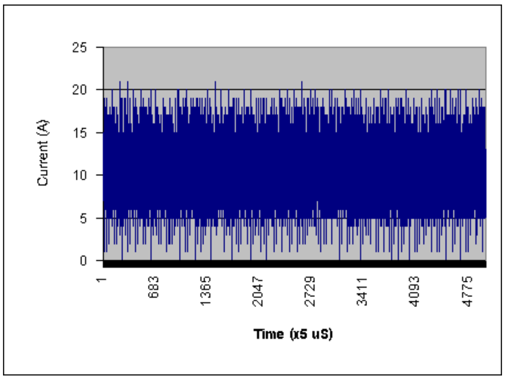

Figure 7 The current profile without power saving

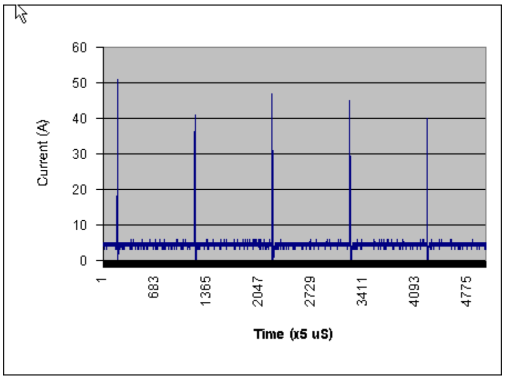

Figure 8 The current profile with power saving

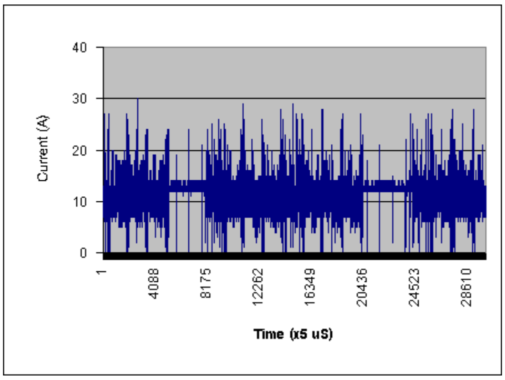

Figure 9 The current profile of disk scanning

5. DISCUSSION AND FURTHER IMPROVEMENT

Resolution

Since the current implementation of the measurement unit employs an 8-bit pulse width measurement, the resolution of the measured current of this technique is lower than the one measured using a digital multimeter which employs *n*-bit A/D converter (where *n* is greater than 8). However, this resolution would be improved by using one of following three approaches. The first approach is a time-based approach where high-speed electronics devices must be employed. Available FPGAs such as Virtex [6] families from Xilinx will increase the resolution up to four times compared to the current implementation. In the second approach, the amount of pulse width variation is increased if the supply voltage to the DC-DC converter is decreased to the proper voltage level. In this case, care must be taken to assure that the input voltage is within the DC-DC converter input voltage range during the maximum CPU current. For the last approach, the pulse-width differences between the reference pulse, the pulse width when there is no load current, and the instantaneous pulse width will be converted to an analog value for analog processing. This value will then be amplified prior to be digitized by a higher resolution A/D converter. However, this approach is more complicate and will be susceptible to switching noises in a DC-DC converter circuit.

Linearity

It can be seen from equation (4) that the linearity of this technique is dependent on Rs. Unfortunately, Rs of a typical MOSFET increases as the current between source and drain increases. This will affect the overall accuracy to some extents depending on the selection the MOSFETs, PCB layout, and the inductor. The accuracy is approaching the best value when the variation of Rs is relatively small compared to total resistance in (4). Fortunately, in current design practice the value of Rs is selected as low as possible in order to reduce the power loss in a DC-DC converter. Moreover, the variation of Rs in a typical MOSFET is relatively low within a working current range.

Temperature Dependency

As this technique depends heavily on the correctness of PCB trace resistance, inductor resistance, and turn-on resistance of switching devices, the overall measurement characteristics will suffer from temperature variation. There are two approaches to reduce this degradation. The first approach relies on selection of low temperature coefficient parts such as MOSFETs and inductors. The second relies on the measurement procedure, the DC-DC converter should be temperature stabilized prior to the measurement. Fortunately, for a typical task-level energy measurement, the measurement time is relatively short that the temperature rise cannot be noticed.

6. CONCLUSION

An operating frequency independent energy measurement technique for high speed microprocessors is proposed. The technique is based on the relationship between the microprocessor current consumption and the variation of pulse widths in a synchronous buck DC-DC converter. As the current is integrated during the converter cycle which may cover many microprocessor machine instructions, the energy measured is accurate over a wide operating frequency range of the microprocessor. The prototype implementation together with the test results are detailed. The results agree with previous works with better accuracy at higher operating frequency.

REFERENCES

[1] M. Viredaz and D. Wallach, Power Evaluation of Itsy Version 2.4, *Technical Report Technical Note TN-59,* Compaq Western Research Laboratory, February 2001.

[2] F. Bellosa, "The benefits of event-driven energy accounting in power-sensitive systems*", Proceedings of the 9th ACM SIGOPS European Workshop*, Kolding, Denmark, September 2000.

[3] J. Flinn and M. Satyanarayanan, "PowerScope: A Tool for Profiling the Energy Usage of Mobile Applications*", 2nd IEEE Workshop on Mobile Comp. Syst. and Apps.,* pp. 2–10, New Orleans, LA, Feb. 1999.

[4] F. Chang, K. Farkas, and P. Ranganathan, Energy-driven Statistical Sampling: Detecting Software Hotspots, *Compaq Western Research Laboratory Research Report 2002/1,* March 2002

[5] J. J. Labrosse, *MicroC/OS-II.* R & D Books, Lawrence, KS, 1998.

[6] Xilinx Corp., Virtex 2.5 V Field Programmable Gate Arrays datasheet , *DS003-1 (v2.5) April 2, 2001*