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High-speed turbo decoding algorithm and its implementation

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Abstract

In this paper, we propose a high speed turbo decoding algorithm and present results of its implementation. The latency caused by (de)interleaving and iterative decoding in conventional MAP turbo decoder can be dramatically reduced with the proposed scheme. The main cause of the time reduction is to use radix-4, center to top, and parallel decoding algorithm. The reduced latency makes it possible to use turbo decoder as a FEC scheme in the real time wireless communication services. However the proposed scheme costs slight degradation in BER performance because the effective interleaver size in radix-4 is reduced to an half of that in conventional method. To ensure the time reduction, we implemented the proposed scheme on a FPGA chip and compared with conventional one in terms of decoding speed. The decoding speed of the proposed scheme is faster than conventional one at least by 5 times for a single iteration of turbo decoding.

I Introduction

In satellite communications and 3rd generation mobile communication system, turbo codes are adopted for high speed data transmission. Recently, the trend of wireless communication is changed from the conventional narrow band voice service to the wide band multimedia service. Therefore, it is highly required to develop the high speed turbo decoder. The important problems of high speed applications of turbo decoder are decoding delay and computational complexity. To solve the problem with latency of turbo decoder, two types of decoding algorithms are proposed in the paper. The first type is radix-4 decoding algorithm. The previous state at $t = k - 2$ going forwards to a current state at $t = k$ and the reverse state at $t = k + 2$ going backwards from a current. Time interval from $t = k - 2$ to $t = k$ is merged into $t = k$. Therefore, we can decode two bits source data at the same time without performance degradation. And we may reduce the block size buffered in memory. In order to apply the radix-4 algorithm, we have derived the branch metric (BM), forward state metric (FSM), α, backward state metric (BSM), β, and log likelihood ratio (LLR), λ. Another type is center to top algorithm. In conventional scheme, to calculate the LLR, decoder must wait for until finishing the BSM (or FSM) calculations. But center to top method doesn't need to wait. Decoder calculates FSM (left to right) and BSM (right to left) simultaneously. When FSM and BSM reach at same point, decoder begins to calculate the LLR.

In this paper, we combined the two types of proposed scheme and parallel decoding algorithm. The proposed scheme is desirable in designing of high speed turbo decoder because it provides significant reductions in memory requirements of the decoder, as well as allowing increased parallelism. To testify high speed decoder, we implemented the proposed scheme onto an FPGA chip (Altera FLEX10K) and compared with conventional one in terms of decoding speed. The proposed scheme is demonstrated in a 4 states, R = 1/2 turbo MAP decoder.

The paper consists of the following Sections. In Section 2, we analyze the three types of high speed turbo decoding algorithm. Section 3 describes computer simulation results of new high speed turbo decoder. In Section 4, we find optimal parameters for implementation and design the high speed turbo decoder. Section 5 concludes the paper.

II High SpeedDecoding Algorithm

2.1 Scheme1 :Radix 4algorithm

Using the unified approach to state metrics, a 2^{v-1} state trellis can be iterated from time index $n-k$ to n by decomposing the trellis into 2^{v-k} subtrellises, each consisting of k iterations of a 2^k statetrellis. Each 2^k states subtrellis can be collapsed into an equivalent on stage radix 2^k trellis by applying k levels of lookahead to the recursive update. Collapsing the trellis does not affect decoder performance since there is one to one mapping between collapsed trellis and radix 2 trellis. An example of the decomposition for a four state radix 2 into an equivalent radix 4 trellis using one stage of lookahead is shown in Figure 1.(K=3 $g_1 = (7)_{octal}$, $g_2 = (5)_{octal}$ Kmeans constrain length)

(a) 4 state radix 2 trellis (b) 4 state radix 4 trellis

Figure 1 Trellis Structure