APDE(Antenna Positioning Drive Electronics) Design for MSC (Multi-Spectral Camera)

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Abstract: As a main management unit of MSC, PMU controls the MSC payload operation by issuing commands to other sub-unit and PMU internal modules. One of these main control functions is to drive the APS(Antenna Pointing System) when APS motion is required. For this purpose, SBC(Single Board Computer) for calculating motor commands and APDE for driving APM(Antenna Pointing Mechanism) by PWM signal operate inside PUM. In this paper, details on APDE design shall be described such as electronic board architecture, primary and redundant design concept, Cross-Strap, FPGA contents and latch-up immune concept, etc., which shall show good practices of electronic board design for space program.

Keywords: MSC, APS, PMU, APDE, SBC

1. Introduction

Accurate tracking of the KGS(K2 Ground Station) by the active X-Band Antenna during an X-Band Contact Transmission Pass is a requirement necessary for meeting the RF Link Budget. In order to do that, the tracking profile to be executed by the APS must be calculated in advance based on predicted S/C Orbit and Attitude parameters as function of time. For accurate tracking performance it is necessary not only to accurately predict the S/C Orbit and Attitude parameters as function of time during the X-Band Contact period, but also to establish an accurate common time-base to be used for the predictions on the ground, as well as for the actual execution of the tracking profile on-board the S/C. The XTS is a system combined of many functional blocks. Since XTS is essentially an open loop system (no real-time feedback from the ground is utilized in order to zero the pointing error), the achieved accuracy of pointing the RF beam towards the Ground Station will be totally dependent on executing an accurately defined tracking profile. The tracking profile must be calculated in advance, transmitted to the S/C in a compressed format (by polynomial approximation) as a Tracking Parameter File (TPF), then transferred from OBC to the PMU, and decompressed (by polynomial reconstruction) by the PMU, and executed by the APDE/APM servo loops as a continuous motion profile. All functions involved in these steps must be well defined, and operate within defined performance accuracies in order to obtain the required XTS performance results. In this paper, We introduce MSC electronic system, explain operational mode of XTS and then describes of the details of APDE design as a part of XTS system that is shown in Fig.1 where only MSC functional blocks are presented.

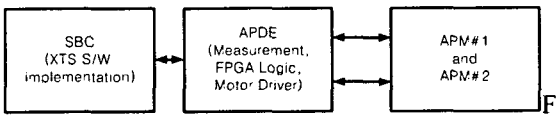

Fig. 1. XTS functional blocks in MSC

2. MSC electronic system

The MSC payload consists of EOS, PMU, PDTS(Payload Data Transmission Subsystem) and interconnection harness as shown in Fig. 2. The EOS consisting of OM(Optical Module) and CEU(Camera Electronic Unit) is to obtain data for high resolution images by converting incoming light into digital stream of pixel data. The PDTS, which comprises of the DCSU(Data Compression & Storage Unit), the CCU(Channel Coding Unit), the QTX(QPSK Transmitter), the APM(Antenna Pointing Mechanism) and Antenna, stores and transmits these digital image data to the ground station through X band antenna. The PMU, consisting of several subassemblies with an architecture that supports a cold redundancy concept, provides electrical and software interfaces between the MSC and the spacecraft, controls all the MSC subsystem by the ground station commands and reports all the SOH(State Of Health) telemetry to the spacecraft. The PMU consists of the SBC(Single Board Computer), the THTM, the NUC(Non-Uniformity Correction board), the APDE(Antenna Pointing & Driving Electronics Board) and the PSM(Power Supply Module). Especially, as the main controller of the MSC payload, the SBC provide serial communication channel to MSC external subunits and other subunits inside PMU like THTM. It also executes arriving commands from OBC, receives telemetry data from THTM and sends it to the OBC, and performs antenna control and self-test, etc. For the normal XTS operation, SBC communicates with

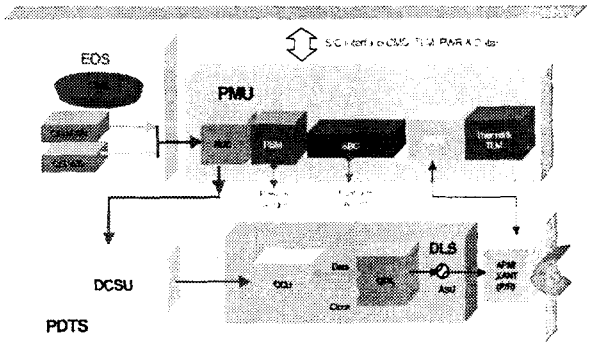

Fig. 2. MSC Block Diagram

satellite through 1553B interface for receiving control commands and responding with telemetry data, and implements S/W logic by which it controls XTS mode transition, S/C absolute time synchronization, TPF reconstruction, servo loop, BIT function. APDE gets command from SBC via RS422 serial communication for APM control in which it reads resolver data and generates PWM signal according measurement data and motor driver command from SBC.

3. Operation modes of antenna tracking S/W

The antenna tracking S/W has the 9 different operational modes-Off, Standby, Normal profile tracking, First elevation operation, First Azimuth operation, IBIT, Ground Test, In-orbit test, Parking. All APDE is powered off and APS motors are disabled in Off mode and a pre-programmed XTS test profiles in PMU servo S/W are executed in Ground Test mode in accordance with uploaded parameters with commands of EGSE. In-orbit test cause the APS to executes a tracking profiles according to uploaded parameters after launch and Parking mode commands tracking S/W to be moved to Park position(0,0) of APM. The operations in other rest modes are explained below.

1) Standby Mode

The XTS STBY Mode is a transit mode. Transition between any XTS Operational Modes is possible only by passing through STANDBY Mode and transition to STBY mode is possible from any other XTS Operational Mode (even during execution of a tracking profile, which be interrupted). And each of the XTS operational modes will automatically return to STBY Mode after successful execution or after Mode Time-out condition forcing return to STBY. In this mode the APDE circuitry is powered ON according to one of the 3 possible configurations of Default, Normal, Cross-Strapped by configuration command. In STBY mode the APDE shall disable both elevation and azimuth motor drivers, and (for additional safety) PWM="0" is commanded by the ATS s/w. Therefore no powered APS motion is possible in this mode while the APS AZ/EL angular positions (APS axes resolvers) are continuously monitored, as well as the APDE status, by appropriate TLM packets and/or parameter dump.

2) Normal Mode

The XTS Normal Operation is used for normal Down Link Transmissions, and is performed in parallel to other MSC missions. Normal Operation is required to perform MSC missions such as Direct Imaging Mission, Record and playback imaging Mission, Playback Mission and MSC Service Mission. In this mode the APS shall perform two-axis motion according to a commanded Tracking Profile. Both Azimuth and Elevation drivers are enabled. The desired TPF must be indicated by index in the Mission Command. For each Transmission Pass a dedicated TPF is needed. Once MST reaches the TPF Start Time the XTS Servo S/W will calculate every 10 msec the APM motor drive (PWM) signal values necessary to drive the APM motors towards the position commanded by the reconstructed Tracking Profile, taking into account feedback from the actual antenna position. Once MST reaches the TPF End Time the APS should have reached the Parking position (0,0) degrees. The XTS will automatically leave the Normal Operation Mode and return to STANDBY mode.

3) XTS First Elevation Operation

When executing this mode for the first time (after successful pyro ignition) it shall be verified by the operator that the APS is still in stowed position at AZ/EL (0,+5) degrees. The purpose of this procedure is to release the Hold & Release Mechanism (HRM) latch, thus preventing the APS to return to Elevation angles > 0 degrees. Upon entering this mode, the XTS shall enable only the APDE Elevation motor driver and servo loop. The APS is then commanded to move to an elevation of +15° at a velocity of <10°/sec, according to a pre-programmed function. At completion of this procedure (after time-out of 5 seconds from beginning of execution) the XTS shall automatically return to STBY Mode, however the APS shall remain at 15 deg. Elevation (as preparation for the First Azimuth Operation). No RF Transmission is allowed during execution of this mode. The First Elevation Operation may be executed (followed by First Azimuth Operation) whenever needed to clean the APS slip-rings.

4) XTS First Azimuth Operation

This mode will normally follow the execution of First Elevation Operation. The purpose of this procedure is to verify free motion of the APS azimuth axis, and clean the APS slip-rings. Upon entering this mode, XTS shall enable both APDE Azimuth and Elevation motor drivers and servo loops. The APS is then commanded to hold a constant elevation position of +15°, while performing in azimuth 15 rotations CW and 15 rotations CCW at a velocity of <30°/sec. Immediately upon completion of the rotations the antenna shall be returned to parking position (0,0). At completion of this procedure (after time-out of 5 seconds from beginning of execution) the XTS shall automatically return to STBY Mode, however

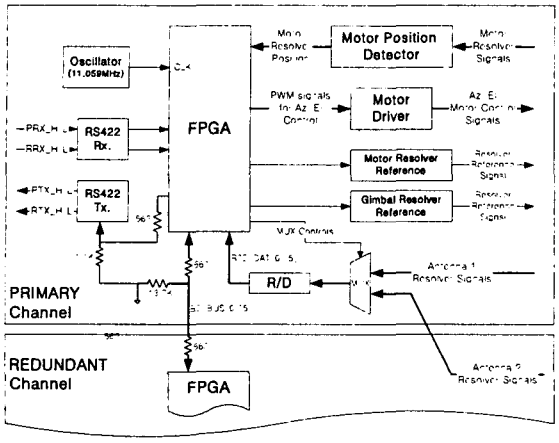

Fig.3 Block diagram of APDE

the APS shall remain at 15 deg. Elevation (as preparation for the First Azimuth Operation). No RF Transmission is allowed during execution of this mode. The First Azimuth Operation may be executed (in combination with a First Azimuth Operation) whenever needed to clean the APS slip-rings.

5) IBIT mode

In IBIT mode both AZ and EL motor drivers and servo loops are disabled and RF transmission is allowed. In this mode the APDE R/D's are fed with combination of synthetic sinusoidal signals imitating specific resolver angles. The APDE will return to the PMU-SBC a sequence of 8 angle measurements, every 0.5 seconds the angle measurement will be varied according to a fixed pattern. The angle measurements shall be checked for correctness and accuracy. Upon completion of the series of angle measurements the XTS shall return automatically to STBY Mode.

4. APDE Design

The Antenna tracking is supported by H/W and S/W blocks. The main parts of H/W are SBC and APDE boards inside the PMU, interconnected by a serial communications channel, and the APS. The S/W blocks include the ATS (Antenna Tracking System) S/W module running on the SBC platform, as well as the S/W controlling the serial communications link to the APDE.
The APDE configuration is shown in Fig.3. There are 2 Primary/Redundant APDE circuits on the single board with partial cross-strapping. Each one is divided into 3 sub-systems, FPGA Controller, Measurement Block (includes R/D), Antenna Driver, which may be switched on/off separately. Detail explanation is given below.

1) overall architecture

As shown in Fig.3 general functional blocks and subcircuits of the channel consist of Motor Driver block, Motor Resolver Interface block, Gimbal Interface block, controller block and serial communication block. All necessary functional logics to be used in generating PWM signals, Resolver reference signals are provided by FPGA controller according to the commands and control parameters from SBC and measurement data from resolver in APM. Motor driver block generates PWM signals that meet specifications of motors in APM to move antenna. Resolver interface block reads antenna resolver data through A/D converter in 16-bit with a cross-strap configuration which is supported inside a board. And serial communication block makes connection to SBC with full cross-strap to support primary/redundant design concept. The bus connection between each FPGA in Fig. 3 is for supporting cross-strap operational mode of XTS.

2) Motor and Resolver Interface

The (primary or redundant) APDE channel controls 2 SAGEM's motors by the PWM command, for Azimuth, Elevation axes, and built-in motor resolver shall be used as the rotor position sensor to commutate the current in the motor windings. The driver output shall have the option of high impedance, controlled by SBC disable command in order not to flow current in disable condition of motor movement. The APDE channel shall drive only motors of the corresponding APM. As a measurement the APDE channel shall measure two SAGEM resolvers (azimuth and elevation axes). The analog Antenna angular position shall be converted by the Resolver-to-Digital (R/D) to 16bit digital data. Each one of the APDE channels shall excite only the resolvers of the corresponding APM.

3) SBC-APDE Interface

One of important functions of the APDE is to serve as electronic interface between APM and SBC. In order for the APDE to receive motor commands from the SBC and return APM sensor data(gimbal angular position through resolver sensors), the SBC shall be connected to the APDE board via RS-422 compatible interface. Each one of the APDE channels shall communicate with primary or redundant SBC via half duplex hardware with full cross strap design. This communication is performed by the Master/Slave Serial protocol, where SBC acts as master while APDE as slave.

4) H/W configuration

The APDE board can be configured to operate at normal or cross-strap configuration by the configuration command from SBC. Only one APDE channel shall be active (power on) in the normal configuration The Power Supply Module (PSM) should supply the input operational voltage to the active channel and the active APDE channel shall interface with corresponding APM to measure the APM gimbals angular position through resolver sensors, and drive the APM motors. Both APDE channels(primary and redundant) shall be active in the cross-strap configuration. The one channel shall be full powered on while other partially on. The APDE H/W internal design shall provide partial cross-strap. This design shall allow the operation of both APM using ei-

ther (primary or redundant) R/D converter. The communication protocol between the SBC and APDE includes a flag which defines the APDE H/W configuration. The details are explained bellows.

5) R/D Latch-up protection

The APDE H/W design includes Latch-Up Protecti on in which protection circuit shall disconnect power supply from R/D to avoid damage during Latch–Up event whenever the amount of current exceeds some limit.

6) FPFA design

As main logic core of the APDE it executes functions of Handling of serial communication protocol, acquisitions of data from two channel Resolver to Digital converter, Analogue MUX control and PWM control of four H-Bridges, which drives a pair of motors. To allow for full redundant operation, the APDE includes two identically designed FPGA devices, one for each of the primary and redundant channels. Besides the interface of each device with its own channel, there is an additional "bridge" interface between the two devices, thereby providing the APDE with an auxiliary Cross-Strap operating configuration. It functional structure is depicted in fig. 4 and include the following blocks -UART, TRANCEIVER_CNT, PWM_1, R2D, MSGDATMUX, ANALOGMUXCNTR, CROSS_STRAP_MUX.

7) Physical construction and dimension

The APDE card shall be assembled on a rigid PCB, which is equipped with a pair of right angle connectors placed along the PCB long edge. The Primary and Redundant channel component groups shall separate and locate as shown in Fig. 5. Thus Redundant C.S(Component Side) is placed at the same side as the Primary P.S(Print Side) and Redundant P. S shall be the same as the Primary C. S after a rotation of 180 degrees about the axis A.

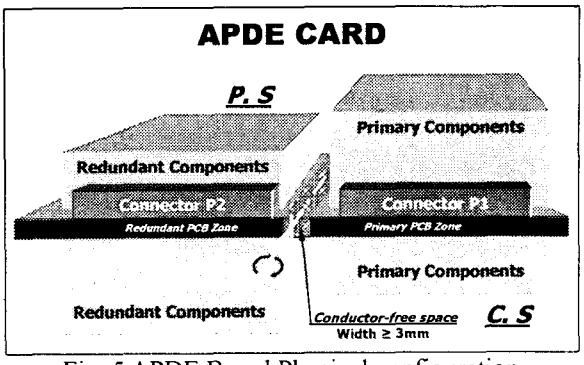

Fig. 5 APDE Board Physical configuration

For MSC to communicate with ground station it should operate its own antenna properly according to the predefined profile. This operation is performed by XTS which consists of H/W and S/W. In this paper, we described details on designs of APDE board which is a main electronic board in XTS. It has primary and redundant design concepts, and provides full-cross-strap connections for serial communication and partial-cross-strap for Resolver measurement, motor driving. In addition to that, latch-up protection circuit prevents APDE board from a possible damage when some high current flow due to latch-up phenomena. And, the APDE has the capability of supporting several operational modes by combining primary and redundant board with the unique design concept in which it is possible for each operation voltage to be supplied separately by the control of controller board in PMU.

4. Conclusions

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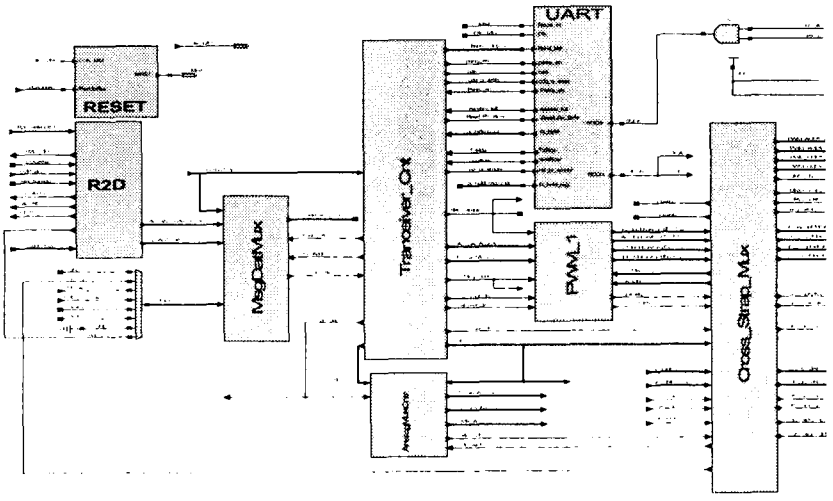

Fig. 4 APDE FPGA Design block diagram