ULTRA LOW-POWER AND HIGH dB-LINEAR CMOS EXPONENTIAL VOLTAGE-MODE CIRCUIT

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Abstract: This paper proposed an ultra low-power CMOS exponential voltage-mode circuit using the Pseudo-exponential function for realizing the exponential characteristics. The proposed circuit provides high dB-linear output voltage range at low-voltage applications. In a 0.25 μm CMOS process, the simulations show more than 35 dB output voltage range and 26 dB with the linearity error less than ± 0.5 dB. The average current consumption is less than 80 μA. The proposed circuit can be used for the design of an extremely low-power variable gain amplifier (VGA) and automatic gain control (AGC).

1. INTRODUCTION

The advances in the CMOS VLSI technology and the market demand for portable and mobile electronic equipment lead to increasing reductions on the power consumption. CMOS devices feature high-input impedance, extremely low-offset switches, high packing density, low-switching power consumption, and most importantly, they are easily scaled. Scaling down the transistor sizes can then integrate more circuit components in a single chip so the circuit area, and thus its cost, will be reduced. When a MOS transistor size is decreased, not only are its channel length and width reduced, but also the thickness of the gate oxide. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced. Also, lowering the supply voltage is the most efficient way to lower the power consumption. As a result, low-voltage and low-power CMOS VLSI circuits are of particular interest.

The exponential functional circuit is the key component for the design of VGAs and AGCs, which are widely used in analog signal processing; such as in hearing aids, disk drive, and telecommunication applications [1-3]. This circuit is not available in CMOS technology since CMOS transistors follow a square-law characteristic in strong inversion. However, it is easily obtained in bipolar technology. Unfortunately, the bipolar techniques for VGAs and AGCs are not compatible for monolithic low voltage CMOS-based analog and mixed-signal circuits. Moreover, good performance bipolar transistors are not readily available in the conventional technology, while BiCMOS solution may not be cost-effective. Although CMOS transistors exhibit exponential characteristics in weak inversion, except the very low-speed application, the circuit could be too slow.

Since there is no intrinsic logarithmic MOS device operating in the saturation region for CMOS technologies, the exponential characteristics can be implemented by using a "pseudo-exponential" generator [1-4], or Taylor series expansion for realizing the exponential characteristics [5-7]. However, these previously reported approaches show very small dB-linear output range less than 17 dB while dissipate high power (> 0.3 mW) [5-7].

In this paper, the author proposes a new and very compact exponential functional circuit that offers very high output range (26 dB with error less than ± 0.5 dB) while consumes ultra low power (less than 80μA). The simulation results will be given to verify the validity of these approaches.

2. BASIC APPROXIMATIONS

As mentioned in section 1, two exponential approximation functions have been used. The first one used Taylor series expansion for realizing the exponential characteristics and truncates its Taylor polynomial with the accuracy needed. According to the Taylor series expansion, a general exponential function can be expressed as

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \ldots + \frac{a^n}{n!}x^n + \ldots \quad (1)$$

Where a and x are the coefficient and the independent variables, respectively. For $|ax| << 1$, the Taylor series approximation function can be given as

$$e^{ax} \approx 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (2)$$

By using the Taylor expansion with its first order polynomial, the second method based on the "pseudo-exponential" function for realizing the exponential characteristics, which is given as

$$e^{ax} = \frac{e^{ax/2}}{e^{-ax/2}} \cong \frac{1 + ax/2}{1 - ax/2} \quad (3)$$

for a = 0.1, the plots of the pseudo-exponential approximation and the Taylor series approximation are given in Fig. 1 (a) by the dash-dotted and dashed lines, respectively.

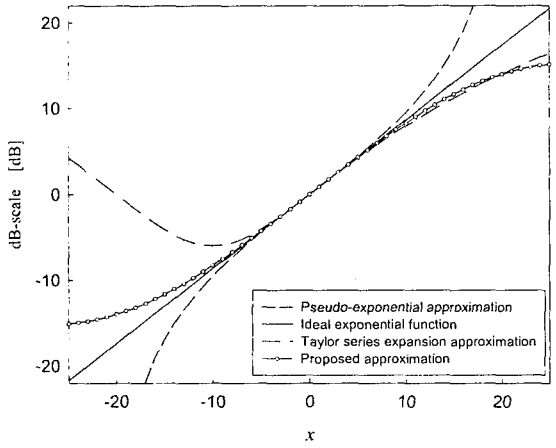

Fig. 1 (a) Plots of various functions on dB-scale

As shown in Fig. 1 (a), the Taylor series approximation and the pseudo-exponential approximation provide 12 dB and 15 dB ranges with the linearity error less than ± 0.5 dB, respectively. Typically, the "pseudo-exponential" generator is of particular interest since it provides larger dB-linear range compared to that of the other one. From Eq. (3), it is obviously that the implementation of the pseudo-exponential generator based on the second-order Taylor polynomial results in higher dB linear range. However, to the author's knowledge, there is no approach based on the second-order polynomial pseudo-exponential generator. Consequently, this paper proposed a very compact circuit that implements this approximation.

The exponential approximation based on the second-order Taylor expansion is as follows

$$e^{2ax} = \frac{e^{ax}}{e^{-ax}} \cong \frac{1 + ax + (ax)^2/2}{1 - ax + (ax)^2/2} \quad (4)$$

the numerator and denominator in Eq. (4) are all second-order Taylor series approximation functions. The proposed approximation can achieve about 20 dB with linearity error less than ± 0.5 dB as depicted in Fig. 1 (a) by the o'symbol line, which means that by using Eq. (4) the circuit obtains 5 dB improvement compared to that of Eq. (3).

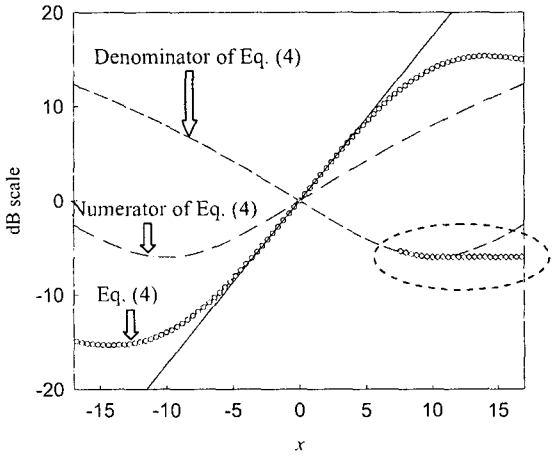

Fig. 1 (b) Plots of various functions on dB-scale

Fig. 1 (b) shows the detail plot of Eq. (4) which is drawn for a = 0.1. As shown in this figure, for $|x| >$ 5 the o'symbol line deviates from the ideal exponential function. For $x > 5$, if a part of the dashed line in the ellipse of Fig. 1(b) go downward to the diamond's line, the Eq. (4) will move close to the ideal exponential function, leading to the improvement of the dB linear range. By applying this technique, this paper can also obtain 6 dB improvements, leading to 11 dB linear improvement in total, if compared to Eq. (3)

The proposed circuit to implement Eq. (4) will be developed in section 3.

3. CIRCUIT DESCRIPTIONS

3. 1 BASIC CIRCUIT

To implement the Eq. (4), the Taylor series expansion approximation is needed. This section presents a basic and very compact circuit for realizing the Taylor approximation as shown in Fig. 2 [9]. The

transistors M1 and M2 in Fig. 2 are assumed to be in saturation region. Hence, the drain current of these two transistors is given as

$$I_d = K(V_{GS} - V_{TH})^2 \quad (5)$$

where

I_d is the drain current,
K is the transistor's parameter,
V_{GS} is the gate-source voltage, and
V_{TH} is the threshold voltage.

The output current I_{out} of the basic circuit in Fig. 2 is given as

$$I_{out} = K(V_{in} - V_{TH})^2 + K(V_{BIAS} - V_{TH})^2 \quad (6)$$
$$= K(V_{in}^2 - 2V_{TH}V_{in} + V_{BIAS}^2 - 2V_{BIAS}V_{TH} + 2V_{TH}^2)$$

the threshold voltage is supposed to be constant. From Eq. (6), the output current I_{out} as a function of the voltage V_{in} can be Taylor series approximated function as in Eq. (2) by controlling the bias voltage V_{BIAS}.

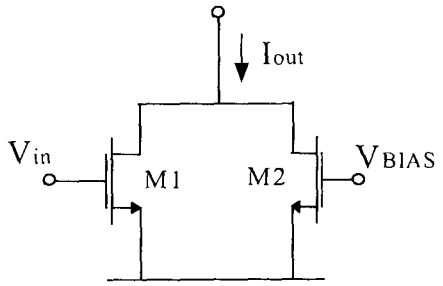

Fig.2 Basic circuit for realizing Taylor series approximation function.

3.2 PROPOSED EXPONENTIAL VOLTAGE-MODE CIRCUIT

From the basic circuit in Fig. 2, the complete proposed circuit is given in Fig. 3. The proposed circuit uses two basic circuits in which one uses the NMOS transistors and the other uses PMOS transistors. In Fig. 3, by controlling the V_{BIAS1} and V_{BIAS2}, the current I_1 and I_2 can be realized as Taylor series approximation functions. By adjusting the V_{BIAS1}, V_{BIAS2}, and the aspect ratios of transistors in the basic NMOS and PMOS circuit, the ratio I_1/I_2 can be identical to the approximation function shown in Eq. (4).

As shown in Fig. 3, the current I_1 is copied to the drain current of the transistor M8. And, the current I2 is directed to the common drain node of the two diode connected transistors M5 and M6, which is also the gate of M9. As reported in [10] the transistors M7 and M8 constitute the linear I-V converter, and as reported in [4] the output voltage of this converter is given as

$$V_{G,M9} = \frac{V_{DD} - |V_{Tp}| + V_{Tn}}{2} - \frac{I_2}{K(V_{DD} - |V_{Tp}| - V_{Tn})} \quad (7)$$

Where $V_{G,M9}$ is the output voltage of this converter which is also the gate voltage of transistor M9.

The transistor M9 is assumed to be in the triode region and acts as a voltage controlled resistor. For small drain-source voltage, the resistance exhibited by M9 is given as

$$R_{DS} \approx \frac{1}{K_{M9}(V_{G,M9} - V_{TH})} \quad (8)$$

Consequently, the current I_1 flowing through M9 will generate a drain-source voltage, $V_{DS} = R_{DS}I_1$, proportional to I_1/I_2.

From Fig. 3, the input dynamic range should be

$$V_{Tn} < V_{in} < V_{DD} - V_{Tp} \quad (9)$$

Where V_{Tn} and V_{Tp} are respectively threshold voltage of NMOS and PMOS transistors.

4. SIMULATION RESULTS

The proposed circuit was verified in 0.25 μm CMOS technology with the supply voltage of $V_{DD} = 2$ V and $V_{SS} = 0$ V. The bias voltages V_{BIAS1} and V_{BIAS2} are respectively 0.78 V and 1.25 V. The threshold voltage of NMOS and PMOS transistors in our process is 0.5 V and 0.6 V, respectively. From Eq. (9), the input dynamic range is thus from 0.5 V to 1.4 V. The performance of the proposed exponential voltage-mode circuit is given in Fig.4. As V_{in} lies in the input dynamic range, the exponential approximation as in Eq. (4) is obtained with linear 20 dB range with the error less than ±0.5 dB. Out of this valid input range, the linearity error between the exponential approximation and the ideal exponential function is increased as depicted in Fig. 1(b) by the o'symbol line. However, for $V_{in} > 1.4$ V, the transistor M3 is in the triode region and then cut-off. As a result, the I_2 (*i.e* the denominator of Eq. (4)) deviates from the ideal exponential function, and it performs as the diamond's line in the ellipse in Fig. 1(b), leading to the improvement of the dB-linear range. As shown in Fig. 4 by the solid line, the proposed circuit can achieve 35 dB range and 26 dB-linear range with the error less than ±0.5 dB.

5. CONCLUSIONS

This paper proposed a simple circuit to achieve the pseudo-exponential approximation function. The

proposed circuit achieves 26 dB linear range with error less than 0.5 dB at ultra low-power consumption (less than 80 μA). It can be used for the design of an extremely low-power VGAs and AGCs. The proposed circuit in this paper could also be used as a current-to-voltage converter by adding the linear I-V converter, which is discussed in section 2, to the input of the circuit in Fig. 3.

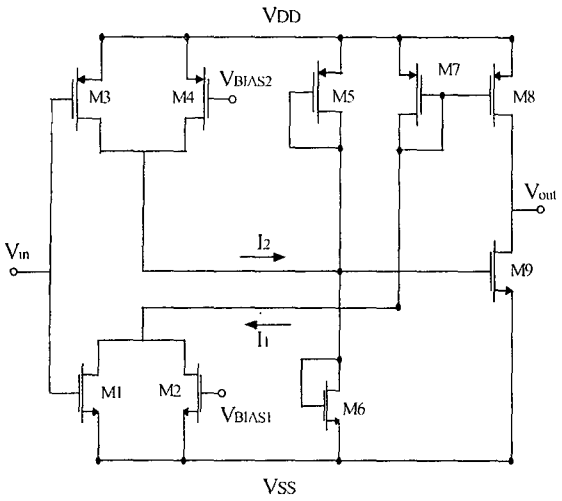

Fig. 3 The proposed exponential voltage-mode circuit

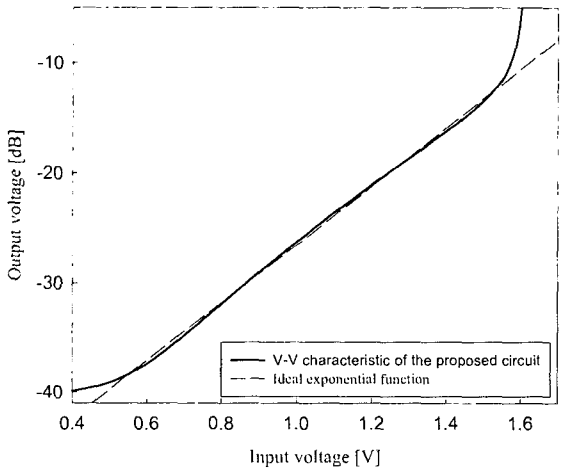

Fig. 4 The performance of the proposed circuit shown in Fig. 3.

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