The Trap Characteristics of SILC in Silicon Oxide for SoC

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Abstract:

In this paper, The stress induced leakage currents of thin silicon oxides is investigated in the nano scale structure implementation for SoC. The stress and transient currents associated with the on and off time of applied voltage were used to measure the distribution of high voltage stress induced traps in thin silicon oxide films. The stress and transient currents were due to the charging and discharging of traps generated by high stress voltage in the silicon oxides. The channel current for the thickness dependence of stress current, transient current, and stress induced leakage currents has been measured in oxides with thicknesses between 41□ and 113.4□, which have the channel width x length 10x1um, respectively.

The stress induced leakage currents will affect data retention and the stress current, transient current is used to estimate to fundamental limitations on oxide thicknesses. The weight value of synapse transistor was caused by the bias conditions. Excitatory state and inhitory state according to weighted values affected the channel current. The stress induced leakage currents affected excitatory state and inhitory state.

I. Introduction

The traps are generated inside the oxides and at the oxide interfaces by the applied electric fields across the oxide and the flowing currents through the oxides in the nano scale structure for SoC. The trap charging and discharging currents can be explained by the flow of electrons into and out of traps generated by the stress high electric field. The traps are negatively charged near the cathode and positively charged near the anode respectively in the condition. The charge state of the traps can easily be changed according to the application of repetitively low electric fields after the stress high electric fields. Measurements have shown that the traps are relatively uniformly distributed throughout 113.4□ to 814□ silicon oxide thicknesses. In this study we present evidence that shows to the difference trap densities near anodes and cathodes of thicker oxides in the nanoscale structure. It was due to the charging and discharging after high electric field stressing.

The tunneling front model could be used to analyze the low level currents and pretunneling currents that have been observed in stressed silicon oxides. The transient currents associated with the during and removal of low voltage to the stressed silicon oxides were determined to be the charging and discharging of the traps generated in the silicon oxides. These transient currents were analyzed to determine the distribution of the stress generated traps in the silicon oxides near the anode and cathode interfaces.

II. Results and discussion

The current was composed of three regions, the low level, pretunneling region, the tunneling region and the breakdown region. Onset tunneling voltage was measured 7.2[V] 9.2[V] 10.2[V] with fluence 1.07×10^{-8} [C/cm^2], 1.02×10^{-11}[C/cm^2], 1.19×10^{-13}[C/cm^2] in the oxide thickness between 41□, 86□, 112□ respectively. Prior to the onset of tunneling the currents were in the low ampere range. The current density according to the gate bias voltage was measured in the oxide thickness between 41□, 86□, 113.4□ respectively has been shown Fig. 1.

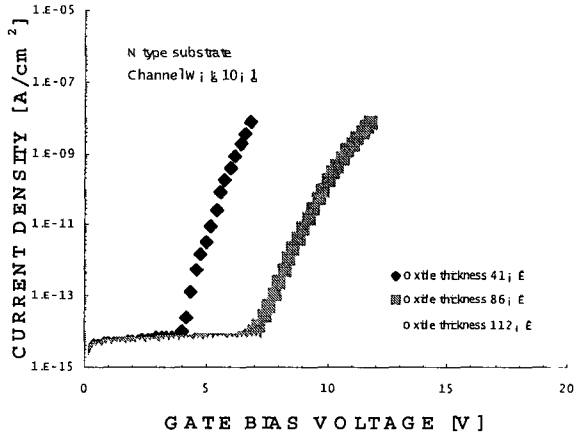


Fig.1 Gate bias voltage vs. current density in the oxide thickness between 41□, 86□, 112□ respectively

Constant voltages with high tunneling currents were used to stress the oxides. The stress currents were

measured during the stress and integrated to obtain the fluence through the oxide. The transient currents associated with the turn off of the stress voltages were measured. The constant gate voltages were on time when the positive currents flowed. As long as the applied voltages were less than the onset voltage of the tunneling current, the stress and transient currents were represented by the charging and discharging.

The stress currents through an unstressed oxide measured during application of constant positive gate voltage and the transient currents through an unstressed oxide measured after application of constant positive gate voltage has been shown in Fig. 2.

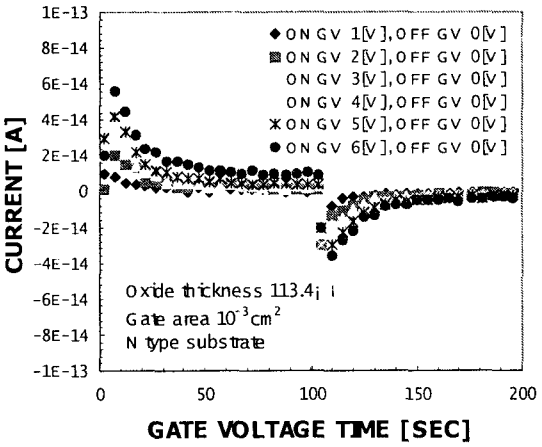
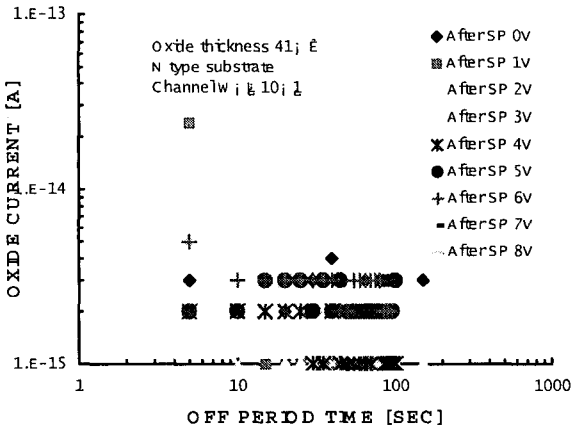


Fig. 2 The stress and transient currents through an silicon oxide after/during the applied positive electric field

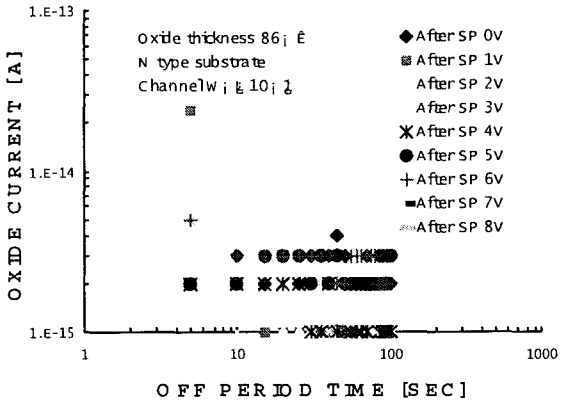
The constant electric field were on time when the positive currents flowed and were off time when the negative currents flowed. As long as the applied electric fields were less than the onset electric field of the tunneling current, the transient currents were represented by the charging and discharging. The central 0 value of vertical axis was used in order to plot both positive and negative currents on the same scale. The central 0 value of vertical axis was 10^{-15}[A] for the positive currents shown in the figure and -10^{-15}[A] for the negative currents shown in the figure.

The stress currents were not exponential decay when the applied voltages were made larger than the onset of tunneling but the transient currents were exponential decay when the applied voltages were made less than the onset of tunneling. The transient currents were subsequently measured at low electric fields below the onset electric field of tunneling.

When the voltages applied to the oxide were increased, transient currents were measured, as shown in Fig. 3



(1)



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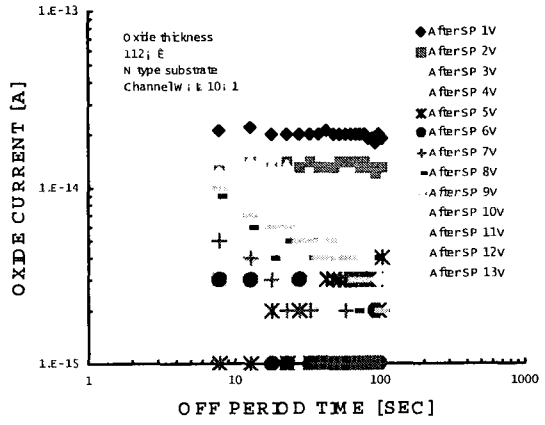

(3)

Fig. 3 The transient currents through silicon oxide after the applied positive gate

The stress currents were not exponential decay when the applied voltages were made larger than the onset of tunneling but the transient currents were exponential decay when the applied voltages were made less than the onset of tunneling. The transient currents were subsequently measured at low voltages below the onset voltage of tunneling.

The stress currents when the voltage stresses were on time for the voltages for which FN tunneling was significant. The stress currents reflected the changes in the shape of the tunneling barrier due to trapping of electrons in the oxides. The transient currents after stress voltage were off time were decayed slowly. The transient currents followed an exponential decay.

The capacitor in this case was stressed at -17[V] for 100[sec] respectively. The transient currents were measured after the stress at 5[V] for 100[sec]. The transient currents after application of a voltage pulse for an oxide that had been stressed with either positive stress voltage or negative voltage has been shown in Fig. 4.

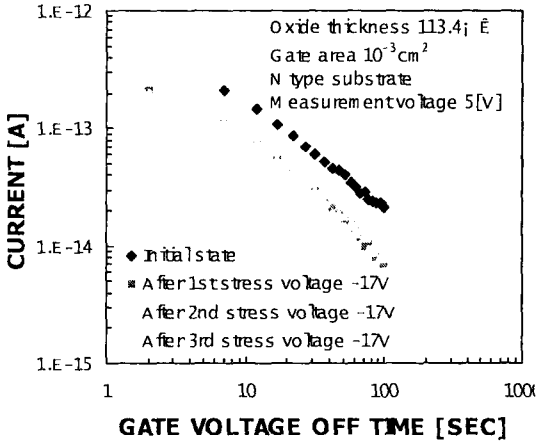

Fig. 4 The transient currents through silicon oxide after the applied pulse voltage -17[V]

After the oxides had been stressed and traps had been generated in the oxides, the pretunneling currents and the discharge currents rose. The discharge currents have been adequately explained in terms of the tunneling front model. The pretunneling currents that flowed when the low measurement voltages were applied were also related to the charging of the stress generated traps. difference in these two charging currents had the 1/t time dependence that had previously been associated with the discharging of these traps by the tunneling front. Thus, by fitting the difference in the currents to a 1/t dependence, the charging of the traps in the oxide could also be explained by the tunneling front model.

Whenever the measurement polarity was changed, it was necessary that the one time only leakage current caused by the transient tunneling charging discharging of the traps. The stress induced leakage currents were measured on an 113.4□thick oxide fabricated on n type silicon after positive gate voltage stressing at 13V has been shown in Fig. 5.

The stress induced leakage currents measured after a high electric field stress showed a higher stress induced leakage currents than subsequent stress induced leakage currents.

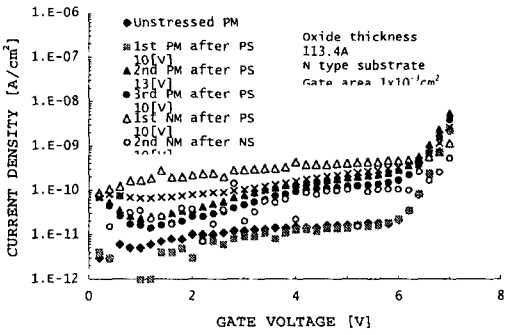

Fig. 5 The stress induced leakage currents of a 113.4 □oxide after negative gate voltage stressing at 13V

The stress induced leakage currents showed a one time only leakage current whenever the measurement polarity was changed. This one time only leakage current was caused by the transient tunnel charging discharging of the traps near the interfaces. The stress induced leakage currents depend on trap location. The decay of the low electric field tunneling current was decided to use the increase in the stress induced leakage currents as a measure of trap distributions in the oxides. The stress induced leakage currents are related to trap assisted tunneling processes in thin oxides. The stress induced leakage currents are proportional to the stress induced trap densities. The negative measurement electric fields sampled the traps near the substrate and the positive measurement electric fields sampled the traps near the gate.

III. Conclusions

The transient currents associated with low voltage pulses applied to thin oxide of the polysilicon gate Metal Oxide Semiconductor capacitors have been analyzed in terms of the charging and discharging of stress generated traps in the oxide. The tunneling front model was used to explain the 1/t time dependence of the decay current after application of a low voltage pulse. The transient currents were dependent on the stress polarity. The stress generated transient currents were relatively uniform the order of 10^{-11}□10^{-15}[A] after a high field stress voltage.

The stress anode and cathode were used to attempt to find the differences in trap densities of silicon oxides for the nano scale structure. The traps are negatively charged near the cathode and positively charged near the anode respectively. The charge state of the traps can easily be changed according to the application of repetitively low electric fields after the stress high electric fields.

References

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