Implementation of sigma-delta A/D converter IP for digital audio

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Abstract:

In this paper, we only describe the digital block of two-channel 18-bit analog-to-digital (A/D) converter employing sigma-delta method and x128 decimation. The device contains two fourth comb filters with 1-bit input from sigma-delta modulator, each followed by a digital half band FIR(Finite Impulse Response) filters. The external analog sigma-delta modulators are sampled at 6.144MHz and the digital words are output at 48kHz. The fourth-order comb filter has designed 3 types of ways for optimal power consumption and signal-to-noise ratio. The following 3 digital filters are designed with 12tap, 22tap and 116tap to meet the specification. These filters eliminate images of the base band audio signal that exist at multiples of the input sample rate. We also designed these filters with 8bit and 16bit filter coefficient to analysis signal-to-noise ratio and hardware complexity. It also included digital output interface block for I2S serial data protocol, test circuit and internal input vector generator. It is fabricated with 0.35um HYNIX standard CMOS cell library with 3.3V supply voltage and the chip size is 2000um by 2000um. The function and the performance have been verified using Verilog XL logic simulator and Matlab tool.

Keyword: ADC(Analog-to-Digital Converter), Sigma-Delta Modulator, FIR Filter, Comb Filter, SNR(signal-to-noise rate)

1. INTRODUCTION

Recently, ADC(Analog to Digital Converter) must be designed to offer high performance and low power consumption within small area by trend of mobile system. Sigma-Delta A/D Converter is very suitable structure in voice or audio signal processing that require the slow speed and high resolution. Therefore, in this paper we describe the digital block of two-channel 18-bit analog-to-digital (A/D) converter employing sigma-delta method and x128 decimation that is based on the implementation of a modulator to perform high resolution, optimal SNR and low-voltage, low power consumption. Also, we use filters as comb filter and half band FIR filter. But, if there are been many filters, because complexity of hardware increases, we designed these filters with 8bit and 16bit filter coefficient to analysis signal-to-noise ratio and hardware complexity [1-5].

The design is fabricated with 0.35um HYNIX standard CMOS cell library. After, The Chip will be tested using test board with FPGA equipment and ATS2 digital test equipment.

This paper is organized as follows. First, in section 2, we introduce about structure of sigma-delta ADC digital block and explain structure and feature of each block. Section 3 shows simulation result. Also, in section 4, we show chip layout and test result. Finally, we present a conclusion in section 5.

2. SIGMA-DELTA ADC

Figure 1 shows digital block diagram of sigma-delta ADC.

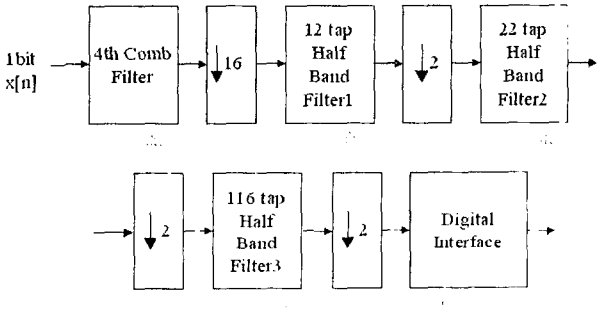

Fig. 1. Sigma-delta ADC digital block diagram

The comb filter, first block of Figure 1 has high clock frequency of 128 sampling frequency. So comb filter block consumes most power. Design optimization for this block influences in whole power consumption and optimization of circuit. This paper designed three methods for comb filter as follows.

1. Using integrator and differentiator.
   The block implements 5^{th}, 7^{th} integrator and differentiator as Figure 2. Also, we designed warp-around method for diffusion issue in output of integrator.

2. Implementation using FIR filter for comb filter.
   In this method, diffusion issue not appears. But needs multiply operation, so increased area and power consumption. This method shows Figure 3.

3. Implementation using current input and previous input.

This method not uses integrator. It is optimal method about power and performance. This method shows Figure 4.

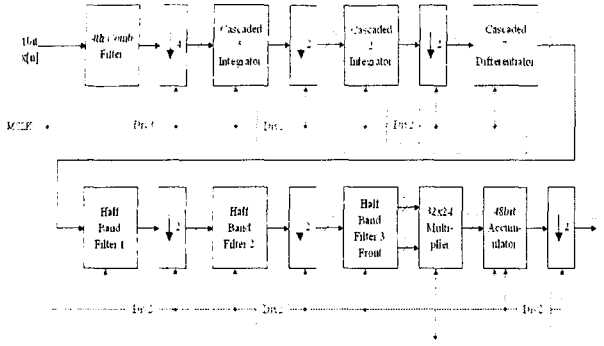

Fig. 2. ADC digital block using integrator and differentiator

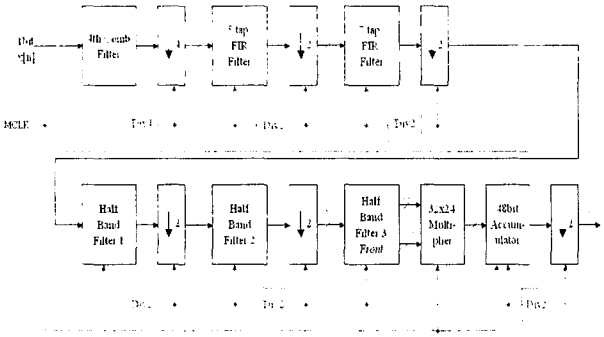

Fig. 3. ADC digital block using FIR filter

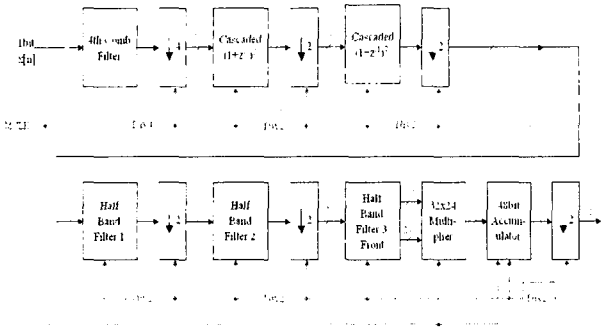

Fig. 4. ADC digital block not using integrator

2.1 Comb Filter

Third-order sigma-delta modulator output has +1 or −1 value of 1bit. The external analog sigma-delta modulators are sampled at 6.144MHz and the digital words are output at 48kHz. The equation of Comb filter is as follows equation (1).

$$H(z) = \left(\frac{1 - z^{-4}}{1 - z^{-1}}\right)^4 \left(\frac{1 - z^{-8}}{1 - z^{-4}}\right)^5 \left(\frac{1 - z^{-16}}{1 - z^{-8}}\right)^7 \qquad (1)$$

Also, Comb filter designed x16 down sampling as Figure 5.

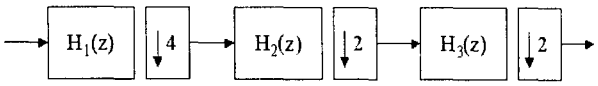

Fig. 5. Comb filter block diagram

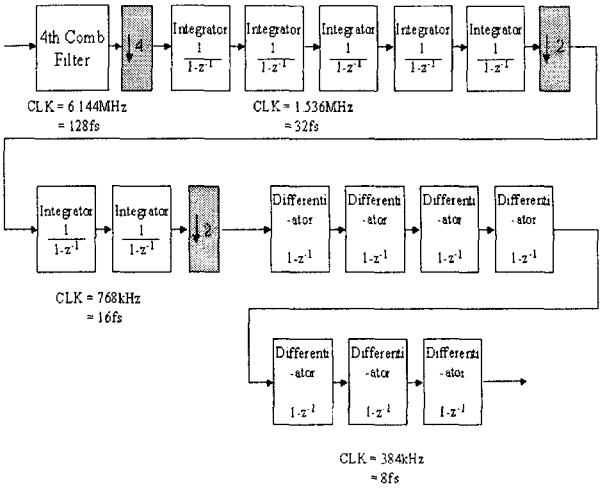

Fig. 6. Comb filter block diagram about equation (1)

2.1.1 Comb filter using integrator and differentiator

Figure 6 shows comb filter detail block diagram using integrator and differentiator. Fourth-order comb filter receives input by high-speed output of x128 sampling frequency. So we designed using ROM. Equation (2) is equation about forth-order comb filter[6].

$$H(z) = \left(\frac{1}{256}\right)\left(\frac{1 - z^{-4}}{1 - z^{-1}}\right)^4 \qquad (2)$$

It can appear FIR form as follows.

$$H(z) = \frac{1}{256}\left(\sum_{i=0}^{3} z^{-i}\right)^4 = (1 + z^{-1} + z^{-2} + z^{-3})^4 = \frac{1}{256} + \frac{4}{256}z^{-1} + \frac{10}{256}z^{-2} + \frac{20}{256}z^{-3} + \frac{31}{256}z^{-4} + \frac{40}{256}z^{-5} + \frac{44}{256}z^{-6} + \frac{40}{256}z^{-7} + \frac{31}{256}z^{-8} + \frac{20}{256}z^{-9} + \frac{10}{256}z^{-10} + \frac{4}{256}z^{-11} + \frac{1}{256}z^{-12} \qquad (3)$$

1-bit(+1, -1) value of x(n), x(n-1), x(n-2), x(n-3), x(n-4), x(n-5), x(n-6), x(n-7), x(n-8), x(n-9), x(n-10), x(n-11), x(n-12) is stored 1 bit register. It can common use coefficient of ROM, because it is right and left symmetry laying stress on x(n-6) as appear figure 7. The coefficient of ROM is outputted value of 8 bits calculated beforehand according to x(n), x(n-1), x(n-2), x(n-3), x(n-4), x(n-5). The value appears 2's complement and MSB is sign bit. 00000000 is value of "0" and from 10000000 to 11111111 appear negative number. This method is efficient for power consumption and area.

In figure 7, it shows 1-bit forth-order comb filter using ROM. It uses two 8-bit address and 64word * 8bit ROM.

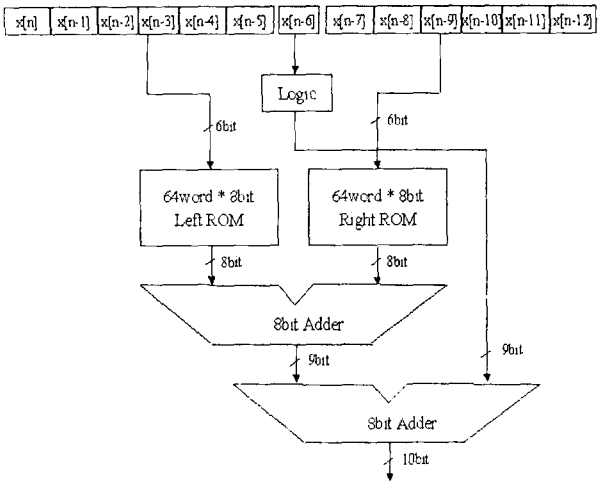

Fig. 7. 1-bit forth-order comb filter using ROM

1) Fifth-order Integrator

The 10-bit output of figure 7 is inputted fifth-order integrator filter of five integrators. Each integrator is designed form by $y[n] = x[n] + y[n-1]$. The integrator is implemented circuit by addition of current input and previous output. It is designed x2 decimation. The output bit of integrator is considered by equation (4).

$$Minimum\ word\text{-}length = Input\text{-}bit + klog_2M \qquad (4)$$

It is input-bit =10 and k=5, M=2. So Minimum word-length is 15bit.

2) Seventh-order Integrator and differentiator

As figure 6, seventh-order integrator is received output of fifth-order integrator. It is organized IIR filter which two integrators are linked by series. The word lengths of Input and output have 32bit.

Seventh-order differentiator has x8 sampling frequency, because it is designed x16 decimation. It has equation by $y[n] = x[n] - x[n-1]$.

2.1.2 Comb filter using FIR

Comb filter using integrator appears diffusion issue. So we are designed by creating to output of modulo form. But it needs verification by system level[7][9].

In this method, we consider comb filter using FIR. The equation of implemented FIR function is as follows.

$$H_2(z) = \left(\frac{1 - z^{-8}}{1 - z^{-1}}\right)^5 \qquad (5)$$

It is received x4 decimation input. So it can be change FIR filter form as follows.

$$H_2(z) = \left(\sum_{i=0}^{1} z^{-i}\right)^5 = (1 + z^{-1})^5 \qquad (6)$$

$$= \frac{1}{2^5}(1 + 5z^{-1} + 10z^{-2} + 10z^{-3} + 5z^{-4} + 10z^{-5})$$

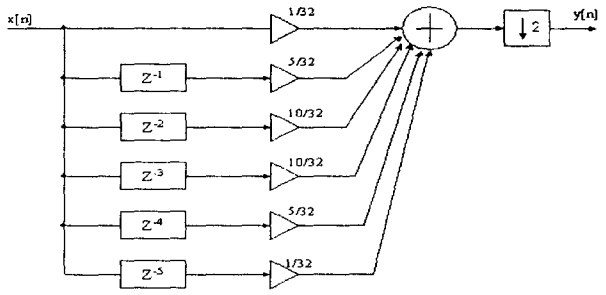

Fig. 8. FIR filter about $H_2(z)$

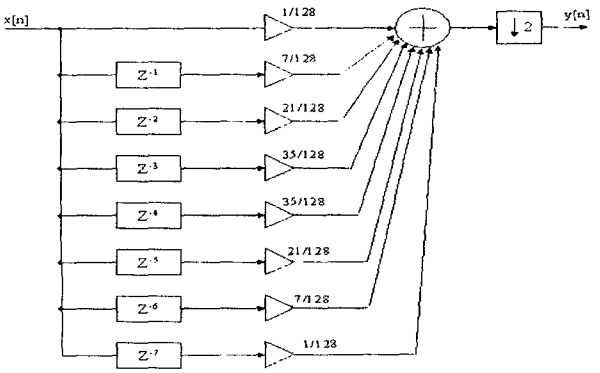

Fig. 9. FIR filter about $H_3(z)$

Similarly, $H_3(z)$ is as follows.

$$H_3(z) = \left(\frac{1 - z^{-16}}{1 - z^{-8}}\right)^7 = \left(\sum_{i=0}^{1} z^{-i}\right)^7 = (1 + z^{-1})^7$$

$$= \frac{1}{2^7}(1 + 7z^{-1} + 21z^{-2} + 35z^{-3} + 35z^{-4} + 21z^{-5} + 7z^{-6} + z^{-7}) \qquad (7)$$

This method prevents diffusion issue by accumulating value of previous output. But it s increased area and power consumption.

2.1.3 Comb filter using current input and previous input

This method can be design by figure 10. It is used equation (8), (9).

$$H_2(z) = \left(\frac{1 - z^{-8}}{1 - z^{-1}}\right)^5 = \frac{1}{2^5}(1 + z^{-1})^5 \qquad (8)$$

$$H_3(z) = \left(\frac{1 - z^{-16}}{1 - z^{-8}}\right)^7 = \frac{1}{2^7}(1 + z^{-1})^7 \qquad (9)$$

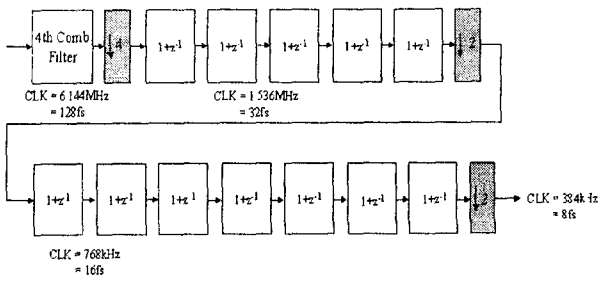

Fig. 10. Comb filter not using accumulator

This design needs to circuit to have many registers that can be store for previous value. But it does not need to multiply. In these reasons, it is efficient more than using FIR filter.

2.2 HBF(Half Band Filter)

Three HBF filter is linked by series follows comb filter. HBF filter coefficients have value of "0" in 2/n filter coefficients. Therefore can reduce number of multiplication and area of hardware and the operation amount. There are applied cases of frequency feature that lengths of pass-band and stop-band have each 1/2 of whole frequency band or ripples of stop-band have same feature[8].

Each HBF equation is as follows. HBF1 equation is equation (10) and HBF2 equation is equation (11).

$$y[n] = c_0*x[n] + c_1*x[n-1] + c_2*x[n-2] + c_3*x[n-3] + c_4*x[n-4] + c_5*x[n-5] + c_6*x[n-6] + c_7*x[n-7] + c_8*x[n-8] + c_9*x[n-9] + c_{10}*x[n-10] + c_{11}*x[n-11] \quad (10)$$

$$y[n] = c_0*x[n] + c_1*x[n-1] + c_2*x[n-2] + c_3*x[n-3] + c_4*x[n-4] + c_5*x[n-5] + c_6*x[n-6] + c_7*x[n-7] + c_8*x[n-8] + c_9*x[n-9] + c_{10}*x[n-10] + c_{11}*x[n-11] + c_{12}*x[n-12] + c_{13}*x[n-13] + c_{14}*x[n-14] + c_{15}*x[n-15] + c_{16}*x[n-16] + c_{17}*x[n-17] + c_{18}*x[n-18] + c_{19}*x[n-19] + c_{20}*x[n-20] + c_{21}*x[n-21] \quad (11)$$

Also, Figure 11, 12 and 13 show filter features by impulse response curve.

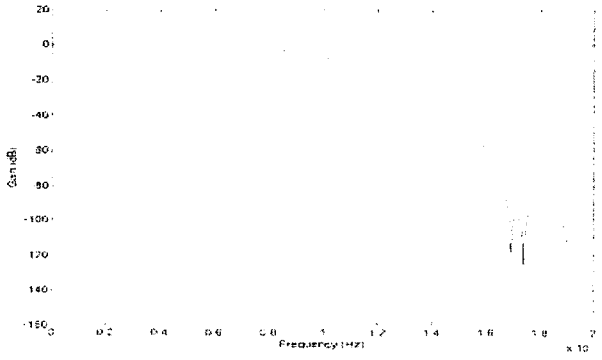

Fig. 11. HBF1 filter feature using MATLAB (16 bit coefficient)

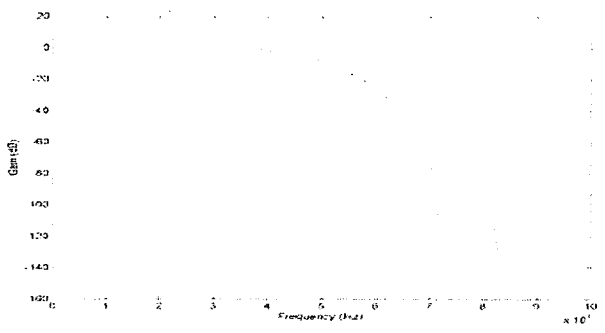

Fig. 12. HBF2 filter feature using MATLAB (16 bit coefficient)

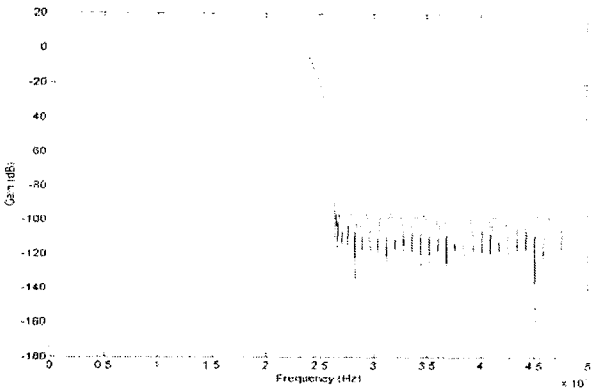

Fig. 13. HBF3 filter feature using MATLAB (24 bit coefficient)

3. SIMULATION RESULTS

Top-down design approach is used in the design of sigma-delta ADC. The logical model of sigma-delta ADC is described by using Verilog HDL at register transistor level and was verified with the Verilog XL simulator at the Cadence. Figure 14 shows a simulation result.

The verified HDL code through simulation is synthesized using STD90 standard cell libraries and Synopsys tool. Gate level verification is performed by timing information, which is extracted from netlist and gate models. Also, we are considered block test. So, There are 16-test modes. The result of simulation is well on the system clock 6.144MHz.

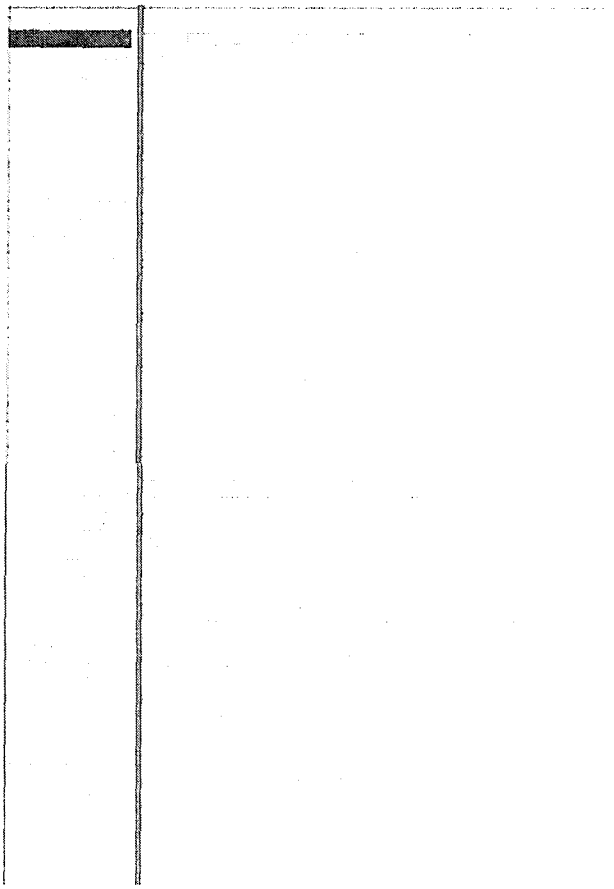

Fig. 14. Logic simulation result of the sigma-delta ADC

4. CHIP LAYOUT RESULT

Figure 15 shows a chip layout. We used the CTS (Clock Tree Synthesis) and Auto P&R with Apollo tool.

The chip is fabricated with 0.35um HYNIX standard CMOS cell library with 3.3V supply voltage and the chip size is 2000um by 2000um Symbols and Acronyms. Total 108 pins were used and the chip includes 16 test modes.

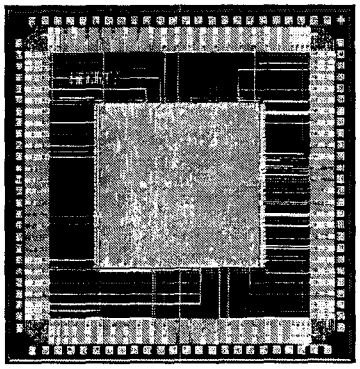

Fig. 15. Chip layout

5. CONCULUSION

In this paper, we only describe the digital block of two-channel 18-bit analog-to-digital (A/D) converter employing sigma-delta method and x128 decimation.

We designed the sigma-delta ADC using top-down design approach. In the logic simulation result and the matlab test result, we could confirm that have high SNR and performance. It proved that is suitable in audio signaling. In the near future, we will verify through the test board, which implemented FPGA logic and using ATS2 digital test equipment. Also, we will design by including macro block for high performance, low power consumption and area.

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