Design and Implementation of 160x192 pixel array capacitive type fingerprint sensor

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Abstract : This paper proposes an advanced circuit for the capacitive type fingerprint sensor signal processing and an effective isolation structure for minimizing an electrostatic discharge(ESD) influence and for removing a signal coupling noise of each sensor pixel. The proposed detection circuit increases the voltage difference between a ridge and valley about 80% more than old circuit. The test chip is composed of 160 x 192 array sensing cells (9,913x11,666 um^2). The sensor plate area is 58 x 58 um^2 and the pitch is 60um. The image resolution is 423 dpi. The chip was fabricated on a 0.35um standard CMOS process. It successfully captured a high-quality fingerprint image and performed the registration and identification processing. The sensing and authentication time is 1 sec(.) with the average power consumption of 10 mW at 3.0V. The reveal ESD tolerance is obtained at the value of 4.5 kV.

Key words : fingerprint, capacitive type, pixel array, charge sharing, image algorithm

1. ITRODUCTION

The fingerprint is known to be the most representative bio-metric for authentication of individual persons. Some research organizations have published papers on semiconductor-based capacitive sensing schemes and demonstrated the possibility of a single-chip solution. By measuring the variances of the capacitance according to the distance from the chip surface to the finger's skin, the pattern of a fingerprint, i.e., ridges and valleys, can be obtained. A capacitive fingerprint sensor converts the capacitance between the top-level metal plate of sensor and fingerprint's ridge or valley to voltage, and compares this voltage with the reference voltage and makes a binary image signal. Then, it decides whether or not the image is registered fingerprint using an authentication algorithm.

This paper proposes an advanced sensor detection circuit for the capacitive type fingerprint sensor signal processing and an effective isolation structure for removing an electrostatic discharge(ESD) influence and for removing a signal coupling noise of each sensor pixel. A detection circuit of charge sharing is proposed, which minimizes the influences of internal parasitic capacitances and amplifies the voltage difference between a ridge and valley. The test chip was fabricated on a 0.35um standard CMOS process.

2. FINGERPRINT SENSOR DETECTING CIRCUIT

The finger is modeled as the upper electrode of the capacitor, and the metal plate in the cell as the lower electrode. These two electrodes are separated by the passivation layer of the silicon chip and air. We define this series-connected capacitor Cf, which is composed of a capacitor between the metal plate and the chip surface and another one between the chip surface and finger's skin. The capacitance of Cf is at its maximum value when a ridge has contact with the passivation layer. As the distance between the chip surface and the finger's skin increases, the capacitance becomes smaller. The feedback capacitive sensing scheme, sample and hold scheme, charge transfer scheme, and charge sharing scheme have been designed to process the weak sensor signal[1][2][3][4][5].

This paper designed the advanced charge sharing scheme as shown in Fig. 1 Because the parasitic capacitance, Cp1 and Cp3 of the sensor metal plate, reduces the voltage difference between ridge and valley such as equation-1, it gives limitation in the operating range of reference voltage and becomes an important factor in fingerprint sensor's sensitivity decline.

$$V_{ridge}-V_{valley} = \frac{(C_{p2} * C_{ox}) * Vdd}{(C_{p1}+C_{p2}+C_{p3})^2 + (C_{p1}+C_{p2}+C_{p3})*C_{ox}} \quad (1)$$

Here,
C_{ox} : passivation layer capacitance
Vridge : detected voltage of ridge
Vvalley : detected voltage of valley

Usually, because Cp1 and Cp2 are the MOS transistor's source or drain capacitor, they have much smaller value than Cp3. Therefore, we need a circuit methodology to remove parasitic capacitance Cp3 that exists on the lower part of the sensor plate.

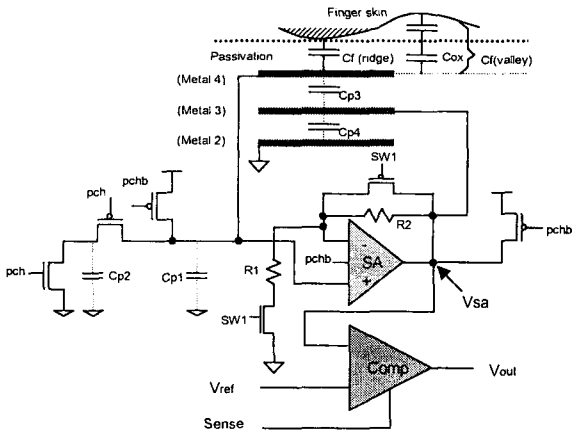

Fig. 1. Proposed detecting circuit of a charge-sharing scheme

The proposed sensor detecting circuit has three operating modes such as shown in Fig. 2. At the precharge mode, the nodes of Fig. 1 are precharged. At the unit-gain mode, the SA operates as a unit-gain buffer. The unit-gain buffer keeps the voltage difference of Cp3 to approximately 0 volt. Therefore, SA can effectively remove the influence of the parasitic capacitance, Cp3. Finally, The detected sensing voltage is greatly amplified at the amplification & sensing mode. Fig. 3 shows the SA(simple current mirrored amplifier) for the small area below the sensor plate.

To confirm this effect, we extracted each parasitic capacitance from the optimized layout of sensor 1-pixel using 0.35um standard CMOS process. Cp1 and Cp2 are 4.3fF, and Cp3 is 86fF. The Cf of a ridge capacitance is the same as passivation capacitance(Cox = 43fF). The valley is estimated as 0.1fF.

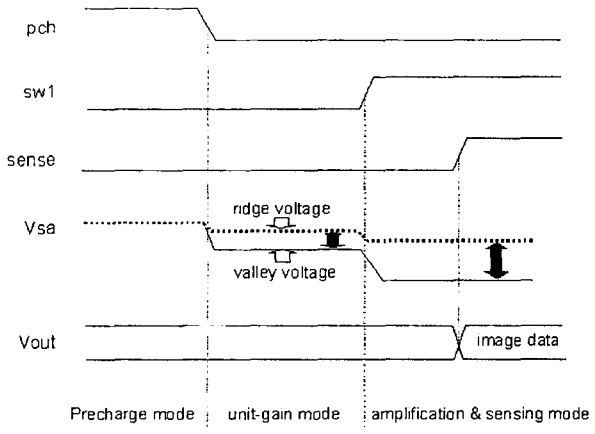

Fig. 2. Operating mode of the detecting circuit

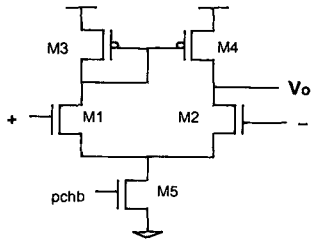

Fig. 3. Simple current mirrored amplifier(SA)

An improvement can be seen by the HSPICE simulation of the cell with condition of 0.35um typical parameter and 3.0V power supply after layout extraction in Fig. 4. The lower curve represents the output voltage when the parasitic capacitance of the sensor plate is removed and amplified the detection voltage with the proposed technique. The voltage difference between the contacted point (ridge) and the non-contacted point (valley) is more than 1.1V. Thereby, the comparator easily discriminates the ridge and valley. The upper curve represents the output voltage with the non-amplification. It would have not been easy to discriminate the pattern with the small voltage difference which is about 0.6V between the two extremes. Our method produces about 80% improvement in the voltage difference between ridge and valley. As a result, we can get high-quality images without the influence of the reference voltage(Vref) variation according to a pixel location of the sensor array.

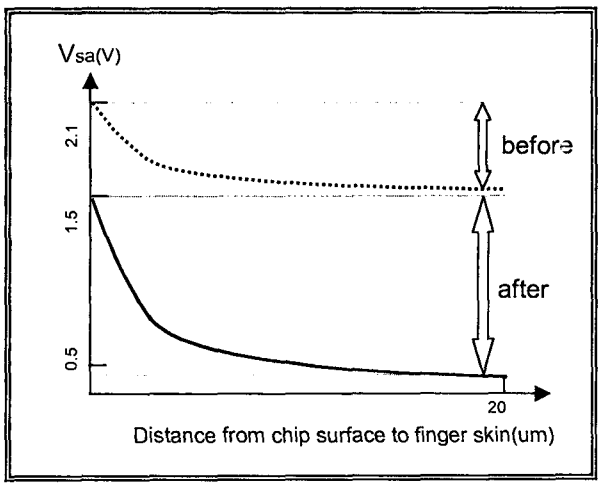

Fig. 4. Effectiveness of the sensor plate's parasitic capacitance compensation and amplification technique. (Vdd=3.0V, 0.35um CMOS typical process).

Several structures have been proposed for ESD protection, but implemented by adopting a special fabrication process[6]. In Fig. 5, we applied grounded metal2 plate and stacked VIA to remove ESD and noise, which are the most important problems in a semiconductor fingerprint sensor. The metal2 plate is used as a shielding plate for ESD protection. we also applied the grounded stacked VIA around sensor 1-pixel to protect the sensor circuit from horizontal coupling noise. As a result, Our sensor signal processing circuit becomes free of vertical and horizontal noise and ESD.

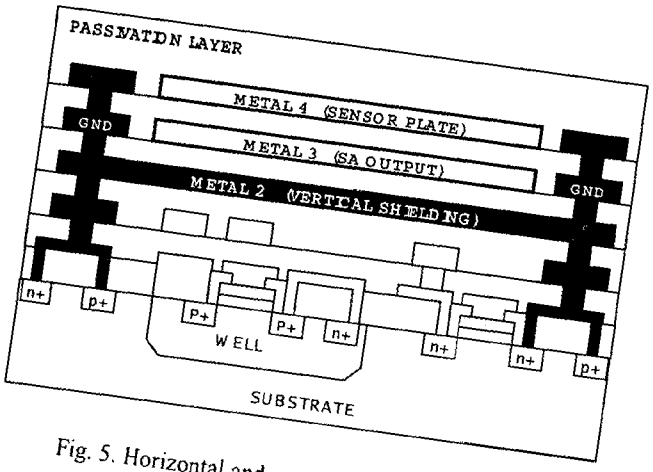

Fig. 5. Horizontal and vertical isolation structure

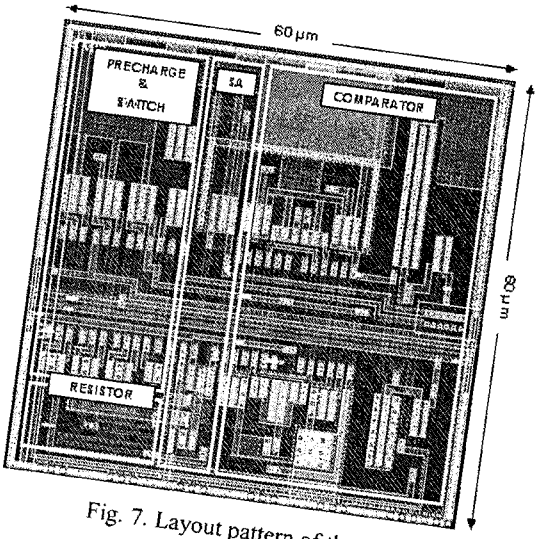

Fig. 7. Layout pattern of the pixel

3. ASIC IMPLEMENTATION OF THE FINGERPRINT SENSOR

To check the effectiveness of the proposed architecture, a test chip was fabricated using a standard 0.35um CMOS 4-metal process. Fig. 6 is a micrograph of the chip. The die size is 12 by 12.7 mm , and the sensor region is 10 by 11.7 mm. The array size is 160 x 192, and there are 30,720 pixels in the array. Each pixel contains 24 MOSFET's. The sensor plate is built above these transistors and is 60 x 60 um^2. The density of a fingerprint image is 423 dpi. The chip contains 955K MOSFETs including the controller circuit. Fig. 7 shows the layout pattern of one pixel. Fig. 8 shows the scanning electron microscope (SEM) micrograph of the pixel array and an individual pixel. The sensor plate, GND wall, and shielding metal plate are built above these circuits. One can see that the sensor plate and the ground wall are built above the logic circuit, and the sensor plate is shielded by the ground wall.

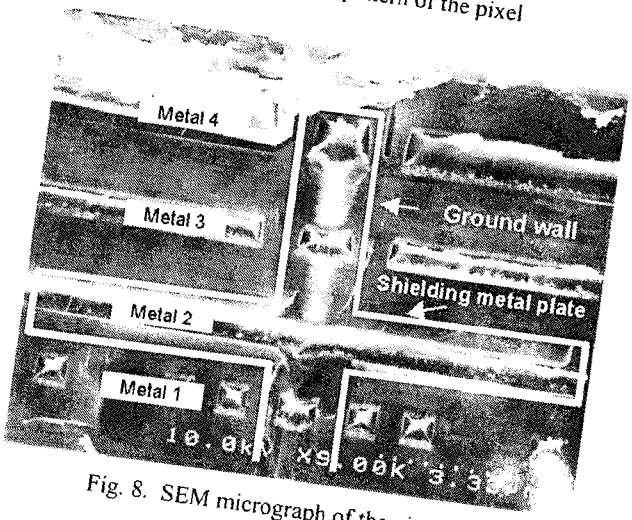

Fig. 8. SEM micrograph of the pixel array

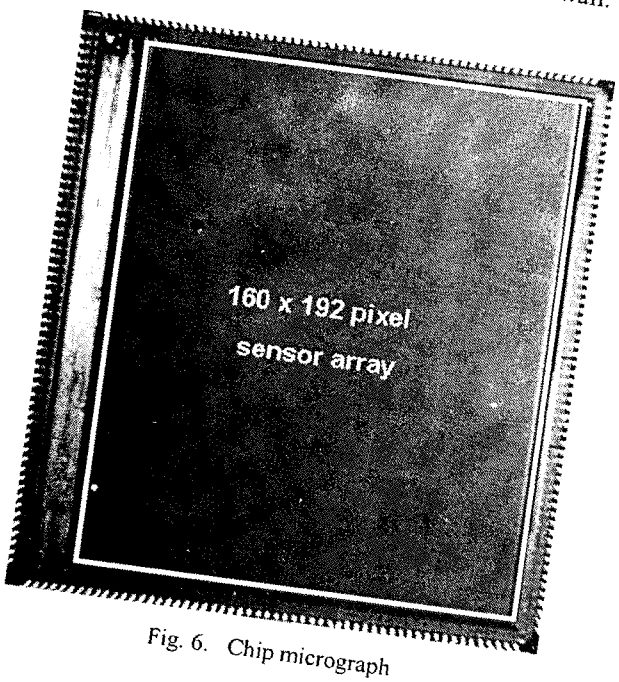

Fig. 6. Chip micrograph

Fig. 9 shows a binary fingerprint image obtained from the sensing circuits without any additional signal processing. The image confirms that the sensor and the sensing circuit can sense and binarize the fingerprint. The sensing circuit produces a binary fingerprint image in about 1.5 ms. The fingerprint identification is completed within 1 sec. The total period to sense and identify a fingerprint is 1.1 sec. The power consumption is 10 mW for sensing and identification at a supply voltage of 3.0 V. To determine the identification accuracy, we performed 200 tests. In the package, the die is placed on the PCB to help users put their finger at the chip surface(Fig. 10). For each identification, two images were sensed to get fine fingerprint image. The stranger-rejection rate was more than 99.9%, and the user-rejection rate was less than 1%.

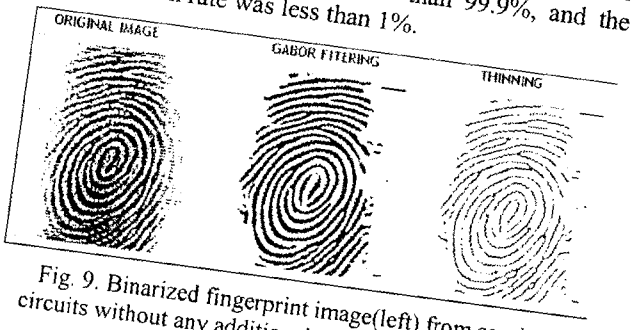

Fig. 9. Binarized fingerprint image(left) from sensing circuits without any additional signal processing, and the result of identification(center and right)

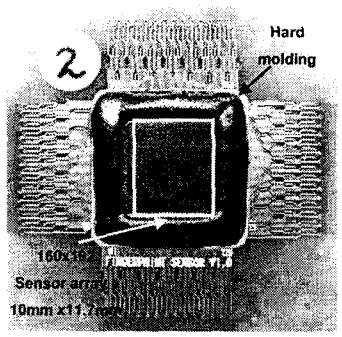

Fig. 10. Sensor package

Tolerance to ESD is necessary because otherwise, the fingerprint sensor could be destroyed by the charge from the finger. To ensure ESD tolerance, we use the GND wall and shielding metal plate structure in the sensor circuit. The GND wall and shielding metal plate are connected to the ground and surround the sensor plate to discharge the charge from the finger . The ESD tests were carried out five times using the same voltage by directly touching the sensor surface with the probe. We applied the maximum voltage of 4.5 kV to the probe electrode. Final tests were carried out at 4.5 kV. Testing of 50 samples did not produce any failures. The results indicate that the sensor did not degrade and that the ESD tolerance of the test samples could exceed 4.5 kV without failures. Fingerprint images obtained before and after the ESD tests are the same. A voltage of 2.0 kV, which is the standard in conventional LSI ESD tests, was used to test the ESD tolerance. However, even for the 4.5 kV test, the fingerprint image did not degrade, which indicates that the proposed sensor has high ESD tolerance.

These experimental results confirm that our new architecture is suitable for user authentication on small, thin, and portable equipment. The characteristics of the sensor are summarized in Table I.

TABLE I CHARACTERISTICS OF TEST CHIP

Process	0.35um standard CMOS 4-metal, 1-poly
Die size	12 mm x 12.7 mm
Sensor array area	10 mm x 11.7 mm
No. of pixels	30,720(160 x 192)
Image resolution	423 dpi
Tr. count	955,000
Pixel size	58 x 58 um^2
Pixel pitch	60 um
Time of image capture	1.5 msec
Time of identification	1.1 sec
Power dissipation	10 mW @3.0V
ESD tolerance	4.5 KV

4. CONCLUSION

This paper proposes an advanced detection circuit for the capacitive type fingerprint sensor signal processing and an effective isolation structure for removing an electrostatic discharge(ESD) influence and for removing a signal coupling noise of each sensor pixel. New detection circuit of a charge sharing minimizes the influences of internal parasitic capacitances and amplifies the voltage difference between the contact(ed) point (ridge) and the non-contact(ed) point (valley). The voltage difference is more than 1.1V. The comparator easily discriminates the ridge and valley. Our method results in about 80% improvement in the voltage difference between ridge and valley.

The test chip is fabricated on a 0.35um standard CMOS process. The test chip is composed of 160x192 array sensing cells (9,913x11,666 um^2). The sensor plate area of one-pixel is 58um x 58 um and the pitch is 60um. The image resolution is 423 dpi. The sensor chip successfully captures a high-quality fingerprint image and performs the registration and authentication processing using the identification algorithm. The sensing and authentication time is 1.1 sec with power consumption of 10 mW at 3.0V. The sensor chip was subjected to ESD test. The ESD tolerance of our chip was obtained at the value of 4.5 kV. The stranger-rejection rate of the chip is more than 99.9% and the user-rejection rate is less than 1%. These experimental results confirm that our new architecture is suitable for user identification on small, thin, and portable equipment.

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