New Wafer Burn-in Method of SRAM in Multi Chip Package (MCP)

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Abstract

This paper presents the improved burn-in method for the reliability of SRAM in MCP. Semiconductor reliability is commonly improved through the burn-in process. Reliability problem is more significant in the Multi Chip Package, because of including over two devices in a package. In the SRAM-based Multi Chip Package, the failure of SRAM has a large effect on the yield and quality of the other chips - Flash Memory, DRAM, etc. So, the quality of SRAM must be guaranteed. To improve the quality of SRAM, we applied the improved wafer level burn-in process using multi cell selection method in addition to the current used methods. That method is effective in detecting special failure. Finally, with the composition of some kinds of methods, we could achieve the high quality of SRAM in Multi Chip Package.

Key Words : burn-in, reliability, SRAM, stress

1. INTRODUCTION

Recently electronic industries aregrowing rapidly as the semiconductor technology is developed. That enables us to use many portable products cellular phone, digital camera through our living space. The trend of Semiconductor industry is developing higher- performance memory. This higher-performance memory becomes known fusion memory. Fusion Memory is the compound of Flash Memory, DRAM, SRAM, etc in a package. As using a fusion memory, the manufacturer of electronic product has the advantage of space, performance, size, and cost. Most of all, for higher-performance and capacity, the higher- density of memory is needed. So we developed higher-capacity SRAM using a SRAM interface and DRAM cell, so called 1-transistor SRAM.

In this paper, we consider seriously that the defect of each memory cause the failure of overall memory in fusion memory or Multi-Chip Package (MCP). That is the problem of reliability [1]. Semiconductor chip reliability is commonly improved through burn-in process, including high temperature, high voltage, and long time [2]. To achieve high reliability 1-transistor SRAM in MCP, we apply new burn-in method in addition to the previous method for DRAM cell.

2. CONSIDERATION OF PREVIOUS METHOD

Most of memory products are tested as follows [Fig.1].

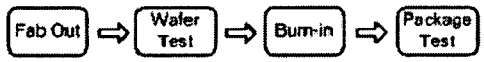


Fig. 1. Test Sequence of Memory Product

As shown in Fig.1, memory test is divided into two parts - wafer level and package level, and generally between two parts burn-in step is processed for the reliability and quality guarantee. Burn-in step has very severe condition- high temperature over 100℃, high voltage over chip power voltage [3].

2.1 Conventional Wafer Level Burn-in Method

Wafer burn-in method applied to most memory product is that each Word Line (W/L) and Bit Line (B/L) has a different electrical level and disturbs neighbor lines efficiently. Methods usually used are divided into 3 cases [4].

(i) True/Complement method
- has W/L 0, 3 and W/L 1, 2 different electrical level.

(ii) Eve/Odd method has W/L 0, 2 and W/L 1, 3 different electrical level.

(iii) Sensing method - has B/L different electrical level when reading a cell data. But, not connected to data output signal line.

Through these methods, we can give an electrical stress to memory cell with external signal for test mode in a burn-in step [5].

As a result of those burn-in cases, we can cause gate oxide failure, excess junction leakage, and inter-layer dielectric breakdown [1] [6]. In addition, after all word line is activated, we can give a stress between bit line and bit line, cell and cell through bit line sensing [Fig.2].

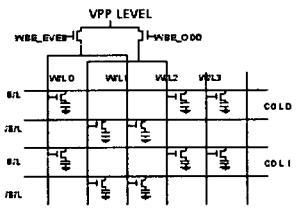


Fig. 2. Typical Schematic Structure for Burn-in

2.2 Comparison of Wafer and Package Level Burn-in

In Multi Chip Package, if any chip has a failure, other chips also go to fail. So, it is very important whether wafer level quality is reliable or not. Therefore we compare the result of package level burn-in with that of wafer level burn-in [2].

Fig. 3 shows the result of package level burn-in failure. Main portion of failure is classified into 3 types failures of bit line in cell block, single bit failure, and bit line in sensing circuit.

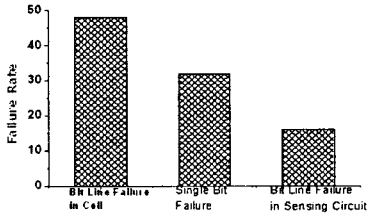
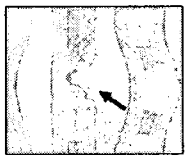
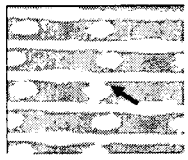


Fig. 3 Main Portion of Failure after PackageLevel Burn-in

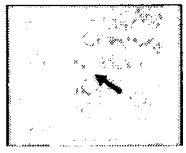
The appearances of each failure are as follows.



(a) Bit Line Failure



(b) Single Bit Failure in Cell Block



(c) Bit Line Failure in Sensing Circuit

Fig. 4. Physical Appearance of Failure after Package Level Burn-in

These features are main failure of memory product, short failure. Now, we consider the

correlation problem of both wafer level and package level. So we experiment with going onthe bath-tub evaluation by conventional wafer burn-in method.

By the condition described above, we progress bath-tub evaluation and as a result of that, we get the saturation level in 10 minutes that failures cannot occur any more [Fig.5].

As mentioned before, failure rate has become zero after 10 minutes. But failure case is different from that of package level burn-in [Fig.3]. Most different point is that the portion of bit line failure in sensing circuit is very small.

Table.1 Conventional Wafer Level Burn-in Condition

Method	Activation Cell	Cycle Time	Power
True/Comp	Half Word Line	1m sec	5.7 V
Eve/Odd	Half Word Line	1m sec	5.7 V
Sensing	Half Word Line	5m sec	5.7 V

Of course, wafer level failures may include more hard-defect. Those could be caused by the particle occurred during fabrication process. And most of particles have an effect on cell block that have the largest section of chip area. Therefore, we think that single bit failure was increased than package level.

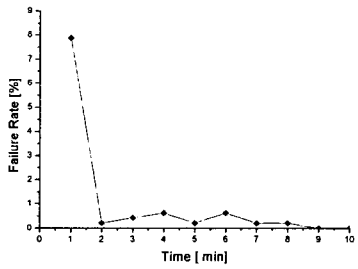


Fig. 5. Graph of Wafer Level Burn-in Bath-Tub Curve

Table.2 Failure Case After Conventional Wafer Level Burn-in

Failure case	Rate
Single Bit	46 %
Bit Line failure in Cell	41 %
Word Line Failure	5 %
Bit Line failure in Sensing Line	2%

3. IMPROVED WAFER BURN-IN METHOD

For the higher quality of SRAM in Multi Chip Package, we introduced wafer level burn-in step. But, there remain problems, not detected or not stressed failure point exists. The point not detected (shown in Fig.4. (c)) is located in the sensing circuit between data line and cell block.

To give an electrical stress to sensing line, we used a data line for write and read operation. Normally conventional burn-in method use a external signal line for only burn-in. But if we use a data line for burn-in, test time will be taken longer than before. So we selected the multi cell block at the same time to overcome the problem and through sensing line, electrically different high and low data is given. In other words, write and read operation occur normally, but at a time multi cell is selected and a data is transferred to sensing line.

In Fig.6, (1) is the failure point of "bit line failure in sensing circuit". This point is the location where data from cell block is transferred to output signal line. CSL is gate signal between cell data line and output signal line. Fig.4 (c) shows that short failure occur between CSL gate and sensing line contact. Inter-layer dielectric was broken between two points and Tungsten contact met the gate poly slightly.

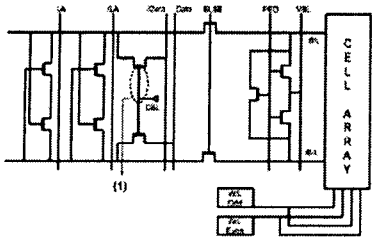


Fig. 6. Location of Bit line Failure in Sensing Circuit, [Defect Point : (1)].

For improved method, some circuitry was inserted, but area overhead is insignificant and tiny. Only a small number of address decoder is disabled for multi cell selection and almost normal operation is implemented.

Table.2 Failure Case After Improved Wafer Level Burn-in

Method	Failure #, After Wafer Burn-in	Single Bit	Bit Line	Sensing Circuit
True/Comp.	35	19	16	0
Even/Odd	27	13	14	0
Sensing	47	26	21	0
New Method	40	24	13	3

Table.3 shows a result of wafer level burn-in after improved method is inserted. The result indicates thatonly new method detects bit line failure in sensing circuit. Conventional methods also detect most failure, but because of using only word line and bit line in cell block, those methods cannot detect the sensing line failure in core area.

Through accurate failure analysis and modeling, we adopt improved wafer level burn-in method and achieved the accordance of wafer and package level burn-in failure.

4. SUMMARY

This paper presents improved method for wafer level burn-in technique. External environment and internal schematic revision are all included. By that method, we can detect the special failure that cannot be caught by conventional methods. In particular, two ideas are proposed for the detection of particular failure. Those are the use of data line for burn-in signal and multi cell selection at a time. Finally we achieve device reliability in wafer level almost reaching package level. The reason that a kind of work is needed is because this product is for multi chip package.

ACKNOWLEDGEMENT

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