# Quadrature Phase Detector for High Speed Delay-Locked Loop

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*Abstract*—**A Quadrature phase detector for high-speed delay-locked loop is introduced. The proposed Quadrature phase detector is composed of two nor gates and it determines if the phase difference of two input clocks is 90 degrees or not. The delay locked loop circuit including the Quadrature phase detector is fabricated in a 0.18 um standard CMOS process and it operates at 5 GHz frequency. The phase error of the delay-locked loop is maximum 2 degrees and the circuits are robust with voltage, temperature variations.**

## I. INTRODUCTION

In recent years, demand for wireless equipment such as wireless LAN and cellular phone has been increased. For wireless equipment, a high dynamic range and high modulation accuracy are important. A quadrature modulator scheme is one of the key factors of the system because the modulator dominates the quality of modulated signal. A direct conversion de-modulation is one of the popular scheme because of its compactness and low cost. However, the direct modulation has modulation accuracy problem because it is difficult to obtain precise quadrature signals at high frequencies. Therefore, it is an important factor for the wireless equipment to generate signals that has 90 degree phase difference.

To generate quadrature signals is also important in wireline communication area such as high speed DRAM and Ethernet. In order to achieve high speed data transfer, the operation speed of the clock generation circuits such as PLL ( Phase-Locked Loop) and DLL (Delay-Locked Loop) should be increased. In this paper, a Quadrature phase detector for high speed DLL is described. The proposed phase detector includes two nor gates that operates at 5 GHz frequency.

## II. Quadrature Phase Detector

### *A. Typical quadrature phase detector*

Fig. 1. shows a typical quadrature phase detector that has been used in high speed clocking circuits. This circuit compares two input signals and determine if the two input signals has 90 degree phase difference or not. The operation of the phase detector is described in Fig. 2. Fig. 2. (a) shows the input clocks has 90 degree phase difference. In this case, the increasing time and the decreasing time of the *VOUT1* signal is identical. Therefore, the voltage level of the output signal is maintained. However, in Fig. 2. (b), the increasing time and the decreasing time of the *VOUT1* signal is different. This voltage level difference is transferred to clock generation circuits. This circuit is basically complex and therefore, it is not suitable for high speed operation.

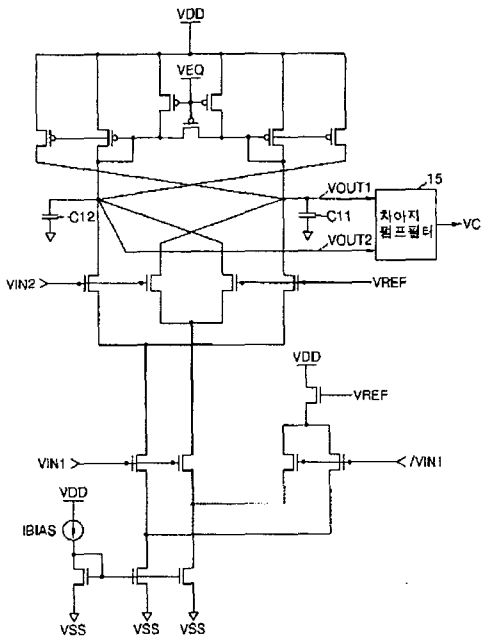
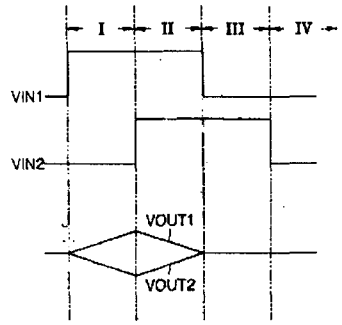
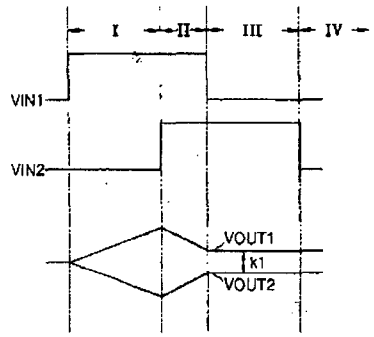



Fig. 1. Typical quadrature phase detector




(a)When the input signals has 90 degree phase difference




(b) When the input signals hasn't 90 degree phase difference

Fig. 2. Operation of the typical quadrature phase detector

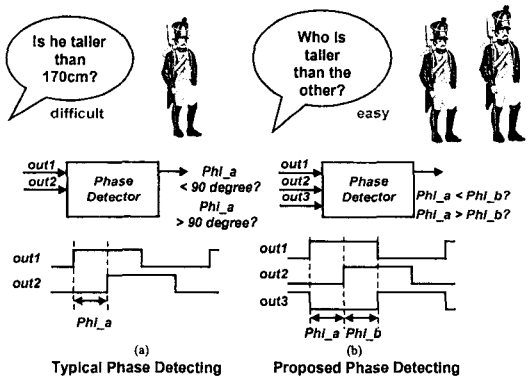



Fig.3. Phase detecting methods comparison

### *B. Relative comparison*

In high speed clock generation circuit such as DLL, phase comparison between two high speed clocks is difficult to implement. In this paper, a relative comparison instead of typical absolute comparison is used. The relative comparison is more accurate than the absolute comparison. Fig. 3. shows the case. If a person is asked to decide if a man is taller than 170 cm or not, it is difficult to answer. However, if the question is changed to "Who is taller than the other?" it is relatively easy to answer. In this paper, the relative phase comparison is used in order to operate at high speed such as 5 GHz.

### *B. Circuits*

The proposed Quadrature phase detector is described in Fig. 2 that shows a DLL circuit diagram. The DLL circuit is composed of phase detector, charge pump, and loop filter. The phase detector consists of two nor gates that compares the phase difference of three input signals. In this diagram, *out3* signal is inverted version of *out1* signal.

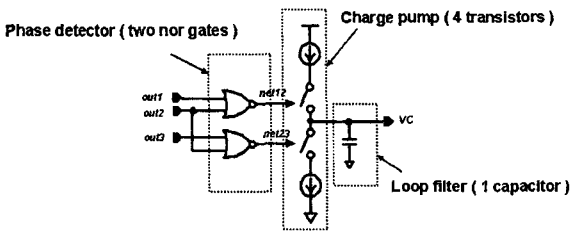
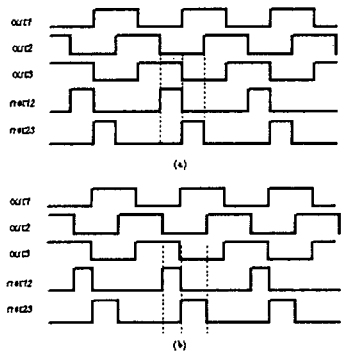



Fig. 4. DLL circuit diagram with proposed Quadrature phase detector.

### *C. Operations*

The operation of the phase detector and charge pump is shown in Fig.5. Fig.5. (a) illustrates the case of all signals have 90-degree phase difference. Inorder to compare the relative phase differences, the detector needs three input signals as shown in the diagram. The pulse widths of *net12* and *net23* represent the phase difference between *out1* and *out2*, *out2* and *out3* respectively. Since each signal has the same phase difference, *net12* and *net23* are identical, so the final control voltage remains unchanged. In Fig.5. (b), the signals have different phase difference. Since the phase difference of out1-out2 is larger than out2-out3, the pulse width of *net23* is wider than that of *net12*, which induces a charge pump current imbalance. The operation of the charge pump is illustrated in Fig. 6. The upper part of the diagram shows the charge pump current. If the clock phases are not evenly distributed, the charge pump currents flow as shown in the figure. The lower part of the diagram shows the control voltage output. Due to the charge pump imbalance, the control voltage decreases in this case.




**Timing Diagram**
(a) Same phase difference
(b) Different phase difference

Fig.5. DLL operation timing diagram
(a) same phase difference
(b) different phase difference

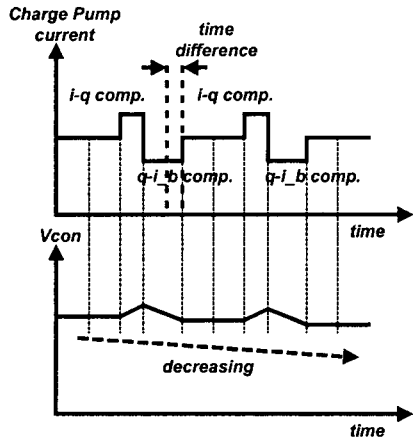



Fig. 6. Operation of the charge pump

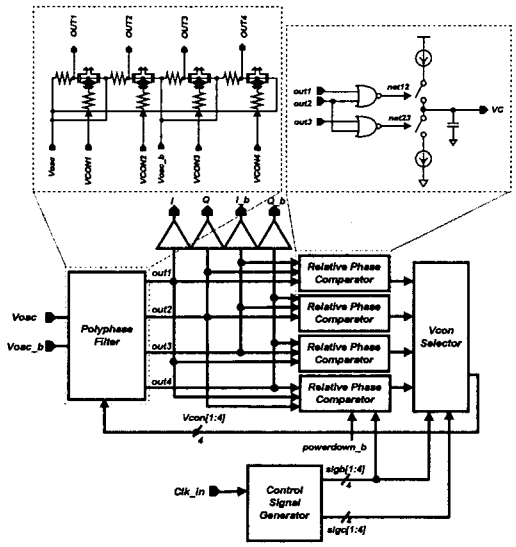



Fig. 7. Example of the quadrature signal generation system.

An example of the quadrature signal generation system is described in Fig. 7. This system generates four different signals that has 90 degrees phase difference respectively.

## III. Experimental Results

The DLL loop operation is proved by simulation. Fig. 8 shows the simulation results of the DLL loop. In this diagram, the upper left part of the diagram shows initial state of the output signals. They have 21 degree phase offset. The upper right part of the diagram shows the final phase offset. In this case, the phase offset is 0.3 degree. The lower left part shows the output signals after buffer and the lower right part shows the control voltage variation with respect to time.

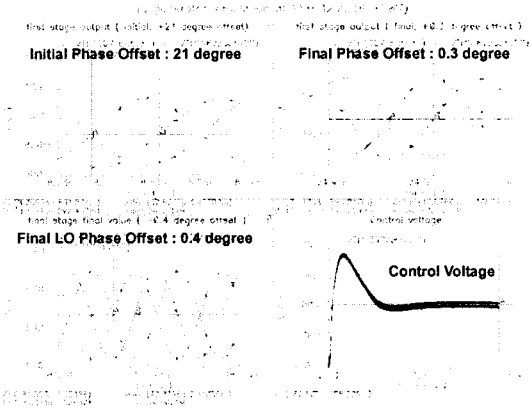



Fig. 8. Simulation results of the DLL loop

The quadrature phase detector is fabricated in 0.18um CMOS process. To prove operation of the circuit, the DLL loop is measured. The output waveforms of the DLL were measures with an oscilloscope. They are supposed to have 90 degree difference. The experimental results are shown in Fig. 9. It shows the measured quadrature signals when the input frequency is in the 5-GHz band. It shows 90 degree phase difference and matched amplitude between two signals.

## IV. CONCLUSIONS

A quadrature phase detector was proposed and implemented. The maximum phase error is 2 degree and the amplitude error is less than 0.5 dB. The proposed phase detector can be used not only wireless applications but also high speed wire line inter chip communications.

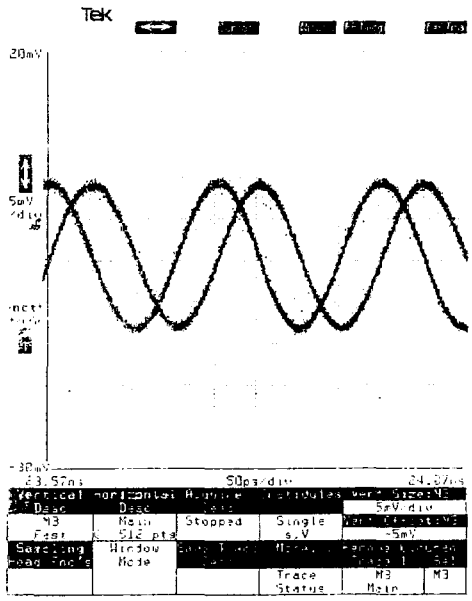



Fig. 9. Measured output waveforms of the DLL

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