Fabrication of Colloid Thrusters using MEMS Technology

Kun Joong Park and Seung Jin Song
School of Mechanical and Aerospace Engineering, Seoul National University
Seoul 151-742 KOREA
sjsong@snu.ac.kr

Manuel Martinez-Sanchez
Department of Aeronautics and Astronautics, Massachusetts Institute of Technology
Cambridge, MA 02139 USA
mmart@mit.edu

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Abstract

This paper presents the preliminary fabrication results of colloid thrusters which can provide thrust of the order of micro to milli-Newtons. MEMS technology has been used for fabrication, and four essential fabrication techniques - deep etching with nested masks, isotropic plasma etching, anisotropic reactive ion etching, and direct fusion wafer bonding - have been newly developed. Among diverse models which have been designed and fabricated, the fabrication results of 4-inch wafer-based colloid thrusters are presented.

Introduction

Colloid thrusters are electrostatic accelerators of charged liquid droplets. They were first proposed and then intensively studied from around 1960's to 1970's as an alternative to normal ion engines. Their appeal at that time rested with the large molecular mass of the droplets, which was known to increase efficiency and thrust density (thrust per exhaust area) because of high mass to charge ratio. However, the required acceleration voltage was also increased to around 10 to 100 kV to accomplish 1000 seconds of specific impulse (exhaust velocity over gravity acceleration) for space missions. Thus, problems with insulation and packaging were created. In addition, a liquid-dispensing emitter provided such a low thrust on the order of micro-Newtons that a fairly massive array of emitters was required, which further discouraged implementation[1].

After lying dormant for over 20 years, the interest in colloid thrusters has been renewed because of recent emphasis on spacecraft miniaturization. Specifically, very small thrust per emitter for fine controllability and high specific impulse are needed for space missions[1]. Also, advances in electrospray science for biological applications (i.e., mass spectrometry for the extraction of charged biological macromolecules from liquid samples) allow thruster operation at more comfortable voltages (1 to 5 kV)[1-2]. Furthermore, the rapid growth in semiconductor manufacturing industry yielded new practical fabrication technologies for micro-electro-mechanical systems (MEMS)[3]. Therefore, it is now possible to mass-produce arrays of liquid-dispensing emitters with a diameter of several micrometers. Besides, colloid thrusters have the possibility to produce thrust ranging from micro to milli-Newtons with the same engine and propellant, allowing one engine to perform multiple missions from precise disturbance cancellation to prime propulsion[4].

Electrospray

Figure 1 shows an electrically-driven colloid jet from a single emitter. The emitter's diameter is 30 μm, and the jet radius is less than a micron[5]. The sequence of generation of such a cone-jet is as follows[5-7]. The convex meniscus of charged liquid at the tip of a capillary emitter deforms in the electric field direction when exposed to a high electric potential difference (at least more than 1 kV). It continuously changes shape into a cone (the so-called the Taylor cone named after G. I. Taylor who predicted the cone semi-angle in the 1960's), and finally a very thin jet emits from a cone apex under certain values of voltage (extraction starting voltage). A liquid jet collapses into a spray of droplets due to inherent surface tension instability and coulombic repulsion, and thrust is achieved by this spray formation.

Design

A generic schematic of colloid thrusters is shown in Figure 2. Before formation of an electrified jet, conductive liquid contained in a tank fills channels by capillarity and there is a pressure difference between the tank and channel exits. A convex meniscus forms at the channel tip (emitter) due to surface tension, and is pulled outward when an electric potential difference is applied between the liquid and the extraction electrode. At sufficiently high voltage differences, a jet emits from the Taylor cone apex, and thus acceleration mode is achieved[4-5].

To implement this system with silicon wafers, wafer-bonded systems have been designed[8]. Two wafers having the same features except propellant inlet holes are bonded, and cut into eight colloid thrusters. Each colloid thruster is composed of a tank, intermediate reservoirs, and emitter channels, all of which are hydraulic features. Due to insulation problems, the electric part, including electrodes, is fabricated separately.

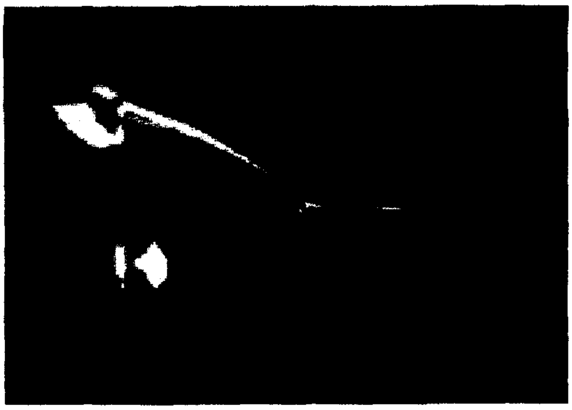

Fig. 1 Photograph of a single emitter colloid jet[5].

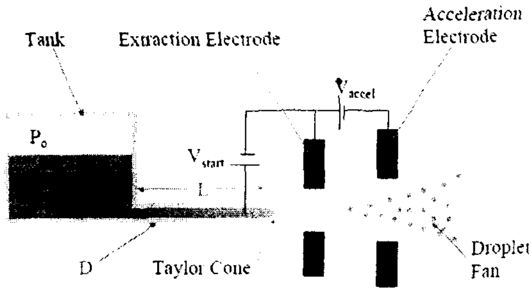

Fig. 2 Schematic of colloid thrusters.

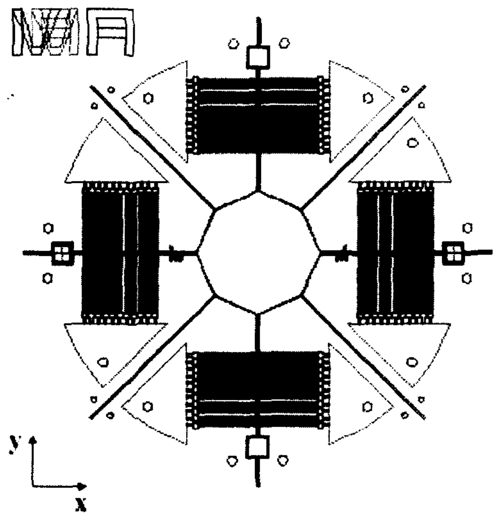

Fig. 3 Overlapped six masks for microfabrication.

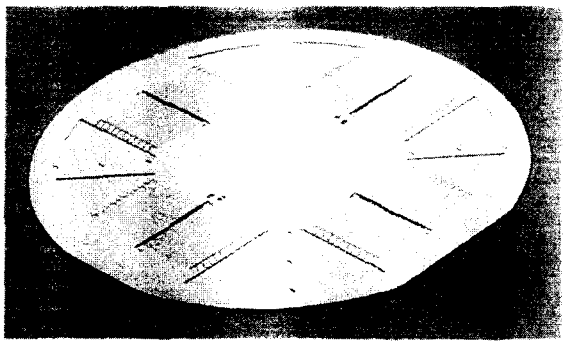

Fig. 4 A fabricated wafer before bonding process.

An overlapped CAD drawing of six masks for microfabrication on 4-inch wafers is shown in Figure 3. Separate masks are needed for fabrication of the alignment key, emitter channels, intermediate reservoirs, tanks, and propellant inlet holes. In the figure, the triangles are the tanks. Each tank is connected to 11 intermediate reservoirs, and each intermediate reservoir is connected to 12 emitter channels. Thus, one colloid thruster has 132 emitter channels. The emitter diameter at 13 μm is the minimum feature size.

Fabrication

Figure 4 shows a fabricated wafer which contains 8 thrusters. Another wafer having the same features but holes for the inlet of liquid propellant was bonded to this wafer. The close-up views of the tanks, intermediate reservoirs, and emitter channels are shown in Figures 5, 6, and 7, respectively. Since the depth of each feature is different, it seems that they are disconnected from one another at the interfaces. The depths are 120 μm, 60 μm, and 6.25 μm, respectively. All of features were fabricated by dry etching.

Deep Etching

For very deep etching (e.g., an etching depth of over about 100 μm), photoresist alone is not usually used for etching masks. The reason is due to the limit of photoresist thickness and vulnerability to burns in the etching chamber. Thus, a silicon oxide (SiO_2) film or a combination of silicon oxide and photoresist is used as an etching mask. Even in the case that the etching depth is not very large, silicon oxide etching masks are preferred, because they can have vertical sidewalls of etching mask opening[9-11]. Compared to this, the sidewalls of etching mask opening developed with thick photoresist (e.g., AZ P4620) are not typically vertical as seen in Figure 8, thus, a problem with etching accuracy arises[12]. In fact, although the fabrication of intermediate reservoirs did not need critical dimension control, for the next upgraded design and fabrication, we used silicon oxide films as etching masks for intermediate reservoirs as well as tanks.

In the early stage of fabrication development, tanks and intermediate reservoirs were etched individually, and details of etching processes were almost the same but etching depths. The brief etching procedures for both features were 1) silicon oxide coating on silicon substrate by plasma-enhanced chemical vapor deposition (PECVD) 2) photoresist coating on the silicon oxide film, 3) photolithography for patterning, 4) etching the silicon oxide to make

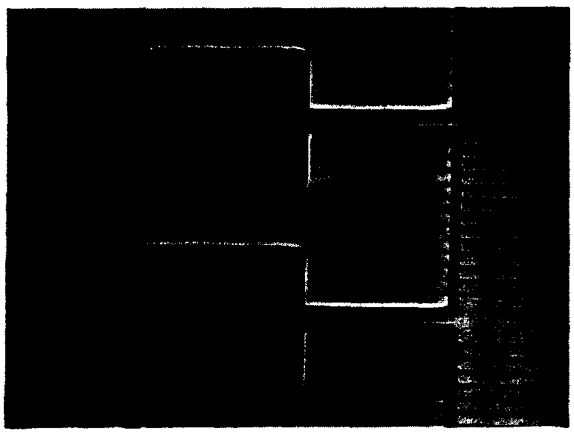

Fig. 5 120 μm deep tank (A), 60 μm deep intermediate reservoirs (B), and 6.25 μm deep emitter channels (C).

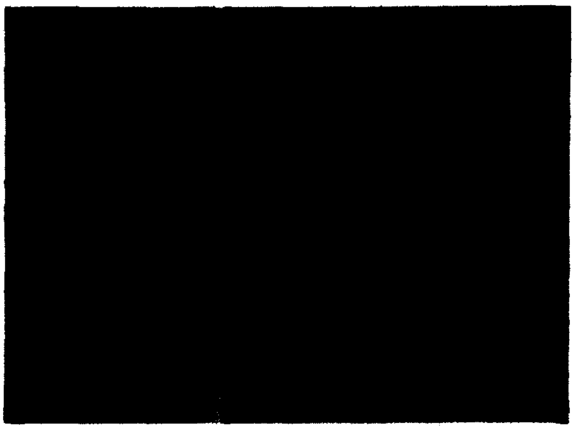

Fig. 6 Intermediate reservoirs and emitter channels.

Fig. 7 Emitter tips with 13 μm diameter. The direction of liquid jet is from the left to the right.

etching mask for the silicon substrate, 5) etching the silicon substrate for features, and 6) removal of the silicon oxide etching mask. Fabrication of each feature requires one loop of all the procedures described above and thus is difficult and costly in time and expense.

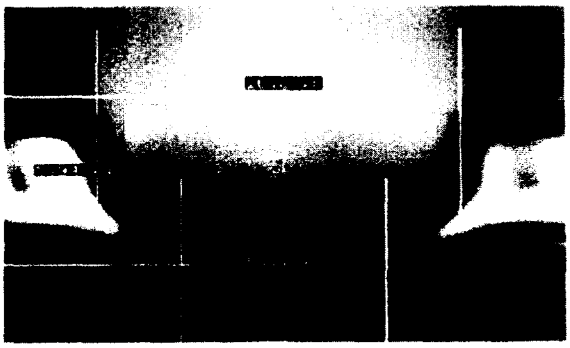

Fig. 8 Etching mask opening of thick photoresist[12].

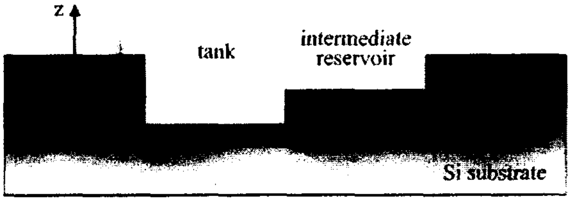

Fig. 9 Side view sketch of the etched tank and intermediate reservoir.

Therefore, the etching technique with nested masks was designed and used to reduce those unfavorable respects[11]. This technique might be applied to etching wafers, which have different depth features, like our system, and was used for etching tanks and intermediate reservoirs (Figure 9). The new procedures included 1) silicon oxide coating on the silicon substrate, 2) photoresist coating on the silicon oxide film, 3) photolithography for patterning both tanks and intermediate reservoirs, 4) etching the silicon oxide to make etching mask for both features, 5) second photoresist coating, 6) photolithography for only the patterning of the tanks, 7) etching the tanks to the depth of 60 μm (the depth difference between tanks and intermediate reservoirs), 8) removal of the second photoresist, 9) etching both tanks and intermediate reservoirs to the depth of 60 μm, and 10) removal of the silicon oxide etching mask. It may appear that this technique is similar to individual fabrication. However, the silicon oxide coating process includes a slow annealing process; therefore, the former is much better than the latter. In addition, by reducing the required number of coating and removal of the silicon oxide film, the features on the substrate surface can be better protected from the harmful fabrication environment (e.g., liquid etchants and plasma). Moreover, this technique might solve the problem of photoresist coating of wafers which have undergone a previous deep etching[11]. Currently, there are problems with photoresist coverage around and inside the etched features.

Tanks and intermediate reservoirs were etched by the deep reactive ion etching (DRIE) technique, and a Surface Technology Systems multiplex Inductively Coupled Plasma Etcher was used. Specifically, the

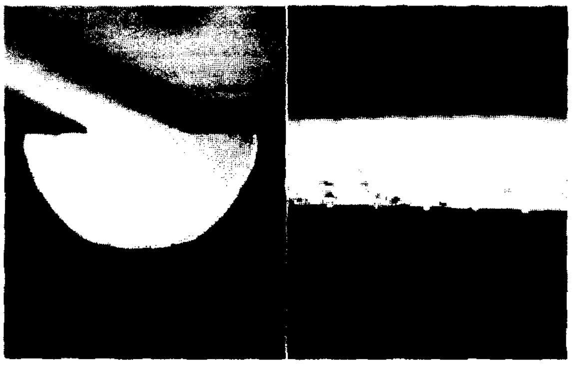

Fig. 10 Cross-sectional view of cut-off emitter channels before removal of the SiO_2 etching mask.

so-called Bosch process, which consists of alternating steps of reactive ion etching in SF_6 plasma and polymer deposition (passivation) from C_4F_8 plasma, was used. During this process, bottom walls of features are etched much more rapidly than sidewalls, thus tank and intermediate reservoirs having nearly vertical sidewalls were achieved[10-13]. Machine operating conditions (i.e., gas flow rate, activation time, overlap time, electrode power, and automatic pressure control valve position) were set by a previously developed recipe, which is known as MIT59, and those were 105 sccm of SF_6 (14 second etching, 0.5 second overlap, 12 W electrode power, and 750 W coil power), 40 sccm of C_4F_8 (11 second passivation, no overlap, 6 W electrode power, and 600 W coil power), and 65° of automatic pressure control valve position. The etching depth was controlled by elapsing process time, and the average etch rate was about 2 μm/min.

Isotropic Etching and Reactive Ion Etching

Figure 10 is a cross-sectional view of cut-off emitter channels before removal of the silicon oxide etching mask. The diameter of emitters was 13 μm, and the opening width of the etching mask was 5 μm. In the figure, the cross-sections of channels are quite semi-circular, indicating good fabrication results. By bonding the two wafers, channels having circular cross-sections were achieved.

For the isotropic etching, the plasma etching technique with an Applied Materials Precision 5000 Etcher was used, and etching gas (plasma source) was SF_6. Generally known mechanism of this etching process is as follows[9-10]. First, generated etchant species in plasma diffuse and adsorb to the substrate. Second, they react with the surface of the substrate. Finally, the reaction products, which are volatile, leave the surface by desorption and diffusion. Since this etching mechanism varies significantly as changes in gas excitation energy and pressure inside the chamber, those parameters were carefully tuned to realize the semi-circular cross-section channels (150 Watt and 120 mTorr, respectively)[9]. If gas excitation energy increases, or pressure inside the chamber decreases, a flux of reactive ions has directionality, and physical etching (ion bombardment to the surface) plays a key role in etching as well as chemical etching. As a result, etching is performed anisotropically, and thus, nearly vertical sidewall features can be produced[9-10]. This process is called reactive ion etching (RIE), and used for etching silicon oxide etching masks with CF_4 gas.

Wafer Bonding

Another essential process was wafer bonding. After wet oxidation, by which silicon oxide was thermally grown on the surface, wafers were bonded by the direct fusion bonding technique. Since the bond strength critically depends on wafer surface condition (e.g., roughness, flatness, and contamination state), chemical mechanical polishing (CMP) and RCA cleaning were performed prior to bonding[9-11]. An Electronic Visions EV450 aligner and an AB1-PV bonder were used for direct bonding, and their alignment tolerance was 0.5 μm. Since van der Waals forces, which keep wafers bonded, are not strong, wafers were annealed at high temperature (1050 °C). During this annealing process, silicon-oxygen-silicon bond is formed by dehydration at the surface, thus the bond strength is much enhanced[9-10].

Conclusion

4-inch silicon wafer-based colloid thrusters have been fabricated using MEMS technology. Efficiency and quality of deep etching have been achieved by use of nested masks. Furthermore, circular cross-sections of emitter channels have been realized by isotropic plasma etching. In addition, anisotropic reactive ion etching for silicon oxide etching masks and direct fusion wafer bonding have been developed well. Efforts are underway to develop advanced models.

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