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DESIGN AND IMPLEMENTATION OF ON-BOARD COMPUTERS FOR STSAT-2

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ABSTRACT

The Engineering Model of on-board computer was developed and tested completely with other sub-systems for STSAT-2. We designed the on-board computer of STSAT-2 which has some improved features compared with that of STSAT-1. A remarkable change is that the on-board computer has a structure of centeralized network communication without a Network Controller of the STSAT-1. That is, the on-board computer directly manages a satellite network. In addition, as many logics are implemented by Field Programmable Gate Array, so we can reduce the weight and size of on-board computer. Also, the developed on-board computer has more improved tolerance against Single Event Upsets and faults than that of the STSAT-1.

Keywords: satellite system, on-board computer, STSAT-2, fault tolerant system

1. INTRODUCTION

The on-board computer (OBC) play an important part in a small satellite with the following functions: communicate with the ground station (GS), store the data of spacecraft and payload, transmit to GS on command, manage spacecraft and payload, and provide the system of operation for flight software (Kim et al. 1996). The OBC therefore needs an ability of high performance calculation and high reliability. Moreover, the OBC must be designed to operate without errors under poor space environment (Kwak & Park 2004).

We consider the structure of a centeralized network communication to solve various problems occurs in the communication of the satellite network. The network controller (NC) was included in OBC of STSAT-1 to access the satellite network with high speed (Kwak et al. 2003). However, there is no a counter-plan against emergencies, such as mechanical troubling of NC. Therefore, we are designed to access the satellite network directly by the OBC.

On the other hand, we reduce the size and weight of the OBC by using Field Programmable Gate Array (FPGA). The satellite network is built in the FPGA. The error detection and correction (EDAC) and watchdog logic is also embedded. In addition, we use an improved method of recovery against Single Event Upsets (SEUs).

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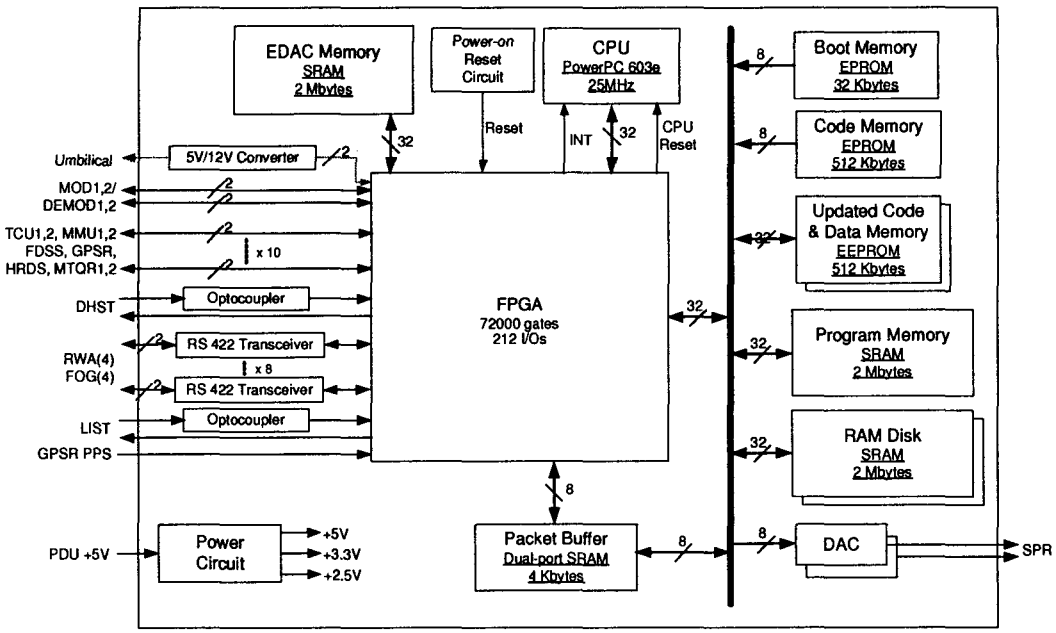

Figure 1. On-board computers architecture for STSAT-2.

In the next section, we describe the OBC architecture for STSAT-2.

2. SYSTEM CONFIGURATION

The STSAT-2 has the redundant OBC and operates as the mode of Cold Standby. The OBC of STSAT-2 consists of CPU, Program Memory, EPROM, RAM Disk, EEPROM and FPGA. The architecture of OBC is shown in Figure 1.

2.1 CPU

We use MPC603e microprocessor as the CPU. The MPC603e is a low-power implementation of the microprocessor family of reduced instruction set computing (RISC) microprocessor. The MPC603e implements the 32-bit portion of the PowerPC architecture, which defines 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. The external clock is 25[MHz] and internal CPU clock is 150[MHz]. The ability of computation is more than 150[MIPS] with 2.5W power consumption.

2.2 FPGA

We use Actel's RT54SX-S as the FPGAs for space applications. Many logics are implemented by FPGAs:

- EDAC logic against SEUs,
- Watchdog logic,
- Pulse Per Second (PPS) counter of GPS,
- Universal Asynchronous Receiver/Transmitter (UART) protocol logic,

- Serial Line Internet Protocol (SLIP) logic,
- Interrupt Controller (IC) logic.

SEUs can cause critical errors in the memory of OBC. We therefore implement EDAC logic to cope with SEUs in the FPGA, using the Hamming code method which consists of 4bit data and 3bit information.

The watchdog is a general logic to reset of the OBC when the CPU is halted by unknown system faults.

The interrupt controller logic is built in FPGA to handle the 43 external interrupts. This logic will be under control of the flight software which reads and analyzes the register of interrupt status.

2.3 MEMORY

The memory of OBC consists of Program memory 2MB, RAM memory 2MB for EDAC, RAM disk 4MB, Boot ROM EPROM 32KB, EPROM 1MB for storing OS kernel and tasks, and EEPROM 2MB for upgrade.

The program memory of OBC has the storage of 2MB and is protected by EDAC logic. We store the data of spacecraft and payload in the Ram disk, and these data are protected by EDAC algorithm based on Reed-Solomon Code.

3. CONCLUSIONS

We developed the EM of OBC for STSAT-2. We fully tested without errors under completed integration. The OBC of STSAT-2 designs in the small size and simple structure corresponding to small satellite. We implement many logics using FPGAs. Therefore, we reduce the complexity of system and then increase the stability of system under space environment. As with high performance CPU, we also improve the processing ability of the OBC.

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