

## **IO Board Design of Next Generation Satellite using the Space Wire Interface**

**Ki-Ho Kwon, Day-Young Kim, Seung-Woon Choi, Jong-In Lee**

Satellite Electronics Department, Satellite Technology Division,  
Korea Aerospace Research Institute(KARI), Daejeon, 305-333, Korea  
E-mail: khkwon@kari.re.kr

This paper presents a feasibility study of an advanced IO board design for the next generation of low-earth orbit satellites. Advanced IO board design includes sensor interface, A/D, D/A, Digital Module, Serial Module etc, and allows to process increasing data rates between IO board and CPU board. The higher data rate involved in modern IO board additionally introduce issues such as noise, fault tolerance, command and data handling, limited pin count and power consumption problems. The experience in KOMPSAT-1 and 2 program with this kind of problems resulted in using SMCS chip set, a high speed serial link technology based on IEEE-1355(Space Wire Protocol)[1,5], as a standard for next generation of satellite IO board design.