A High-performance X/Y-axis Microaccelerometer Fabricated on SOI Wafer without Footing Using the Sacrificial Bulk Micromachining (SBM) Process

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Abstract: In this paper, a x/y-axis accelerometer is fabricated, using the SBM process on a <111> SOI wafer. This fabrication method solves the problem of the footing phenomenon in the conventional SOI process for improved manufacturability and performance. The roughened lower parts as well as the loose silicon fragments due to the footing phenomenon are removed by the alkaline lateral etching step of the SBM process. The fabricated accelerometer has a demodulated signal-to-noise ratio of 92 dB, when 40Hz, 5 g input acceleration is applied. The noise equivalent input acceleration resolution and bandwidth are 125.59 μg and over 100 Hz, respectively. The acceleration random walk is 12.5 μg/$\sqrt{Hz}$. The output linearity is measured to be 1.2 % FSO(Full Scale Output) at 40 Hz, and the input range is over $\pm$ 10g.

Keywords: x/y-axis accelerometer, Sacrificial Bulk Micromachining(SBM), footing.

1. INTRODUCTION

Many recent studies on the microaccelerometers have been focused on the reduction of the mechanical noise by increasing the proof mass [1-3], and the most popular process to achieve this is deep silicon RIE with SOI wafer. In the conventional SOI process, however, the charging of the buried oxide layer during the deep silicon RIE leads to the well-known footing phenomenon [4]. This footing phenomenon results in the unwanted lateral and reverse directional etching of silicon at the silicon/oxide interface. This footing makes the bottom surface roughened and distorted, and it can significantly change the design specifications of devices. A more severe problem of footing is that the silicon fragments separated from the bottom part of the structure float around and cause an electrical short between electrodes.

In this paper, a high-performance microaccelerometer is fabricated by the Sacrificial Bulk Micromachining (SBM) process on a SOI wafer with a (111) device layer. The roughened lower parts as well as the loose silicon fragments are removed by the alkaline lateral etching step of the SBM process [5-9].

2. DESIGN AND FABRICATION OF X/Y-AXIS ACCELEROMETERS

Figure 1 shows the schematic of the accelerometer and capacitive readout circuit. The designed accelerometer consists of proof mass, flexures and sensing combs. The inertia force exerted by applied acceleration compels the proof

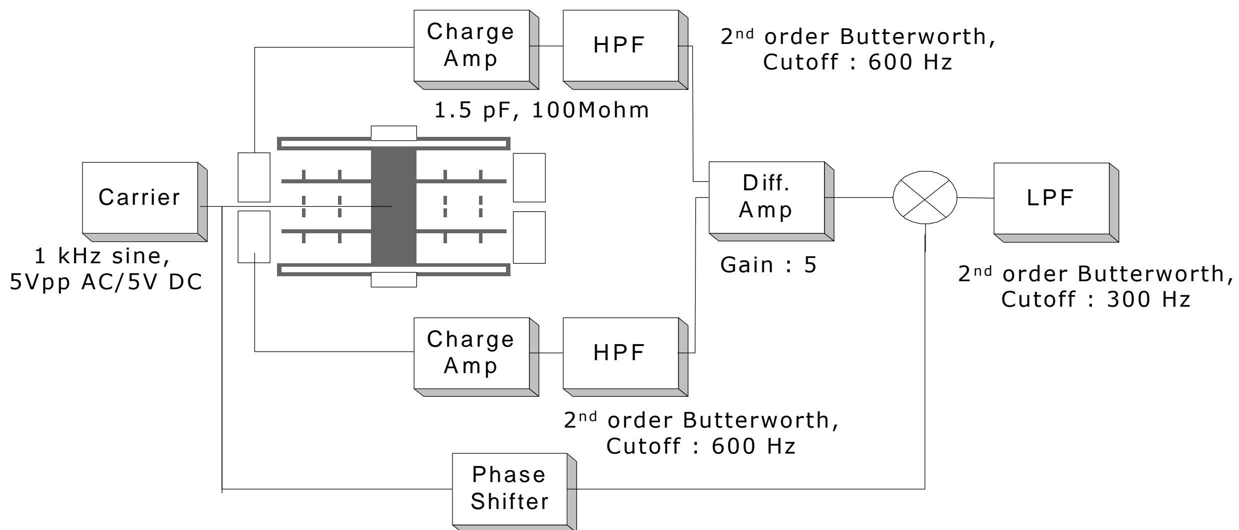


Figure 1 the schematic of the accelerometer and readout circuit

mass to move, and this motion produces the capacitive change. In this paper, the capacitive change comes from the variation of area, not from the variation of gap. This area variational sensing scheme has the advantages of the higher linearity than the conventional gap variational type. The accelerometer has the structure thickness of 40 μm, lateral gap between electrodes of 2 μm, and spring length of 594 μm. Figure 2 shows the modal analysis result using ANSYS. The first mode resonant frequency is designed to be 1 kHz. The design specifications are summarized in table 1.

Figure 2 Modal analysis of the accelerometer

The externally applied acceleration can be measured by detecting this capacitive change. the capacitance changes due to these motions are detected by charge-to-voltage converter. After high-pass filtering the output signal of the charge-to-voltage converter, the signal is demodulated using analog multiplier. After the demodulation, the high frequency components of the signal are removed using low-pass filter, and the acceleration signal is obtained. Figure 3 and figure 4 show the fabrication process flow and fabricated accelerometer, respectively. The fabrication process starts with a SOI wafer with (111) device layer. A tetra-ethyl-ortho-silicate (TEOS) etch mask layer is deposited and patterned. Next, the first deep silicon RIE is performed to the structural depth of 40 ㎛. The sidewall of the structure is passivated by thermal oxide and low stress nitride film. Then the nitride/oxide flims at the bottom are etched away to expose the bare silicon. The silicon is etched again by the deep silicon RIE to the depth of the device layer. This results in the sacrificial gap of 20 ㎛. The wafer is then anisotropically etched in a 20 wt%, 90 ℃ tetramethyl ammonium hydroxides (TMAH) solution for 20 minutes, to release the structure. In this step, the lower parts of the silicon structure without the sidewall passivation are etched in the lateral direction. Also, the roughened lower parts as well as any loose silicon fragments are removed by the alkaline lateral etching. After the release etch step, all sidewall passivation and top oxide films are removed. Then a Ti/Au films are sputtered on the top of the structures for wire-bonding.

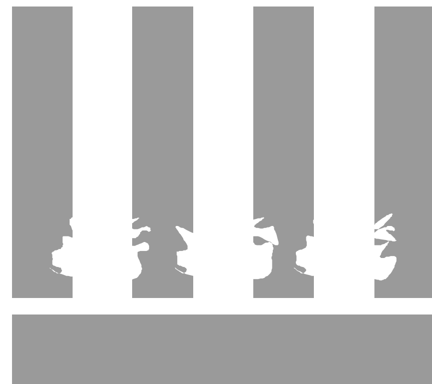
Thickness(um)	40
Gap between Comb(um)	2
Spring width(um)	3.2
Spring length(um)	594
Spring Stiffness(N/m)	4.8
Mass(ug)	40
nominal Cap(pF)	3.3
Resonant Frequency	1 kHz
Mechanical Noise($a_m = \sqrt{\frac{4k_B T \omega_n}{mQ}}$)	15 $\mu g/\sqrt{Hz}$
Electrical Noise($a_e \propto \omega_r^2 \frac{d_0}{V_s} v_e$)	3.8 $\mu g/\sqrt{Hz}$
Operation Pressure(Torr)	atmospheric

Table 1 Design Summary of the accelerometer

(a) Define the structural pattern
using deep silicon RIE

(b) Passivation layer deposition

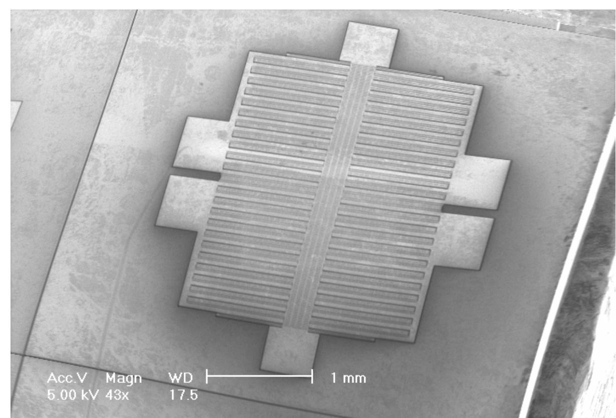
(c) Anisotropic etch using RIE



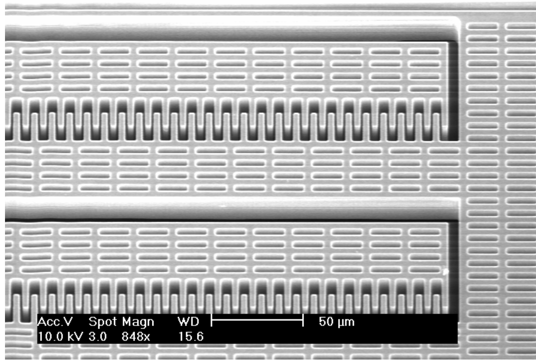
(d) Define the sacrificial layer
using deep silicon RIE
(The roughened lower parts are due to footing)

(e) Lateral wet etch using alkaline solution
- Smoothes roughened bottom surfaces
- Etches silicon fragments

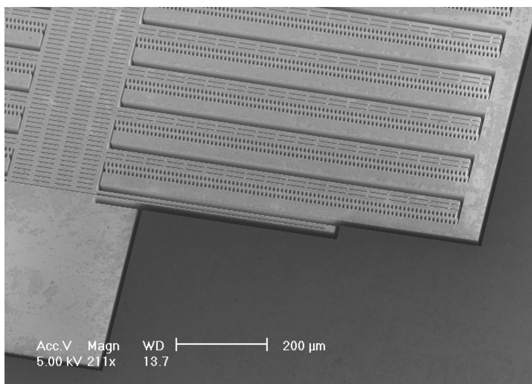
Figure 3 Fabrication Process Flow



(a) Overall view of the accelerometer



(b) Magnified view of the comb electrodes

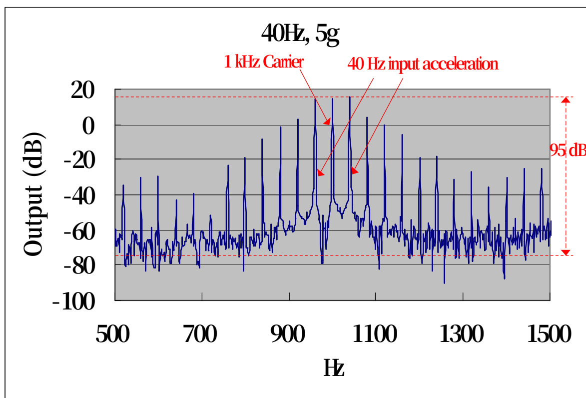


(c) Magnified view of the folded spring

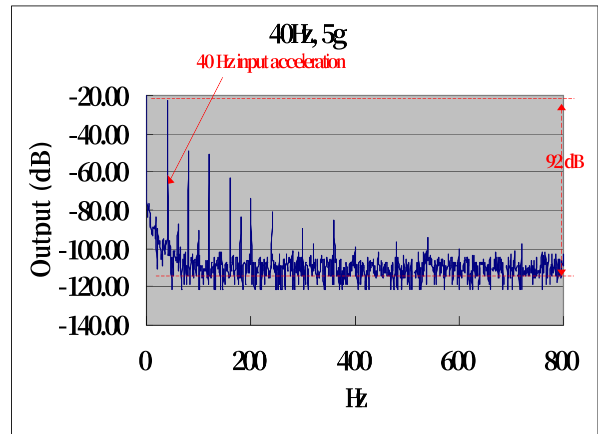
Figure 4 SEM photograph of the accelerometer

3. MEASUREMENT RESULTS

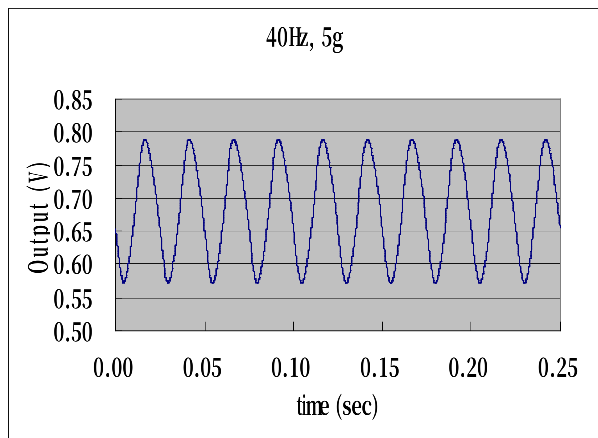
Figure 5 shows the output signals of the fabricated accelerometer. The signal-to-noise ratio (SNR) of the modulated output is 95 dB, and the noise equivalent input acceleration resolution of the modulated output is calculated to be 88.9 µg, as shown in the Figure 3(a). The SNR of the demodulated output is 92 dB, and the noise equivalent input acceleration resolution of the demodulated output is calculated to be 125.59 µg, as shown in the Figure 3(b).



(a) Modulated Output at 40 Hz, 5g input acceleration



(b) Demodulated Output at 40 Hz, 5g input acceleration



(c) Time domain signal at 40 Hz, 5g input acceleration

Figure 5 Output signal of the accelerometer

The input range and linearity is shown in the figure 6. The linearity error is 1.2 %FSO, and the input range is over ? 10 g.

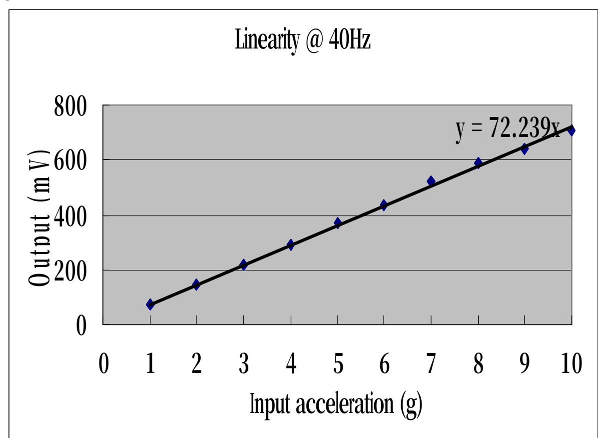


Figure 4 Input range and Linearity at 40 Hz

4. CONCLUSIONS

We fabricated a high-performance x/y-axis accelerometer using the SBM process on a <111> SOI wafer. This fabrication method solved the problem of the footing phenomenon in the

conventional SOI process, and we achieved both the high manufacturability and high performance.
The fabricated accelerometer has a demodulated signal-to-noise ratio of 92 dB, when 40Hz, 5 g input acceleration is applied. The noise equivalent input acceleration resolution and bandwidth are 125.59 μg and over 100 Hz, respectively. The acceleration random walk is 12.5 μg/$\sqrt{Hz}$. The output linearity is measured to be 1.2 % FSO(Full Scale Output) at 40 Hz, and the input range is over ± 10g.

5. ACKNOWLEDGEMENT

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