

Development of the VCXO with the PECL

¹Seung Jin Hong, ¹Jae Kyung Lee, ¹Dal Hwan Yoon, ²Seung Gi Min

¹Dept. of Electronic Engineering, Semyung University

²Human Meditek Co., Ltd.

¹San21-1, Shinwol-dong, Chechon, Korea

Tel. +82-43-649-1790, Fax. +82-43-644-6165

¹E-mail : yoondh@semyung.ac.kr

Abstracts: In this paper, we have developed the voltage controlled crystal oscillator (VCXO) with positive emitter coupled logic(PECL). The VCXO is a crystal oscillator which includes a varactor diode and associated circuitry allowing the frequency to be changed by application of a voltage across that diode. The characteristics of the PECL has the delay time less than 2 ns and the faster logic gate, and the high level output greater than 2.3 V and the low level output smaller than 1.68 V.

Keyword: voltage control, crystal oscillator, faster logic gate, diode.

I. Introduction

Today's mobile communications demand higher communication quality, higher data rates, higher frequency operation and more channels per unit bandwidth. Most of this equipment is portable, low power consumption and small size are also required[1]. All of these constraints combine to make the whole design including component selection and evaluation quite challenging.

Voltage controlled crystal oscillators are commonly found in wireless systems, and other fields of application are Sonnet, Ethernet, optic fiber, digital TV, digital DVD, LAN and GPS that must tune across a band of frequencies[2, 3].

II. Theory of oscillator

A VCXO is a crystal oscillator which includes a varactor diode and associated circuitry allowing the frequency to be changed by application of a voltage

across that diode. This can be accomplished in a simple clock or sinewave crystal oscillator, a TCXO (resulting in a TC/VCXO-temperature compensated voltage controlled crystal oscillator), or an oven controlled type (resulting in an OC/VCXO-oven controlled voltage crystal oscillator)[3].

Recently, the research and development of the VCO (voltage- controlled oscillator) have been diversely processed. The customer have demand the higher communication quality, higher data rates, higher frequency operation and more channels per unit bandwidth.

In order to increase the speed of an oscillator, there are logic gates such as ECL(emitter coupled logic), PECL(positive emitter coupled logic) and LVPECL(low voltage PECL).

There are several characteristics peculiar to VCXOs. In generating a VCXO specification these apply in addition to the characteristics which define fixed frequency crystal oscillators. Primary among the specifications which are peculiar to VCXOs are the following[4].

The voltage which is applied to the VCXO input terminal causing a change in frequency is varying control voltage that is sometimes referred to as modulation voltage, especially if the input is an AC signal.

The deviation is the amount of frequency change which results from changes in control voltage. The transfer function denotes the direction of frequency change to the control voltage. A positive transfer function denotes an increase in frequency for an increasing positive control voltage. Conversely, if the frequency decreases with a more positive (or less negative) control voltage, the transfer function is negative.

Linearity is the ratio between frequency error and total deviation, expressed in percent, where frequency error is the maximum frequency excursion from the best straight line drawn through a plot of output frequency to the control voltage

Modulation rate (sometimes referred to as deviation rate or frequency response) is the rate at which the control voltage can change resulting in a corresponding frequency change. It is measured by applying a sine wave signal with a peak value equal to the specified control voltage, demodulating the VCXO's output signal, and comparing the output level of the demodulated signal at different modulation rates.

Slope/Slope Linearity/Incremental Sensitivity can be a confusing area as these terms are often misapplied. Slope should be really called average slope if it is intended to define the total deviation divided by the total control voltage swing.

2.1 Phase noise

Signal sources such as crystal oscillators produce a small fraction of undesirable energy (phase noise) near

the output frequency. As performance of such systems as communications and radar advance, the spectral purity of the crystal oscillators which they employ is increasingly critical.

Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1 Hz bandwidth at a given offset from the desired signal.

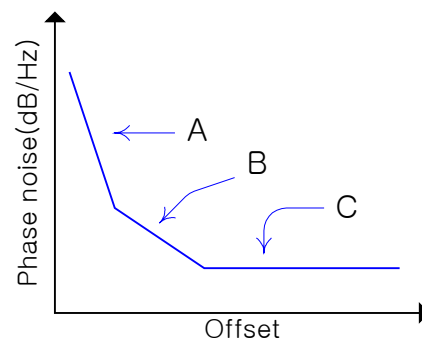


Fig. 1 Three of phase noise

A plot of responses at various offsets from the desired signal is usually comprised of three distinct slopes corresponding to three primary noise generating mechanisms in the oscillator, as shown in Figure 1. Noise relatively close to the carrier (Region A) is called Flicker FM noise; its magnitude is determined primarily by the quality of the crystal. The best close-in noise results have been obtained using 5th overtone AT cut crystals or 3rd overtone SC cut crystals in the the 4-6 MHz range. While not quite as good on average, excellent close-in noise performance may also be achieved using 3rd overtone crystals in the 10 MHz area, especially double rotated types. Higher frequency crystals result in higher close-in noise because of their lower Q and wider bandwidths.

Noise in Region B of Figure 1, called "1/F" noise, is caused by semiconductor activity.

Region C of Figure 1 is called white noise or broadband noise. When frequency multiplication is employed to achieve the required output frequency from a lower frequency crystal, the phase noise of the output signal increases by 20 log (multiplication factor).

2.2 Jitter in clock source

Continuous advances in high-speed communication and measurement systems require higher levels of performance from system clocks and references. Performance acceptable in the past may not be sufficient to support high-speed synchronous equipment. Perhaps the most important and least understood measure of clock performance is jitter. So, the jitter definition of ITU is the short-term variations of the significant instants of a digital signal from their ideal positions in time.

The expected edges in a digital data stream never occur exactly where desired. Defining and measuring the timing accuracy of those edges (jitter) is critical to the performance of synchronous communication systems.

For applications requiring a PECL or ECL VCXO having an RMS jitter of <0.1 ps within the bandwidth of 12 KHz to 20 MHz, the phase noise is measured on the HP3048A phase noise measurement system.

Joe Adler was proposed that the RMS jitter can be treated as small index phase modulation and can be converted from radians to degrees[5]

$$J_{rms} = \left(\frac{360}{2\pi} \right) 10^{\frac{X}{20}} \quad (1)$$

In equation (1), X is the equivalent sideband level of the integrated phase noise and has a dBc value for the integration of the phase noise over 12 KHz to 20 MHz.

III. VCXO design with the PECL

The design process of the VCXO is in Figure 2.

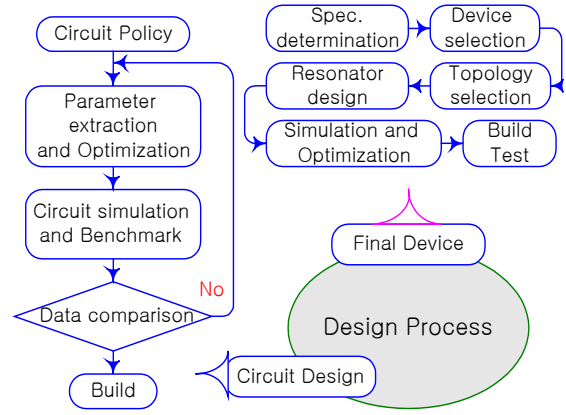


Fig. 2 Design process

The crystal has various formats in cutting angle. Such a crystal oscillator be composed of the blank, electrodes and the base. An electrodes use mainly the Ag, and other use Au, Al, Cr and Ni or mix of their. Also a crystal oscillator has the directional property in the solid state and call it anisotropic. Figure 3 shows the crystal cutting angle.

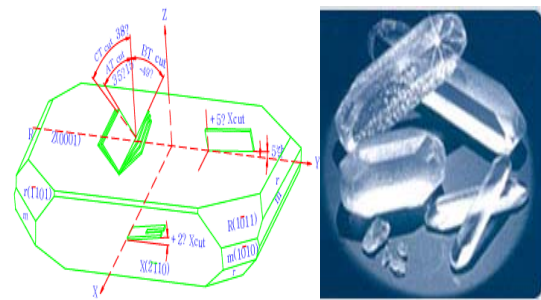


Fig. 3 Crystal structure

Actually, we design the crystal in terms of the specification. In order to obtain higher frequencies in the crystal, the thickness must be thin and use the MESA blank method. The MESA blank method supply

the frequency in the middle of the crystal after making the crystal, and attach to the electrodes and base. We call it high frequency fundamental(HFF) device. Figure 4 shows the crystal made by the MESA blank method.

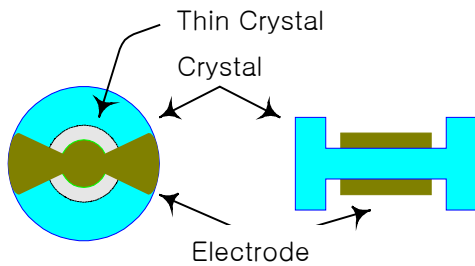
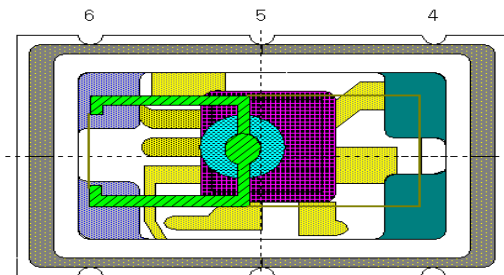


Fig. 4 Upper and side formats of the MESA blank

Other important parameters of determining the performance of the crystal oscillator are the quality and geometric formats of the crystal, cutting angle and allowable tolerance, solid state of an electrode, thickness and size of an electrode, materials, so on.

Figure 5 present an inner structure of the mount package with the MESA blank and their pin arrays. In Figure 5, the IC package is closed to the box with a nitrogen and protected from a outer shock, temperature and other environments and then we can obtain the stabilized output signal.



Pin 1 : Voltage control, Pin 2 : Enable
Pin 3 : GND, Pin 4 : Output
Pin 5 : Complementary out, Pin 6 : V_{CC}

Fig. 5 IC package structure

Figure 6 shows real package connected by the blank and electrodes. A thin film attached to the surface of the blank is connected to the vibrating device and an electrode for supplying the voltage.

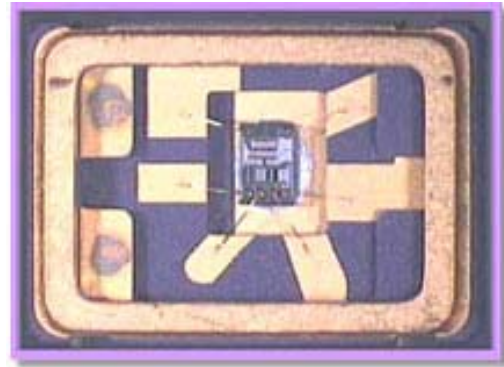


Fig. 6 Real ceramic IC package

Figure 8 shows the VCXO of the 5x7 mm size.

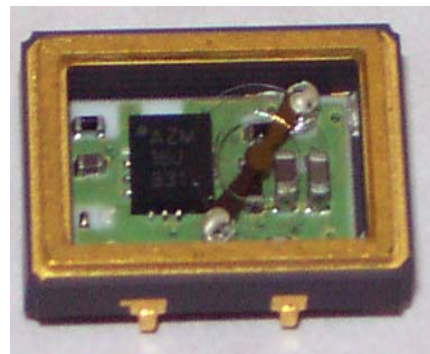


Fig. 7 The manufactured VCXO

IV. Experimental results

In order to test the VCXO performance, we must refer the specification of the VCXO.

Table 1 shows the measured data specification from fundamental frequency 65.2 MHz.

Table 1. The measured data

Freq.	65.2 MHz	Supply voltage	3.3 V
Blank angle	2 °59'±30"	Voltage control	1.65±1.35V

Part No.	Limit	Test
Supply current	75 mA	8 mA
Tolerance	ppm	15.3
Temper stability	0-70/± 20 ppm	
Duty cycle	50 ± 10 %	50.19
Rise time	6 ns Max	5.413
Fall time	6 ns Max	3.588
Pk to Pk	V	3.86
Output voltage	Vh Vmin	
	Vl Vmax	
Pullability	Low : -50 ppm	- 75
	High : + 50 ppm	80
Enable/disable	Pin 1 or 2	Ok

Figure 8 show the jitter signal to the 155.52 MHz VCXO

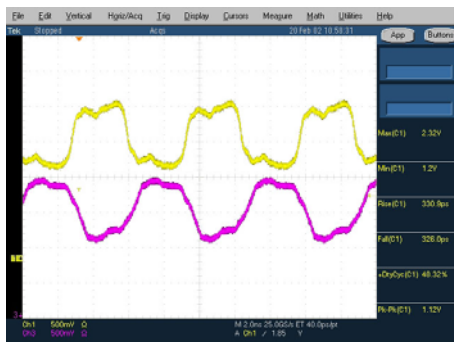


Fig. 8 Jitter signal

In Figure 8, the maximum and minimum of an output voltage are 2.32 V and 1.2 V, respectively. The rise and fall time are 330.9 ps and 326.0 ps, respectively. Then

duty cycle is 48.32 % and Pk to Pk voltage is 1.2 V.

Figure 9 shows the phase noise, loop bandwidth is 96.2 Hz, tune slope is 50 Hz/V and reference superious is 10.0 dB.

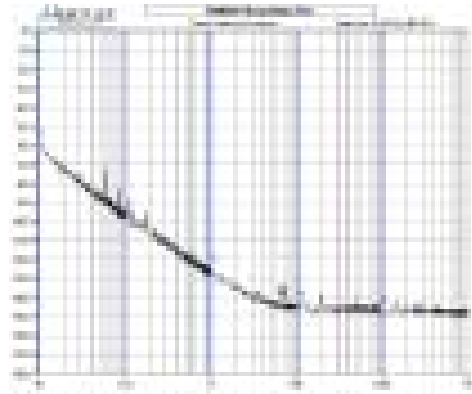


Fig. 9 Phase noise

V. Conclusion

It is especially important with VCXOs that the user not over-specify the product. The particular problem with VCXOs is that increased deviation results in degraded stability which can result in the need for still wider deviation, further degrading stability, resulting in a spiraling increase in the required deviation.

The performance of frequency sources both jitter frequency and amplitude should be considered correctly. It will also determine a cost-effective approach for each application.

In this paper, we have developed the VCXO with the PECL and MESA blank method, and discussed the definition of jitter and phase noise.

In order to use an oscillator of the precise performance, jitter and phase noise are an important parameter. The discussion is by no means complete, but should obtain enough information to apply to an industry field.

References

- [1] Chris O'Connor, "Tracking Advances in VCO Technology," *Microwaves&RF* July, 2002
- [2] www.vectron.com
- [3] U. L. Rohde & G. Klage, "Recent Advances in Linear VCO Calculations, VCO Design and Spurious Analysis of Fraction-N Synthesizers," *Microwave & RF Magazine*, pp. 57-78, Aug. 2000
- [4] Application Notes, "VCXOs voltage controlled oscillators," Vectron International A Technologies Co.
- [5] Vectron International A Technologies Co., "RMS Jitter Calculation in 12 kHz to 20 MHz Bandwidth for VI's CO600 V Series VCXO," Aug. 11, 1999