FGI(Frame Grabber Interface) Design for MSC(Multi-Spectral Camera) Image Data Test

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Abstract: The FGI is an integral component of the MSC test equipment and is situated in a slot along the ISA bus of the test equipment PC. The main function of the FGI is an interface between the MSC image data via hotlink interface and Frame Grabber. The FGI has two independent receiving channels that allow the board to receive image data arriving. The FGI also includes two transmission channels with hotlink transmitters. Additionally, the FGI is capable of generating digital video test patterns to test the NUC.

Keywords: Frame Grabber Interface, MSC Image Data

1. Introduction

The MSC(Multi-Spectral Camera) shall be integrated into the KOMPSAT 2, which is a LEO spacecraft and will be used to generate observation imagery data. The FGI(Frame Grabber Interface) board is an integral component of the test equipment to test MSC image data, which are exactly the EOS(Electro-Optical System) output and the NUC(Non-Uniformity Correction Unit) output, and is situated in a slot along the ISA bus of the test equipment PC.

The FGI has two independent receiving channels that allow the board to receive image data arriving via hotlinks receivers. Each of these channels receives data from a different source. As well, the FGI includes two transmission channels that terminate in hotlink transmitters. During transmission the FGI can send data through each transmission channel separately. Additionally, the FGI board is capable of generating digital video test patterns that are used for the NUC test and the self test by transmitting predetermined video patterns to them, re-receiving and forwarding them to the FG(Frame Grabber) board.

2. Operational Modes

The FGI has the 3 operational modes: the EOS test, the NUC test and the self test mode.

1) EOS Test Mode

In this mode the FGI receives image data from the hotlink receiving channels. The received data is then decoded, reformatted and transmitted to the FG. The two receiving channels receive data from two different sources simultaneously, and the two transmission channels transmit their data simultaneously as well. Fig. 1 shows the block diagram of the EOS image test using the FGI and the FG.

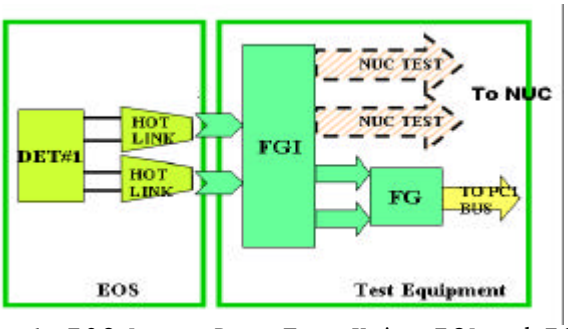

Fig. 1. EOS Image Data Test Using FGI and FG

2) NUC Test Mode

This mode is for testing the NUC's communication channels and data processing capabilities. During the test, the internal pattern generator is used for transmitting a predetermined video pattern to the transmission channels. The NUC retransmits the data back to the FGI after processing the predefined video patterns. The FGI receives the processed data via its receiving channels and then forwards this data to the FG. Since the video pattern is known in advance, this mode of operation makes it possible to test all of the communication channels incorporated in the FGI as well as its data processing capabilities. Fig. 2 describes the NUC image data test diagram using the FGI and the FG.

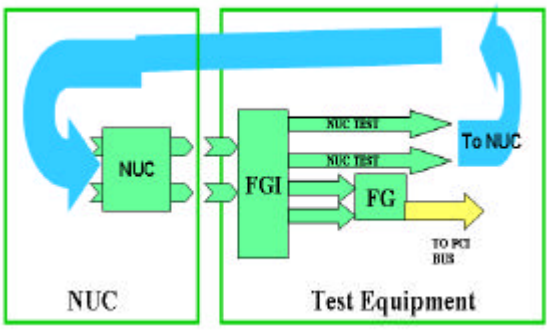

Fig. 2. NUC Test Using FGI and FG

3) Self Test Mode

In this operation mode, the FGI is tested as a stand-

alone unit. This mode is similar to the NUC test mode in the use video patterns created by the integrated pattern generator. The difference is that the transmission channels are connected to the receiving channels directly implementing a loop-around mode of operation.

3. Hardware Design

The FGI board functions as an interface between digital video sources that arrive via hotlinks and additional video processing units. The FGI has two independent receiving channels, two transmission channels and internal patter generator as mentioned before. The FGI is connected to the FG board via a 100-pin SCSI connector and can transmit processed video data to the FG for further handling and storage. Fig. 3 displays a block diagram of the FGI board.

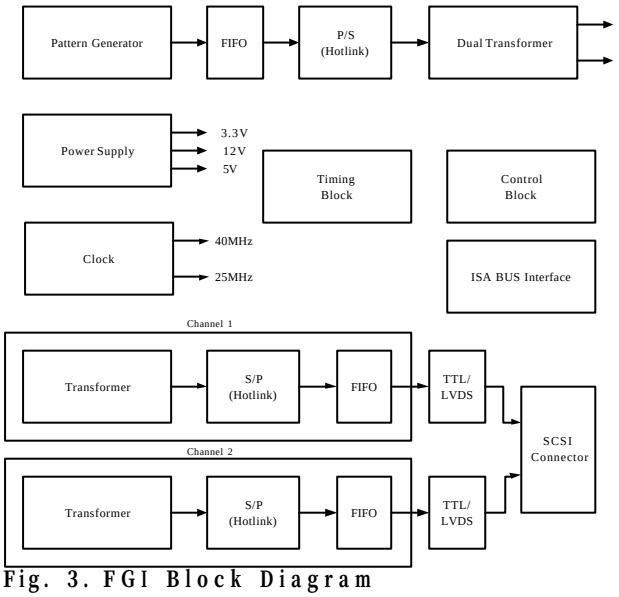

Fig. 3. FGI Block Diagram

The FGI is divided into the following functional blocks: the Powering block, the LVDS transmitter block, the hotlink receiver and the transmitter block, and the FPGA block.

1) Powering Block

The FGI makes use of a single powering source, which is the test equipment PC. The FGI receives 5V and 12V via the PC's ISA bus and refers to this operating voltage as VCC. In addition, voltage regulator uses this 5V voltage to create the 3.3V operating voltage, which is used by the FPGA block.

2) LVDS Transmitter Block

The block receives the TTL image data signals, which have been processed in the FPGA, transforms these signals to LVDS signals and forwards them to the FG. The main advantage in using LVDS signals is that they have a higher reliability and accuracy. The control signals such as the PIXEL_CK, the FRAME_VALID, the LINE_VALID, the DATA_VALID and the 1PPS are transformed by the drivers and transmitted to the FG as well as image data signals.

3) Hotlink Receiver and Transmitter block

The FGI contains two hotlink-receiving channels. Each channel contains a separate hotlink receiver. Therefore, the FGI receives data from two different sources simultaneously. In addition, a dual line isolation transformer serves both of the receiving channels. The function of the hotlink receivers is to convert the PECL serial inputs to TTL parallel 8-bit data.

The FGI also contains two hotlink transmission channels. But, the channels are comprised of a single hotlink transmitter that transmits identical data from its outputs to both channels. In the transmission channels, a dual line isolation transformer serves both of the transmission channels. The function of the hotlink transmitter is to convert the TTL parallel 8-bit data input to PECL serial outputs. It contains an embedded PLL that multiplies the reference clock by 10 for driving its serial shifter. Since the input clock has a frequency of 25MHz, the PECL output signals have a frequency of 250MHz. The reference clock has two functions. It functions the reference clock for the transmitter and also synchronizes the parallel data input for writing.

4) FPGA Block

The FPGA block is the heart of the FGI, as it controls the entire logic of the board and manages the reception, processing and transmission of the video data. The FPGA block is designed to receive two hotlink data streams in serial format. It decodes and converts these data streams to parallel data streams that are transmitted to the FG. While transmitting to the FG, the FPGA also transmits the vital clock and control signals that are received with the original data. In addition, the FPGA block is capable of simulating hotlink transmission using an internal pattern generator.

The FPGA block is divided into several sub-blocks such as the ISA_IO16, the HL_DECODER_A, the HL_DECODER_B, the TRANSMITTER, the VALID_OR, the CLOCKS, and the INT_CONT, and so on.

The ISA_IO16 sub-block manages the communication between the FPGA internal logic and external test equipment units via the PC's ISA bus.

The HL_DECODER_A and HL_DECODER_B sub-blocks receive and process the data received from the hotlink of reception channel #1 and channel #2 respectively. Fig. 4 shows the pixel line format arriving from hotlink transmitter of the EOS. After the header, a 'Start of Image' character signifies the beginning of the video data. And then video data follows and terminates with an 'End of Image' character. Fillers are also placed along

the data stream. After the header is extracted, it is sent to a ‘parallel data storage’ unit where it is stored in 10 bit width and transmitted to the FG.

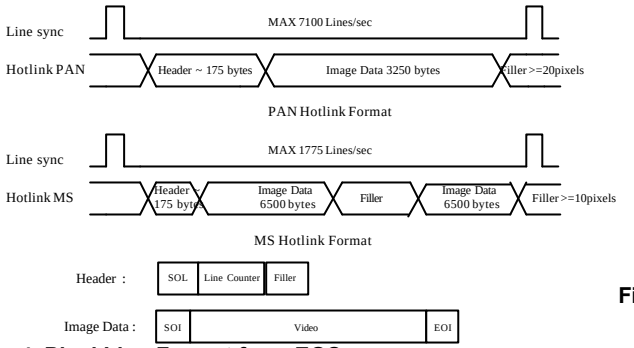

Fig. 4. Pixel Line Format from EOS

Fig. 5 shows the hotlink pixel line format from the NUC. The two main differences between the EOS format and the NUC format are that the number of header is increased and header data include channel ID and the ancillary data as well as the line counter. In addition, a ‘Start of Fame’ is inserted once every 8 lines instead of ‘Start of Line’.

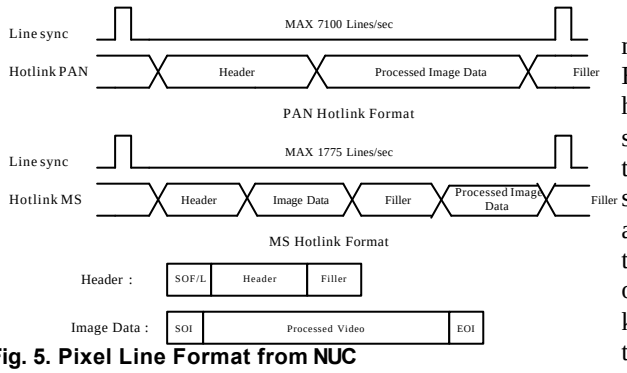

Fig. 5. Pixel Line Format from NUC

The TRANSMITTER sub-block is in charge of generating and transmitting simulated serial data towards the hotlink. This data is used during the NUC test mode and self test. In general, this sub-block generates two identical streams containing predetermined image data patterns for transmission outwards. When generating patterns, each line is divided into groups of 13 pixels, which are referred to as step. Since there are 2600 pixels per line in the PAN channel. It is possible to increase or decrease the pixel values once every step. The actual shape of the pattern that is generated depends on the PATT_SEL command through the ISA BUS. Available patterns are given in the Fig. 6. This sub-block also transmits the PIX signal outward of the FPGA. This signal contains the recent increments or decrements occurring in the generated data pattern and is generated used during debugging stages.

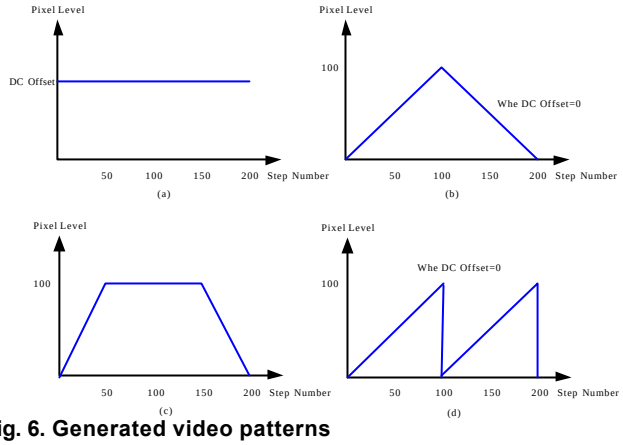

Fig. 6. Generated video patterns

The VALID_OR sub-block receives the data streams from the two reception channels. It also receives the channels’ data validity signals and the main pixel clock.

The CLOCKS sub-block generates internally used clocks from a main clock and the INT_CONT sub-block creates control signals and synchronizes signals with the main clock.

4. Conclusions

This paper shows the design concept and operational modes of the FGI board, which is to test not only the EOS image data but also the NUC image data. In the hardware point of view, the FGI board is situated in a slot along the ISA bus of the test equipment PC and contains two independent receiving channels, two transmission channels. Additionally, the FGI is capable of generating and transmitting digital video test patterns using the FPGA technology in order to test the NUC. In the operation point, the FGI board is designed to have 3 kinds of mode, which are the EOS test mode, the NUC test mode and he self test mode, according to the test target. As the next step of this paper, the implementation result and the application examples can follow.

References

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