Video data output system design for CEU (camera electronic unit) of satellite

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Abstract: In MSC(Multi-spectral camera), the incoming light is converted to electronic analog signals by the CCD(charge coupled device) detectors. The analog signals are amplified, biased and converted into digital signals (pixel data stream) in the FPE(Focal plane electronics). The digital data is transmitted to the PMU for pre-processing to correct for non-uniformity, to partially reorder the pixel stream and to add header data for identification and synchronization
In this paper, the video data streams is described in terms of hardware

1. Introduction

A total of 5280 pixel video signals are read from each detector, 5200 active pixels and 80 isolation, dark and prescan pixels. All pixel video of each detector are output through one output. Every output from CCD port has a separate video-processing channel that incorporates CDS(correlated double sample), PGA(programmable gain amplifier) and a 10 bits A/D(analog to digital converter). The outputs of the A/Ds are digitally multiplexed and driven out using differential line drivers. Every two consecutive detector outputs are then MUXd, converted to 8 bit bytes, serialized and transmitted to the NUC module within the PMU(Payload Management Unit).

2. MSC system

The MSC consists of the EOS(Electro-Optical Subsystem), the PMU and the PDTS(Payload Data Transmission Subsystem). The EOS is to obtain data for high-resolution images by converting incoming light into digital stream of pixel data. The PMU performs electrical and software interfaces between the MSC and the spacecraft, and controls all the MSC subsystem by the ground station commands and reports all the SOH(State Of Health) telemetry to the spacecraft. The PDTS stores and transmits these digital image data to the ground station through X band antenna. The EOS consists of the PAN camera, the MS camera and the CC. The PMU comprises of the SBC(Single Board Computer), the THTM(Thermal & Telemetry Module), the NUC(Non-Uniformity Correction Board), the APDE(Antenna Pointing & Deriving Electronics Board) and the PSM(Power Supply Module). The PDTS consists of the DCSU(Data Compression & Storage Unit), the CCU(Channel Coding Unit), the QTX(QPSK Transmitter), the ASU(Antenna Switching Unit) and the APS(Antenna Pointing System). The fig.1 shows the MSC block diagram.

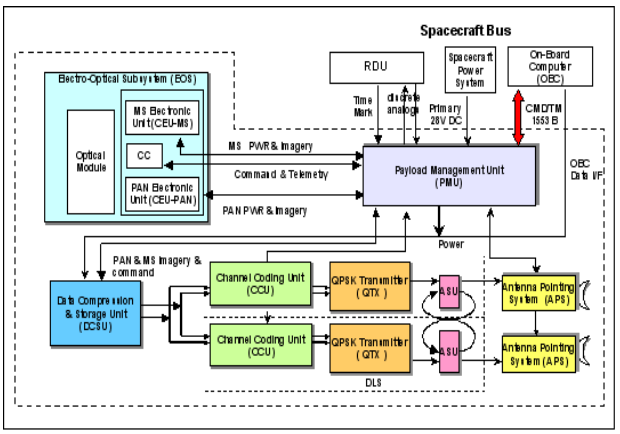

Fig.1 MSC electronic system.

As depicted in the fig.1, the SBC controls all the MSC units by means of receiving commands and data from the spacecraft via mil-std-1553B communication channel and distributing them to the proper unit at appropriate time via serial communication channel such as RS-422. The NUC is in charge of non-uniformity correction of image data. The DCSU deals with image data compression and storage. The APDE controls x-band antenna to make communication link with the ground station. The CCU is in charge of encryption, CCSDS(Consultative Committee for Space Data Systems) data encoding and randomization of incoming data stream from the DCSU. The THTM gathers the analog telemetry from all the units and sends them to the SBC and maintains the temperature of the EOS structure, optics and detectors within specified ranges.

3. Video data processing in FPE

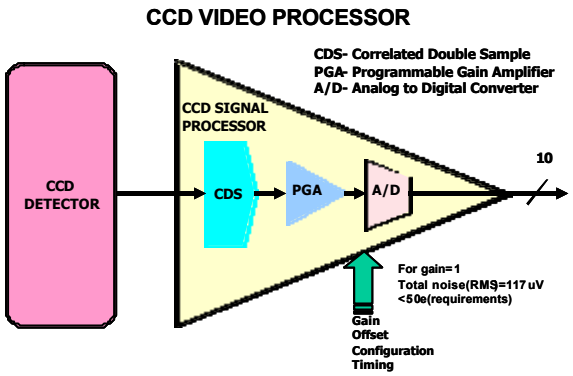

Fig.2 CCD video processor block diagram.

Every output from CCD port has a separate video-processing channel that incorporates CDS, PGA and a 10 bits A/D. In this paper, the TDA8787 is used by video processor. The TDA8787 has the sampling frequency up to 25MHz, PGA gain range of 3dB, and low power consumption. The outputs of the A/Ds are digitally multiplexed and driven out using differential line drivers. Each of the detectors is supported separately with the required timing and power supply circuitry

The TDA8787 is needed the signals those are SHP(preset sample-and-hold pulse) and SHD(data samples-and-hold pulse input). The fig.3 is the pixel frequency timing diagram for TDA8787.

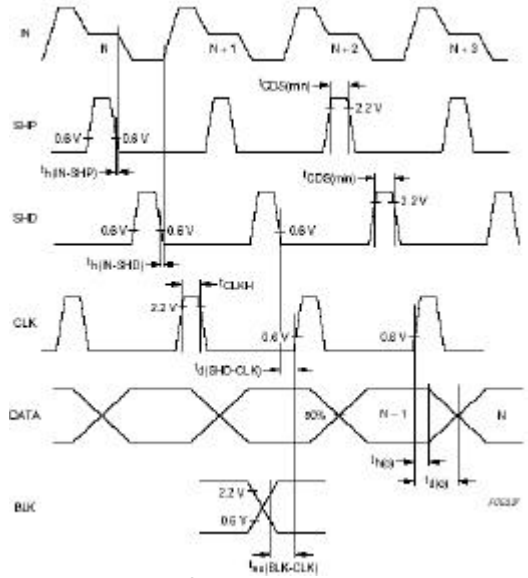

Fig.3 Pixel frequency timing diagram.

The fig.4 and the fig.5 are the real signals those are captured by scope in this paper.

The single band pixel rate is about 40Mpps. Since this pixel rate is high for a single video-processing channel (a feasible video-processing rate is limited to about 12Mpps), then each detector's band shall be configured to up to four output ports (each output pixel rate is about 10Mpps)

A total of 5280 pixel video signals(5200 active pixels and 80 isolation) are read from each detector, are outputted 2640 Even pixel first, and 2640 Odd pixels, according to the CCD detector specification. The fig. 6is the format which is the output from the detector in MSC.

Fig.4 FPE PAN SHD signal

Fig.5 FPE PAN SHP signal

Odd pixels to upper shift register transfer and even pixels to lower shift register transfer
Prescan 1, Prescan 2, ..., Prescan 10 Dark reference 2, ..., Dark reference 20 Isolation 2, ..., Isolation 10 Pixel 2, Pixel 4, ..., Pixel 2598, Pixel 2600, ..., Pixel 2602, ..., Pixel 5198, Pixel 5200 Isolation 10, ..., Isolation 2 Dark reference 20, ..., Dark reference 2
Odd pixels transfer from upper shift register to lower shift register
Prescan 1, Prescan 2, ..., Prescan 10 Dark reference 1, ..., Dark reference 19 Isolation 1, ..., Isolation 9 Pixel 1, Pixel 3, ..., Pixel 2597, Pixel 2599, ..., Pixel 2601, ..., Pixel 5197, Pixel 5199 Isolation 9, ..., Isolation 1 Dark reference 19, ..., Dark reference 1

Fig.6 CCD detector output mode

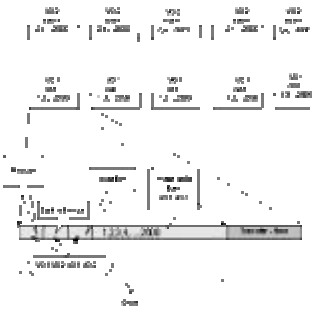

Fig.7 PAN parallel 10 bit MUXd (1)

Fig.8 Pan parallel 10-bit MUXd (2)

The pixel video signals are read with a CDS, amplified and digitized by a 10 bit A/D converter. Every two consecutive detector outputs are then MUXd(Fig.7, Fig.8), converted to 8 bit bytes, serialized by the HOT-LINK data transmitter. The figure below shows the method of the 10 to 8 bit translations. The fig.9 is the converting 10 bit to 8bit and the fig.10 is the simulation result in FPGA code.

The data is transmitted through two differential channels (two pairs of wires) for cross strap requirement. The FPE-MS consist of 2 detectors (video output through 4 pairs of wires) and the FPE-PAN consist of 3 detectors (video output through 24 pairs of wires, 12 pairs for the primary bands and 12 pairs for the redundant bands).

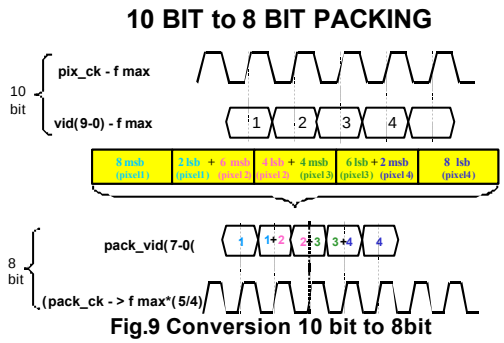

Fig.9 Conversion 10 bit to 8bit

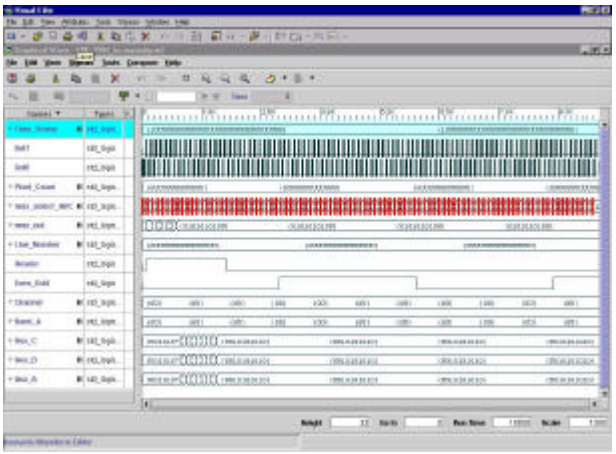

Fig.10 FPGA simulation result(MUXd output)

All the Hot-Link transmission lines are terminated with termination resistors and transformers on both sides to match the characteristic impedance of the line.

Each video data output contains multiplexed data from 2 outputs of a detector's band. The video data rate at the input of the Hotlink serializer is 25 MHz according to the requirements of the DCSU, which receives the data through the PMU. The outputs of the Hotlink serializer are of differential type. The serial data contains all the information and synchronization signals for video restoration.(Fig.11)

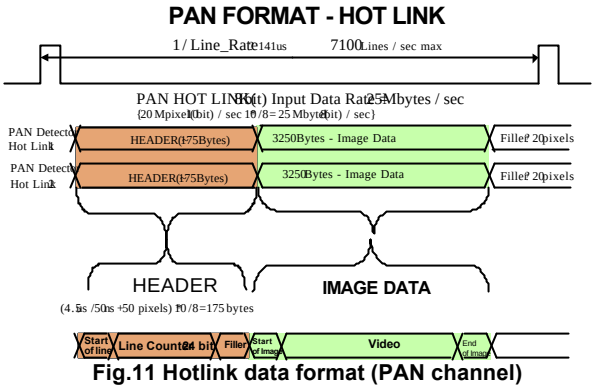

Fig.11 Hotlink data format (PAN channel)

5. Conclusions

The FPE board supplies operating voltages as well as clocks to the CCD detector. The pixel video signals are from CCD detector in MSC need the fast video signal processing and transmitting to PMU. So in this paper, described the method of acquisition video data, video signal processing, and transmitting. In satellite system, the development of the FPE will be based on advanced design methods and tools, and will use the advanced component authorized for space. It's also very important to reduce size, power consumption and weight and enhance performances.

References

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