Design of Main Computer Board for MSC on KOMPSAT-2

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Abstract: SBC(Single Board Computer) is being developed for MSC(Multi-Spectral Camera) on KOMPSAT-2(Korea Multi-Purpose Satellite). SBC controls all the units of MSC system and gets commands and sends telemetry to and from spacecraft bus via 1553 communication channel. Due to the fact that SBC does very important roles for MSC system operation and SBC operates with 100% duty cycle, SBC is designed to have high reliability. SBC which has Intel 80486 as a main processor includes eight serial communication channels, one mil-std-1553 interface channel and several discrete interfaces. SBC incorporates 2Mbyte radiation hardened SRAM(Static Random Access Memory) and 1Mbyte flash memory. There are also PIC(Programmable Interrupt Controller), counter, WDT(Watch Dog Timer) in the SBC. In this paper, the design result of the SBC is presented.
Keywords: MSC, SBC, MIL-STD-1553B, 80486

1. Introduction to the MSC system

MSC is a high resolution multi-spectral remote-sensing instrument. MSC will be installed on KOMPSAT-2 that will be launched in 2004. MSC will perform its mission with the GSD(Ground Sample Distance) of 1m, swath width of 15km and spectral range of 450nm ~ 900nm at the altitude of 685km.

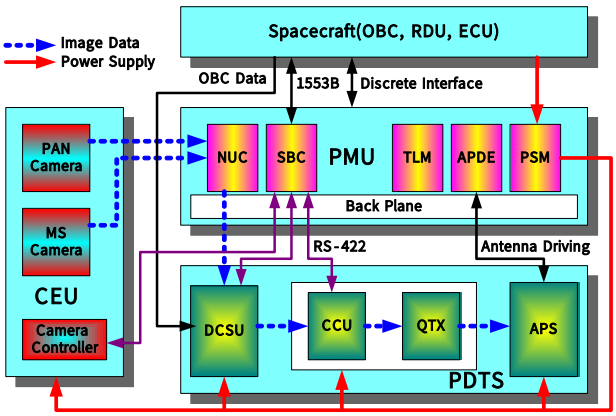

Fig. 1. MSC Electronics Block Diagram

MSC consists of three main subsystems as depicted in fig.1. One is EOS(Electro-Optics Subsystem), another is PMU(Payload Management Unit) and the other is PDTS(Payload Data Transmission Subsystem). EOS receives incident energy and converts them into digital electronic signal and PDTS stores these digital image data and transmits them to the ground station through X-band communication link. PMU performs the electrical and software interface between MSC and spacecraft, and controls all the MSC subsystem according to the ground station commands and reports all the state-of-health telemetry to the spacecraft. EOS consists of PAN (panchromatic) camera, MS(Multi-Spectral) camera and CC (Camera Controller). PMU consists of SBC(Single Board Computer), THTM(Thermal & Telemetry Module), NUC(Non-Uniformity Correction Board), APDE (Antenna Pointing & Deriving Electronics Board) and PSM(Power Supply Module). PDTS consists of DCSU (Data Compression & Storage Unit), CCU(Channel Coding Unit), QTX(QPSK Transmitter), ASU(Antenna Switching Unit) and APS(Antenna Pointing System). NUC is in charge of non-uniformity correction of image data. DCSU deals with image data compression and storage. APDE controls x-band antenna to look at the receiving antenna in the ground station. CC controls EOS to take pictures of ground target. CCU is in charge of encryption, CCSDS(Consultative Committee for Space Data Systems) encoding and randomization of incoming data stream from DCSU. THTM gathers the analog telemetry from all the units and sends them to SBC. THTM also controls the temperature of EOS structure, optic elements and detectors.

2. SBC Requirements

SBC is in charge of the interface between spacecraft and MSC as shown fig.2. SBC controls all the MSC units by receiving commands and data from spacecraft and distributing them to the proper units at appropriate time. SBC gathers all the state-of-health telemetry from all the units and sends them to the spacecraft. SBC has six serial communication channels with other MSC sub-units to transmit control information and receive status information.

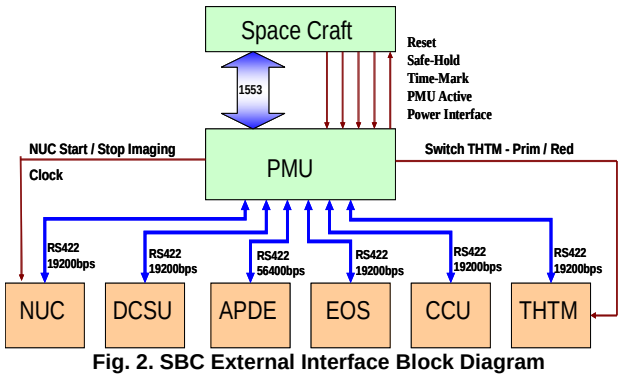

Fig. 2. SBC External Interface Block Diagram

Because SBC controls the whole MSC system with the duty cycle of 100%, it should be designed to have very high reliability. Therefore, SBC needs to have full redundancy and should be designed to support the philoso-

phy that 'a single point failure' shall not cause the mission failure. In addition to that, radiation effect and thermal effect should be considered for the SBC design.

3. SBC Design

SBC consists of several functional modules as shown in fig 3.

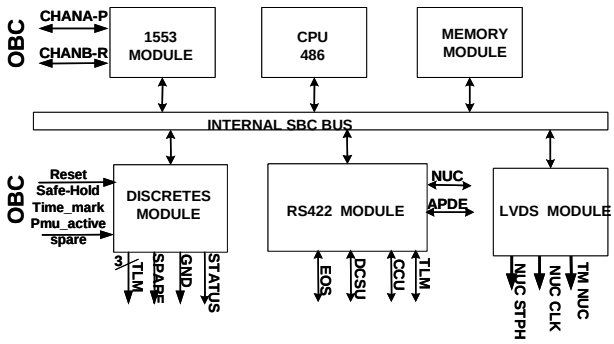

Fig. 3. SBC Block Diagram

1) CPU module

Intel 80486 DX2 processor is used as a main controller of the MSC system. 25MHz clock is applied to the CPU. Because there is clock multiplier module inside 80486 DX2 processor, CPU internal operation is performed at the speed of 50MHz. However, CPU external bus operation is synchronized with 25MHz clock. Even though the CPU provides both paging and segmentation capability, paging mechanism is not used because SBC don't need large amount of memory. Even though the CPU has 8KBytes internal cache and support 'write-through cache update policy', these capabilities are not used for SBC in order to minimize the effect of SEU(Single Event Upset) in the space. There is floating point units inside CPU to provide fast calculation of floating point numbers. There is no DMA(Direct Memory Access) device in the SBC. The CPU has some pins to handle the parity bit of data bus which can be used to detect data bus errors. The CPU has four 32bits write buffer to minimize the effect of memory latency.

2) Memory module

All the software program and system data which is required for mission execution is saved in the memory module. SBC has 1mega-byte flash memory and 2mega-byte SRAM(Static Random Access Memory) even though 80486 CPU supports 4giga-byte physical memory address space. Eight 8×128Kbits flash memory chips build 1mega-byte address space in the SBC. 32 bits CPU data bus is divided into four groups and assigned to each flash memory chip. The flash memory sustains 80Krad at 200rad/hour environment and it is not sensitive to heavy ion effects(until $54MeV/mg \cdot cm^2$). Four 8×256Kbits SRAM chips build 2mega-byte address space. 32 bits CPU data bus is divided into four groups and assigned to each SRAM chip. The SRAM sustains 100Krad. SBC does not have L2 cache memory.

3) 1553 module

SBC has mil-std-1553 communication module. It handles all the communication between MSC and spacecraft bus to support software interface. General interfacing method between CPU and 1553 device is described in the fig.4. 4K words memory space for 1553 device is used in the SBC while the device has 16K words internal memory.

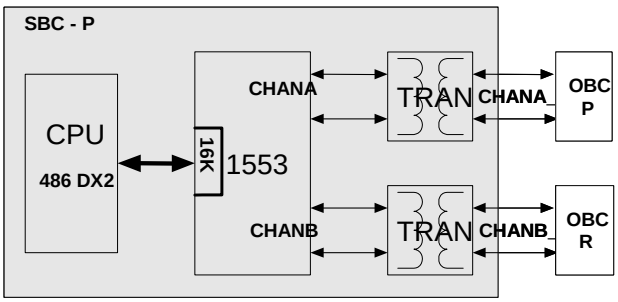

Fig. 4. 1553 device Interface

Due to the fact that 1553 device is 16 bits device, which means the chip has 16 bits data bus, special cares need to be taken to interface with 32 bits data bus CPU. In order to use linear address space from the point of CPU, 'word swapping logic' is required to steer the data word between MSW(Most Significant Word) and LSW(Least Significant Word) when the CPU reads and writes data. Nevertheless, it is handled in another manner in the SBC. Instead of using swap logic, the address bus from the CPU is connected to the 1553 device with 1bit shifted. Therefore, whenever the CPU access the memory of 1553 device, it always read and write LSW, that is, the CPU only access the data words which are aligned on the 4byte boundary. By doing this, complete memory space in the 1553 device can be accessed without the swap logic. 1553 device is configured as an RT(Remote Terminal) and it is connected to the 1553 bus using transformer coupling. Because 1553 device provide both A and B channel, primary and redundant SBC is connected with primary and redundant spacecraft OBC(On-Board Computer) with full cross-strap. 1553 device is configured not to generate CPU interrupt when it sends and receives new message, however, CPU checks it by polling.

4) RS-422 module

RS-422 module contains 8 UART(Universal Asynchronous Receiver & Transmitter) channels to manage all the sub-units by sending command messages and receives telemetry data. SBC has eight serial communication channels. Six of them are used to communicate with six sub-units of MSC system as described in the fig.2 and one of them is used to communicate with EGSE(Electrical Ground Support Equipment) which is

designed for debugging SBC itself at the development phase. The last serial communication channel is dedicated for developing embedded software with real-time operating system. General block diagram is shown in fig.5.

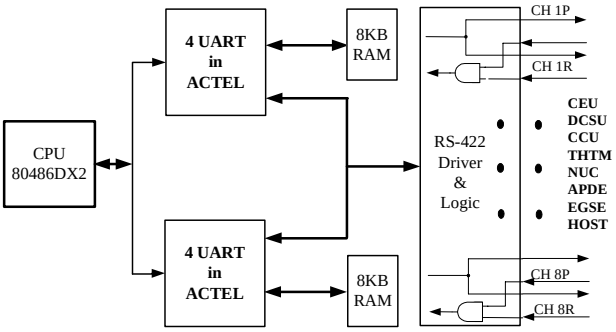

Fig. 5. RS422 Interface Diagram

Each serial communication channel is managed by a UART and four UART reside in one FPGA. Therefore, two FPGA are used to implement eight UART in the SBC. There is 2Kbyte FIFO(First In First Out) buffer between the CPU and each UART. CPU has only to writes data that is to be transmitted to the FIFO buffer, after then sends a command to the UART in order to start transmitting. By using this FIFO buffer, CPU doesn't need to wait for the completion of transmission. When SBC receives a message via this UART, no interrupt will stop the operation of CPU. CPU accesses the FIFO buffer to check if new message is arrived. Due to the fact that SBC does the flow control of the data as a master, FIFO buffer and polling mechanism is working effectively. Each UART provide three registers which enables the embedded software to control the UART. One is 'send/receive register', another is 'byte counter register', the other is 'control register'. One UART that is to be used for software development is implemented with full duplex and it is managed by the CPU interrupt. Because the UART is 8bits device, only the LSB(Least Significant Byte) of the data bus from the CPU is connected to the FPGA and FIFO buffer. From the point of CPU, four byte aligned address space is used for all UART, and three control registers for the UART are assigned to four byte aligned address.

5) Discrete Module

Discrete module deals with the bi-level signal to get discrete commands from spacecraft bus and represents some hardware status of MSC system. Spacecraft can reset SBC board using ‘reset’ discrete signal, and inform SBC using ‘safe-hold’ discrete signal that there will be emergency shut-down in 30 seconds, and provide 1Hz time-mark signal to synchronize both of them, and select one of both primary and redundancy SBC using ‘PMU active’ discrete signal. SBC can assert ‘PMU status’ discrete signal which tells that current SBC is working as an active SBC. All of these discrete signal interfaces are implemented using open collector circuit.

6) LVDS Module

LVDS(Low Voltage Differential Signal) module handles some signals to send accurate clock and discrete signal to NUC to activate image data stream. SBC provides 25MHz clocks to NUC board which will be used as a main clock signal for all the FPGA in the NUC. Because NUC includes several FPGA which handles different band of image data in real-time, therefore all of them need to be synchronized using the same clock. SBC also provides 1Hz time-mark signal to NUC which is received from spacecraft. SBC gives a trigger signal, start and stop photo, to NUC which enables image data stream. All of these signals are transferred through LVDS interface.

7) Interfacing FPGA Design

There is an FPGA(Field Programmable Gate Array) which manages all the timing and logic relation between these modules and CPU. It decodes address bus from the CPU and controls read and write cycle of RAM, flash and 1553 device read and write cycles. It includes PIC(programmable interrupt controller) and WDT (watch-dog timer). All discrete signals from the spacecraft are processed inside FPGA and transferred to CPU using interrupt mechanism. 32bits timer is implemented inside the FPGA and it is provided to CPU as a system clock which is used for real-time operating system. The FPGA can interface the signals from 5v biased CPU, 3.3v biased SRAM and 5v biased flash memory.

8) Other features

Software program in the flash memory can be reprogrammed using the serial communication channel which makes it possible to update the software without removing the flash memory from the SBC board. SBC uses different kinds of bias voltage. CPU uses 5v, and SRAM uses 3.3v, flash memory requires 5v and 12v for on-board programming, 1553 device uses 5v and 15v for driving bus. A few additional layers have been inserted in the SBC PCB to enhance the thermal conduction.

4. Conclusion

SBC is a main controller of the MSC system and plays very import roles for the mission executions. The simple and robust design of the SBC board will make it possible to operate 100% duty cycle in the space.

References

[1] MSC Critical Design Review Package
[2] SBC Hardware Requirement Specification
[3] Intel 80486 Processor Developer’s Manual
[4] MSC PMU Interface Requirement Specification
[5] MSC-BUS Interface Control Document