Development of High Speed Satellite Data Acquisition System

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Abstract: The downlink data rates of the space-born payloads such as high-resolution optical cameras, synthetic aperture radars (SAR) and hyper-spectral sensors are being rapidly increased. For example, the image transmission rates of KOMPSAT-2 MSC(Multi-Spectral Camera) is 320Mbps even if on-board image compression scheme is used.[1] In the near future, the data rates are expected to be a level 500~600Mbps because the required resolution will be higher and the swath width will be increased. This paper describes many techniques they enable 500Mbps data receiving and archiving system.

Keywords: Remote Sensing Ground Station, KOMPSAT-2, SAR Ground Station.

1. Introduction

Satrec Initiative Co., Ltd (SI) was selected as "National Research Laboratory (NRL) for Satellite Image Receiving and Processing System" by Ministry of Science and Technology in 2001. The topics of the NRL project are development of SAR processor and 600 Mbps data receiving system. In this paper, we will present the development of high-speed data receiving system.

Our data receiving system consists of a Pentium PC, high speed RAID, receiving and archiving software, and data receiving card. In the paper, we will describe how the system is configured, what algorithms and techniques are specially used for receiving and archiving high-speed data, and how the data receiving card is designed. At this moment, our system can receive and archive up to 500Mbps. Also, for the future satellite, 600Mbps will be required and we will describe our plan for the development of 600Mbps system.

This paper describes many techniques they enable 500Mbps data receiving and archiving system. Section 2 describes the overall architecture of real-time satellite data receiving and archiving system, Section 3 analyzes the bottleneck of bandwidth improvement. Section 4 describes the improvement techniques of interface bandwidth with antenna system. Section 5 describes the technique that increases the writing bandwidth of storage system that is using COTS (commercial-off-the-self) hardware. Section 6 describes the software buffering technique that enables reliable data recoding in the case of instant speed degradation of COTS components.

2. Overview of RAS system

This section presents the overview of SI's remote sensing image receiving and archiving system (RAS). The RAS system consists by antenna system interface, Data Receiving Card (DRC), host computer using Windows OS and RAID system that is the hard-disk based high performance storage system.

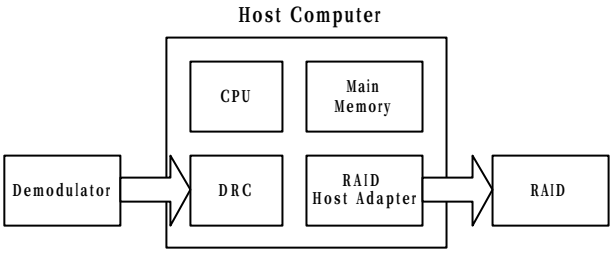

Fig. 1. Hardware Components of RAS.

Fig.1 indicates a simplified view of the RAS system. The downlink data are demodulated and bit-synchronized in the demodulator. The resultant serial data and synchronized clock signal transmit to RAS system. DRC (Data Receiving Card) interfaces the serial data between demodulator and RAS system. It converts the serial data to parallel form, and stores them in a internal memory (FIFO) temporarily, when the it's FIFO is filled with a certain amount of data, it generates an interrupt to the host computer. The software in the host computer recognizes the interrupt from DRC, transfers data from DRC FIFO to main memory, and finally sends the data to RAID through RAID host bus adapter (HBA).

3. Bottlenecks of Bandwidth Improvement

We will begin by considering the bottleneck of bandwidth improvement. We analyze the problem by flow of data signal. This is the central problem of the bandwidth improvement.

- Interconnection with demodulator system.
- Transmission line termination at DRC
- Internal buffer size of DRC
- PCI interface bandwidth of DRC
- The limit of data writing speed of RAID system
- Instant decreasing of I/O performance by RAID and not real-time OS.

4. Improvement of DRC

DRC has three important functions. First, it connects the RAS to the demodulator system. Secondly, buffers the data. Thirdly, interfaces with main-board of host computer by Peripheral Component Interface (PCI).

1) Interconnection with Demodulator

Generally, The demodulator of remote sensing ground station transmits the serial data and synchronized clock signal and the signal output circuit is consisted of Emitter Coupled Logic (ECL) for very high-speed operation. When designing system interconnection, four parameters must be taken into consideration:[2]

- Propagation delay per unit length of line;
- Line attenuation;
- Cross-talk;
- Reflections due to mismatched impedance characteristics of the line, connectors, and line terminations.

For solving the propagation delay, line attenuation, and cross-talk problems, we used same length shielded coaxial cable of data and clock line.

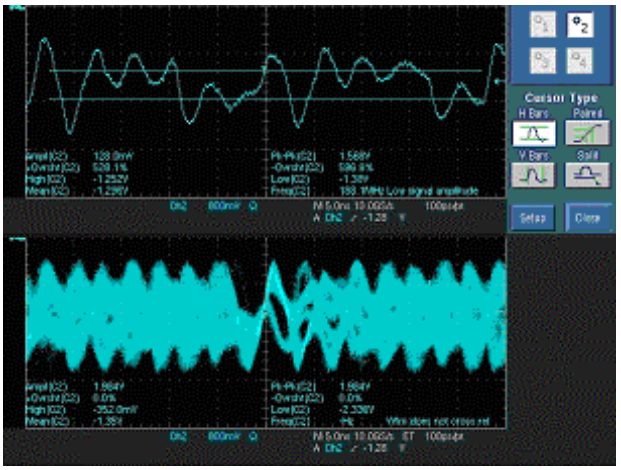

Fig. 2. "Y" Terminated Signal. (360Mbps Serial Data Signal)

The termination of ECL signal transmission line is relatively difficult problem. When high-speed signals are transmitted over long lines, terminations should be used to minimize reflections and distortion. In ECL system, every output must be terminated matching characteristic impedance of the transmission lines. We applied four types terminations mentioned below:[3]

- Parallel Termination
- Thevenin equivalent parallel termination
- "Y" Termination
- Differential Twisted Pair Lines Termination

The "Parallel Termination" and the "Thevenin equivalent parallel termination" set best performance. But, the "Parallel Termination" method needs another power supply so we finally applied "Thevenin equivalent parallel termination".

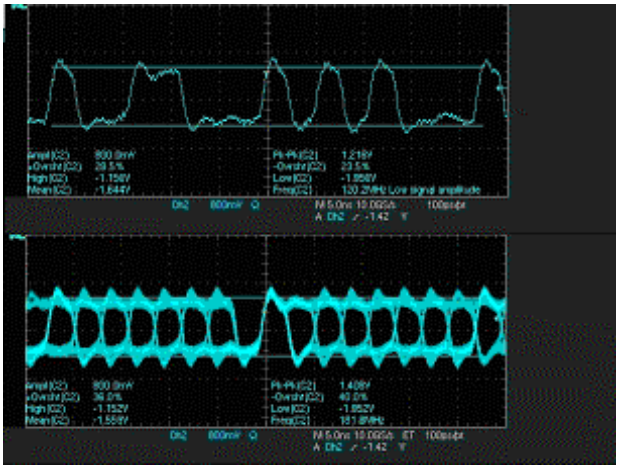

Fig. 3. Terminated by "Thevenin Equivalent Parallel Termination". (360Mbps Serial Data Signal)

2) Extension Buffer and PCI Bus Bandwidth

We experimentally find out the I/O bandwidth of host computer is increased logarithmically by the data block size of input and output. So we increased the internal buffer size of DRC. In practice, four 512kByte FIFO chips that are connected in a cascaded manner are used for DRC internal buffer currently providing 2Mbyte in total. Since the input data is ingested continuously into the DRC internal buffer.

For data ingestion, the bandwidth of host computer PCI bus is a square of input data rates. Because of host computer have to two PCI bus operations at an ingestion cycle. The host computer processes the sequential read and write process that transfer a block of downlink data from DRC to main memory of host computer by PCI bus and write the block to RAID system by PCI bus also. So DRC have to support 1Gbps bandwidth for 500Mbps data ingestion. The maximum input or output data rate of 32bit 33MHz PCI interface is 800Mbps. We finally extended the PCI bus synchronized clock to 66MHz. Then the Direct Memory Access (DMA) that transfers the downlink data from DRC internal buffer to host computer main memory is over 1Gbps bandwidth.

5. Enlargement Storage Bandwidth

The bandwidth of storage system is a square of input data rate for no loss storing. Because, the downlink data acquisition and storing processes have to sequentially operated. So storage system has to support 1Gbps bandwidth for 500Mbps data ingestion. But, recently RAID system only supports 800Mbps bandwidth. However we put tens famous storage system into the benchmark test that measures the continuous writing speed, can't find out the storage system meets the bandwidth requirement. Fig.4. indicates the test result at shortage storage bandwidth.

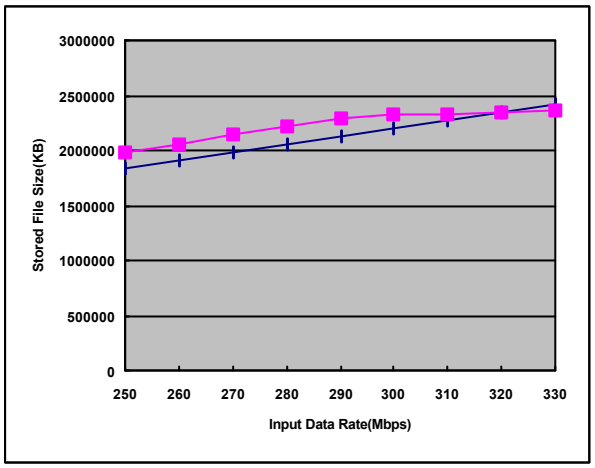

Fig. 4. Upper line shows actual file size, under line shows expected file size. The actual file size hang on the limitation because the bottleneck of storage bandwidth.

We get over this limitation by apply the software stripping technique. Fiq.5. shows the hardware structure of the constructed storage system. Two independent RAID systems connect the host computer using each PCI host adapter. And bind them using the stripe set utility supported by Windows OS. So we can use them like one RAID system and the bandwidth is increased about 50%.

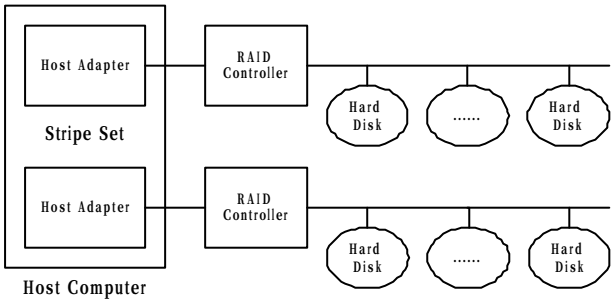

Fig. 5. The Structure of applied Storage System.

6. Reliable Receiving and Archiving Software

The data writing process shows instant and frequent speed degradation as shown in Fig.6. This instant speed degradation may be caused by RAID system and internal operations of the operating system. The instant speed degradation like this in data writing process causes data lost, and consequently unreliable data receiving and recoding capability.

We conquer this problem using software buffering technique.[4] The concept of the software buffering technique is simple. The software uses a large amount of host main memory as a buffer and the data ingestion process divide each read and write thread. The buffer memory executes the role transfer the data from read tread to write thread and absorb the data overflow.

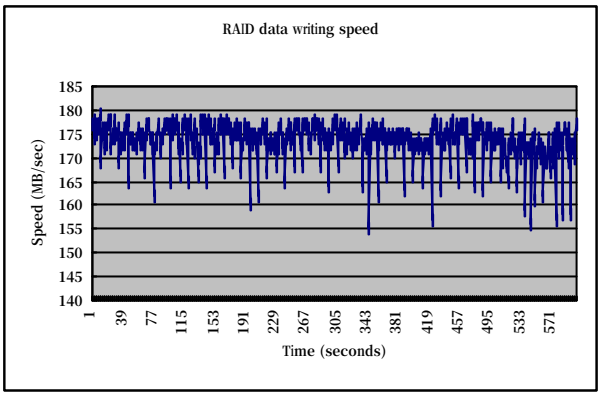

Fig. 6. RAID data writing speed example.

7. Conclusions

In this paper, describes the whole steps of development high-speed satellite data acquisition system. The point is that extend the bandwidth of receiving and archiving system. In the future, we will develop more high-speed system for the SAR and hyper-spectral satellite.

References

[1] KARI, 2000. KOMPSAT-2 System Requirements Review, Korea Aerospace Research Institute

[2] Motorola, William R. Blood. Jr., MECL System Design Handbook, Fourth Edition.

[3] SEMTECH, 2001, Termination Techniques for ECL/LVECL/PECL/LVPECL Devices.

[4] D. S. Shin, W. H. Choi, M. G. Kim and W. K. Park, 2002. Software Buffering Technique For Real-time Recording of High Speed Satellite Data, *J. the Korean Society of Remote Sensing*, 18(3): 147-153.

[5] **URL:** Satreci Initiative Image Processing Solution http://www.satreci.com/~siis.