고전압 GCT(Gate Commutated Thyristor) 소자 설계

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A Novel Design for High Voltage RC-GCTs

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Abstract

Basic design of RC-GCTs (Reserve-Conducting Gate-Commutated Thyristors) by novel punch-through (PT) concept with 5,500V rated voltage is described here. A PT and NPT (non punch-through) concept for the same blocking voltage has been compared in detail. The simulation work indicates that GCT with such PT design exhibits that the forward breakdown voltage is 6,400V which is enough for supporting 5500V blocking. Additionally, the real IGCT turn-off in the mode of PNP transistor has been realized. However, the carrier extraction from N-base to gate terminal will be drastic slowly in terms of NPT structure except for the high on-state voltage drop.

Key words : Gate Commutated Thyristor (GCT), turn-off.

1. Introduction

Integrated gate commutated thyristors (IGCTs) is the new power semiconductor device used for high power inverter, converter, static var compensator (SVC) etc. Hyuandai Heavy Industry Corporation in Korea has already developed 2730kVA IGCTs inverters using 4,000A, 4,500V GCT device for high- speed traction drives. Prospectively, IGCTs could be the power device used for such high-speed traction drives in China in the near future.

In this paper, 1500A, 5500V RC- GCTs with PT concept has been described.

2. Basic Design Concept

Most of the ordinary GTOs (gate turn-off thyristors) are designed as non-punch-through (NPT) concept; i.e. the electric field is reduced to zero within the N-base region. The N-base width has to be increased in order to have the higher blocking voltage in the NPT GTOs. However, the novel punch-through (PT) concept instead of NPT has to be applied for modern IGCTs. In PT design, an additional N-buffer layer stops the electric field extension before it reaches through into the anode region. Thus, a trapezoidal shape of the electric field can be achieved as shown in Fig.1. The device with such electric field distribution can block the high voltage with a substantially reduced N-base thickness. Since the on-state voltage and switching losses strongly depend on the thickness of silicon wafer used, it is highly desirable to develop PT concept with minimal N-base thickness for a given blocking voltage.

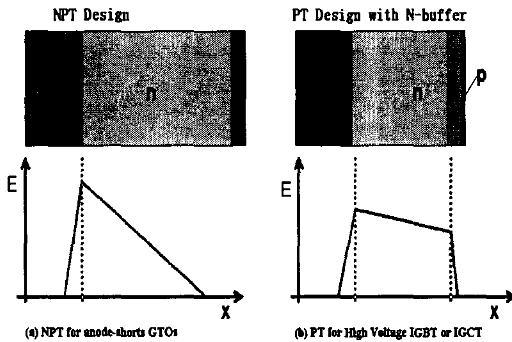

Fig .1. NPT and PT structures.

The RC-GCTs with PT concept is shown in Fig. 2, that the right part is the basic GCTs portion. The left part is the FWD (free-wheeling diode) portion that is integrated in anti-parallel connection with GCTs. For PT design, the N-buffer layer has to be optimized. In order to obtain the fast extraction of carrier stored in the N-base, the shallow transparent P+ layer in adjacent to N-buffer is needed.

For high voltage IGBTs[1], it is necessary to minimize the wafer thickness by PT design to obtain low on-state voltage drop and short turn-off time by means of a dedicated high resistivity FZ N-type silicon. The similar issue has to be considered for high voltage GCTs in terms of the fast extraction of stored carriers in N-base. The selection of N-base parameter is mostly important for PT design. If the N-base width is thicker, the blocking voltage is surely high, however, the on-state voltage will be high and, turn-off time will be long as well. By means of the PT design, the thinner N-base width is possible. Moreover, a higher resistivity used can easily result in flat profile of electric field and real punch-through. Therefore the thin N-base width with the high resistivity is preferable for novel GCTs design.

The basic structure in this paper is punch-through wafer having resistivity of 550Ω cm. The N-base width was determined in 405㎛ for support breakdown voltage of 6,400V. The junction depth of B-Al is 125㎛. The N-buffer layer in the anode- side is 70㎛ in depth and P+ transparent layer depth is 12㎛. The resultant Si wafer thickness is 600㎛.

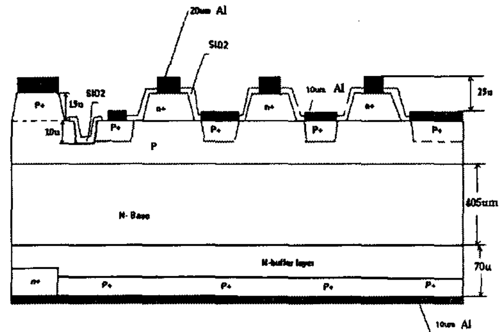

Fig. 2. Cross-sectional view of RC-GCTs.

3. Static Performance

Fig.3 shows the simulation results on electric field and doping profile for bulk region of GCT. Evidently, the electric field stops by the N-buffer layer and the maximum electric field at the main junction J_2 reaches to 1.5×10^5V/cm. For support high voltage in forward direction, the bevel contour of 1.6 degree was applied to surface of main junction J_2. Fig.4 gives the electric field profiles along the line which across the Emax under the 1.6 degree of surface bevel contour when the device breakdowns. It is worth to note in Fig. 4 that maximum electric field ($E_{max}=2.25\times10^5$V/cm) is located beneath the bevel surface about 75㎛. So an effective passivation layer has to be carefully selected to protect the surface breakdown for high voltage PT device.

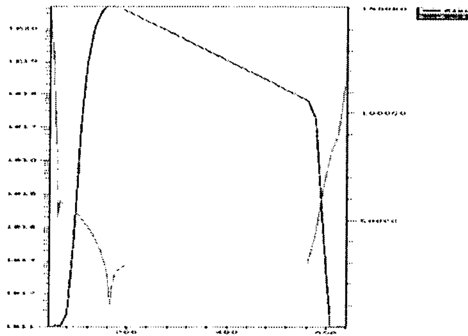

Fig. 3. Electric field (blue line) and doping profile for bulk region of GCT for 6400V breakdown.

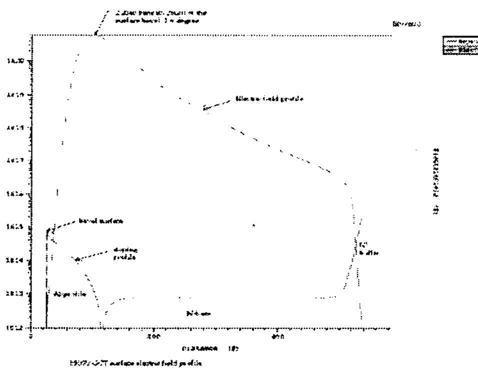

Fig. 4. Surface Electric Field vs doping at maximum electric field beneath 75m of negative bevel.

Fig. 5 shows the breakdown characteristics. It is clearly that this PT design can obtain breakdown voltage of 6,400V. This is enough for support the forward rated blocking voltage of 5,500V.

For the NPT, the N-base width must have at least 740㎛ to support the same breakdown at 6,400V, and the total wafer thickness will be around 1000㎛. Apparently, the N-base width of PT design can be almost 65% of that used for NPT design. The on-state voltage drop (V_{TM}) is expected to be 1.70V in NPT, however, V_{TM} is only 1.36V for PT device as shown in Table 1. Nevertheless, too thicker N-base width of NPT will result in the drastic slow extraction of carriers and long tail current occurred during turn-off. Therefore, NPT concept is unable to be accepted by modern high voltage GCTs.

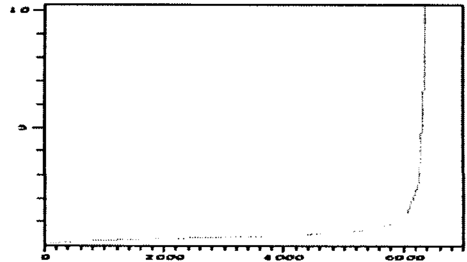

Fig. 5. Forward breakdown voltage characteristics.

4. Dynamic Turn-Off

Fig. 6 shows the mask design for 1,500A, 5,500V RC-GCTs. In the center of Si wafer, free-wheel diode (FWD) is located. The GCT has 4-concentric array with a ring gate terminal for purpose of turn-on and turn-off. The trench 30㎛ in depth for isolation of GCT and FWD is grooved down.

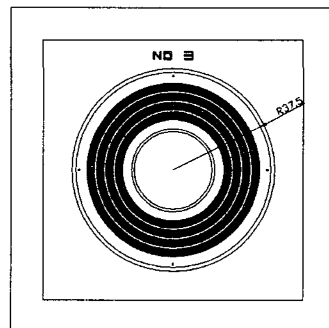

Fig. 6. Mask layout for RC-GCTs.

Fig.7 indicates the dynamic turn-off waveform at turn-off current I_{TGQ} =170A. From this figure, it is clearly that the rise rate of

Table 1. Comaprison of PT and NPT for same breakdown of 6.4kV with -1.6 degree beveling structure.

	ρ_N (Ω•cm)	W_{NB} (μm)	T_{SI} (μm)	X_{JB-AL} (μm)	$T_{N-BUFFER}$ (μm)	$T_{P+TRANSP.}$ (μm)	V_{BO} (V)	E_{MAX} (V/cm)	V_{TM} (V)
PT design	550	405	600	125	70	12	6400	1.5e5	1.36
NPT design	300	740	1000	130			6400	1.5e5	1.70

negative gate current for turn-off ($-di_G/dt$) has already reached up to 850A/μs when re-applied voltage V_D=220V. Therefore, the IGCT turn-off mode i. e. the PNP transistor turn-off mechanism has really been obtained in our design since the sharply negative gate turn-off current ($-di_G/dt$). This is quite differently with the ordinary GTO turn-off in which the rise rate of negative gate turn-off current is too slow (typical $-di_G/dt$ 30A/μs for GTO). The negative gate turn-off current is so sharp that the commutation of anode current to gate terminal is robust. Fig. 8 shows the turn-off waveform at higher anode current of 1,500A when 3,500V DC voltage was applied. The device exhibited the fast turn-off (storage time t_s is only 2μs), and a low tail current has been observed since the narrow N-base has been adapted. If the local carrier lifetime control by proton irradiation[2] can additionally be applied to this device, the tail current will be certainly neglected.

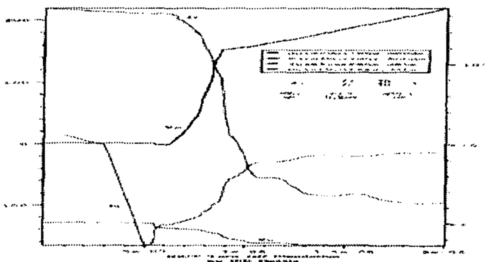

Fig. 7. Turn-off waveform: I_A=170A;V_A=220V; I_G=-170A; V_G=-16V; C_s=0F.

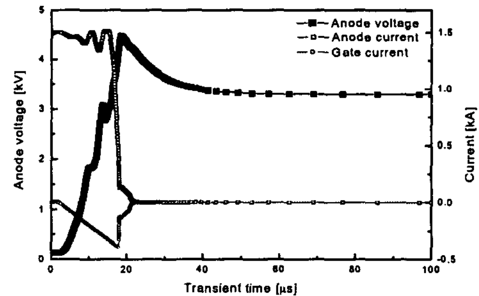

Fig. 8. Turn-off waveform: I_A=1500A;V_D=3500V, C_s=0.

5. Conclusion

The PT structure of 5,500V RC-GCT in this investigation was optimized by simulation. The results indicate that the GCT can have 6,400V for forward breakdown voltage and 1500A for turn-off current. The PT GCTs exhibits the good static performance and dynamic turn-off.

Reference

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