HVDC 송전을 위한 8.5kV급 광 구동 사이리스터의 설계

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The Design Concept of 8.5kV Light Triggering Thyristor(LTT) for HVDC Transmission

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Abstract

The design rule for 8.5kV LTT was discussed here. An inherent integrated breakover diode (BOD) for self -protection function and multi-amplified gate (AG) for improved di/dt capability of LTT was introduced in principle. The trade-off between light triggering input source and high dV/dt limitation has been treated via narrow grooved P-base for gate design. Key process technology for LTT was given, too.

Key Words : Light triggering thyristor, High Voltage DC Transmission

1. Introduction

In the early 1980s, the high voltage DC transmission (HVDC) has been developed by usual electrically triggering thyristors (ETT). In order to improve the reliability of whole HVDC system with reduced electronic elements adopted in thyristor valve, ETT has been replaced by light triggering thyristors (LTT). 4kV/3kA LTT has been developed by Hitachi in 1985. And in 1993, Hitachi has developed 6.6kV/1.2kA LTT used for 300MW (DC ±250kV) HVDC converter. In 1995, 8kV 3.5-5kA LTT was developed in Hitachi for Back to Back (BTB) system. At the same time, Siemens has developed 8.5kV LTT with the integrated break-over diode. In 2002, Siemens has transferred all of process technology of LTT to Xi'an power Electronics Research Institute (PERI) of China upon the cooperation project for 500kV HVDC transmission linked from Guizhou to Guangdong in China. The design concept for 8.5kV LTT are introduced in this paper.

2. Light Triggering Thyristor

2.1 Feature of LTT

In principle, the basic fundamental and fabrication technology of LTT is similar to ETT (Electrical Triggering Thyristors). Fig.1 shows the silicon wafer and its house for 8.5kV 3.5kA LTT. The triggering mechanism and method of LTT is quite different with that of ETT. For LTT, light is directly triggered to the gate via the optical fiber. The carriers activated by light in the light sensing area will turn on the four-layer of PNPN switch shown in Fig.2. And for ETT, the gate current is needed to fire the four-layer of PNPN switch by positive gate voltage pulse. Due to this difference, the switching performance and process technology for two devices has been affected significantly. In LTT, very slightly light signal is needed for directly light drive. Moreover the energy of light for trigger is only one to several tenth of electrical energy for ETT. Therefore, how to improve the light sensitivity without sacrificing dv/dt are the major objectives to LTT's design.

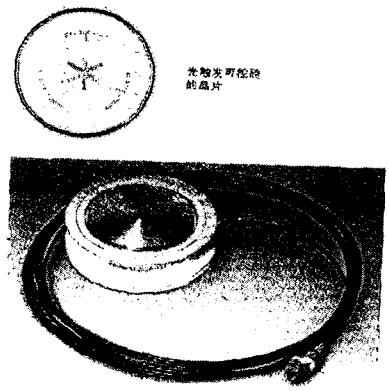

Fig. 1. The Si wafer with assembly house attached the light fiber for high voltage LTT.

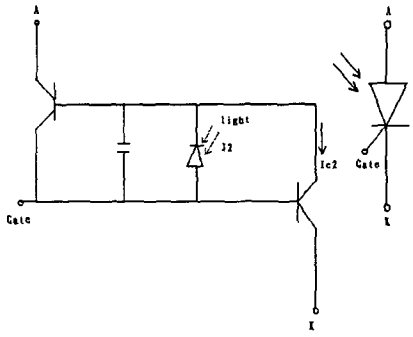

Fig. 2. The symbol and equivalent circuit for LTT.

2.2 Light Triggering against dV/dt

As mentioned above, the gate triggering power (i.e. light triggering power) is significantly relevant to switching characteristics of device for instance turn-on time, delay time, dv/dt performance etc. The triggering power in ETT should either be large enough to meet "heavy triggering" or be strong enough for light power in LTT. From other hand, the output power of currently light source i.e. LED in the today's available market is little low, so the specified structure receiving light in gate area of Si with highest sensitivity is adopted in LTT. In this case it can be obtained light triggering input power less than 10mw(see Fig. 5) if the mentioned specified structure is applied. This means that the area of light sensitive structure in central part of LTT (See d indicated in Fig.3) should be as small as possible. Otherwise the failure features carried out by dV/dt capablity i.e the capable of the thyristor to withstand voltage ramps of several kV/s without being triggered by the resulting displacement current, would suffer. The small structure requires particular protection measure against the onrush of the turn-on current. This is usually done by means of multistage amplifying gates. A lateral current limiting resistor has to be used in additional [1].

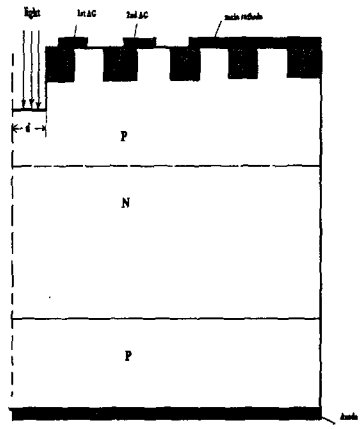

Fig. 3. The basic structure of LTT with grooved p-gate.

2.3. Self-protection of integrated BOD

The novel LTT integrates the both light triggering and over-voltage protection function into a single wafer in order to simplify protection unit assembled in the stack of thyristors valve. From up-to-date technology, it is possible to integrate the over-voltage protection function into the inner of device. But in reality the break-over voltage by (see Fig.6) integrated built-in break-over diode (BOD) should be larger than the minimum voltage that is applied DC voltage in the circuit (V_D). And additionally this voltage ranges should not be so big i.e. it lies in some narrow range, which upper limit (V_{BOD}) should

be smaller than the forward blocking voltage (V_{DSM}) of main device in adequately. To realize this target, the common way is to have chemical or laser etching Si to form recessive structure.

To achieve this target, non-uniformity doping or curved PN junction (etching off the thin layer for B-Al pre-deposit) was adopted in LTT.

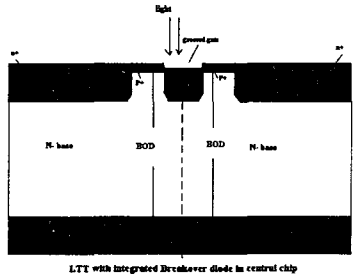

Fig. 4. LTT structure with improved BOD.

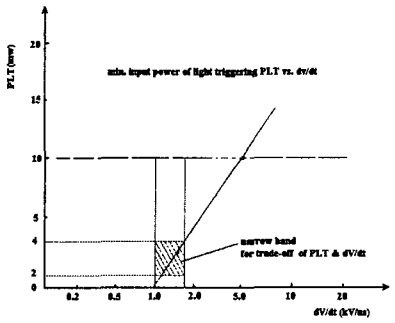

Fig. 5. The relationship of min. input power of light triggering PLT and dv/dt.

2.4 Self-protection Against dV/dt

LTT device should be withstand to instantaneously inrush high dv/dt at several kV/s. If this dV/dt is too low then destruction will be resulted from " re-triggering" in the thyristor. In terms of LTT, dv/dt limitation is very important parameter. However dv/dt and light triggering sensitivity are contradictory parameters, so the compromise between two items is necessary.

Since LTT requires very high in the light sensitivity, the dv/dt limitation will be, therefore, sacrificed. Together with all these items, it is necessary to adjust the doping profile of P- base and its circumscription. In addition, to adjust the amplifying gate (AG) and cathode design can ensures its nominal dv/dt limitation. This procedure is so complicated that difficult to be controlled in proper technology.

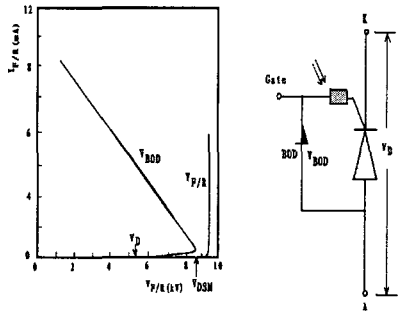

Fig. 6. I-V characteristics of a BOD protected 8.5kV LTT thyristor in the forward mode.

2.5 Ensures of di/dt limitation

High di/dt specification, which is requested from HVDC valves, should be solved in emphasis. The triggering sensing area is very small due to sensitive requirement of LTT. And light energy for triggering is only one to several tenth of electrical triggering energy, too. This is harmful to turn on and therefore, severe impact on di/dt. LTT for this design is composed of five-stages of amplifying gate with a novel integrating bulk resistor, which has an optimization design. As shown in Fig.7, the 1st AG; 2nd AG; 3rd AG; 4th AG; 5th AG forms 5 stages amplifying gate and P^+ base can be considered to have bulk resistor R. Nevertheless, during turn-on phase the 5 auxiliary thyristors turn on consequently, then the main thyrsitor turns on. This will affect the effective Si area to be lost somewhat against existing BOD in the inner of wafer [2].

2.6 Key technology for process

The production process of LTT can, in principle, be similarly to ETT. The triggering structure, however, has to be made quite differently. This has a severe impact on production process. All these differ in the following as compared to ETT:

1) High resistivity of 530Ωcm N-type NTD wafer in thickness of 1490㎛ has to be selected as raw silicon material.
2) For curved PN junction of BOD area, the shallow 7㎛ pre-deposit layer was formed by Al vacuum pre-deposition. And etching of this layer, drive-in process by Al diffusion at 1250 ℃/65hrs is possible. Final junction depth for un-etched Al will be 150㎛.
3) Second Al pre-deposition by vacuum sealed tube and drive-in in order to get high concentration for p-base.
4) Following process is $POCl_3$ diffusion and Boron diffusion as same as usual ETT.
5) Double negative bevel angle is needed for surface contour.
6) The LTT housing needs a very narrowly tolerated alignment of the optical fiber inside the housing for good light yield on the wafer. This is also an critical issue in packing and shipping LTTs and will affect reliability if handled not properly.

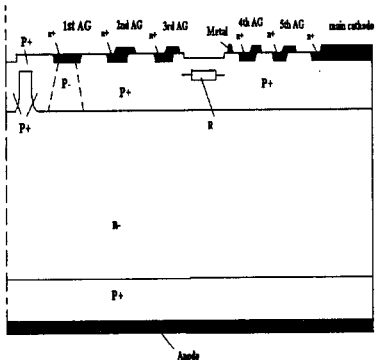

Fig. 7. 5-stages of amplifying gate and BOD with current limiting resistor R for LTT design.

3. Conclusion

The basic design for light triggering p-base and integrated BOD has considered. The trade-off for self-protection against dv/dt capability has been achieved. Improved di/dt limitation against amall light sensitive area via 5-stages amplifying gate has been in our design.

Reference

[1] V. A. K. Temple, "Turn-on reliability breakthrough in light triggered thyristors", in Proceedings of IEDM, pp. 16.1, 1984.

[2] H. J. Schulze, etc., " Light Triggered 8kV Thyristor with a New Type of Integrated Breakover Diode', IEDM, 1999.