Calibration Methodology for TCAD System

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1. Introduction

Accurate and reliable TCAD (Technology Computer-Aided-Design) tools play a major role in development and manufacturing of semiconductor. The progress of ULSI (Ultra Large Scale Integrated Circuit) technologies to yield higher density DRAM and ultra-high performance and low power chips has brought with it the need to use in a wide variety of ways of TCAD tools. As ULSI technology advances, the accuracy and predictive capabilities of process simulation have become more and more important in device design and development [1]. Furthermore, it is necessary to use the process simulation parameters which are globally applicable to all kinds of devices in fabrication.

2. Methodology & Calibrations
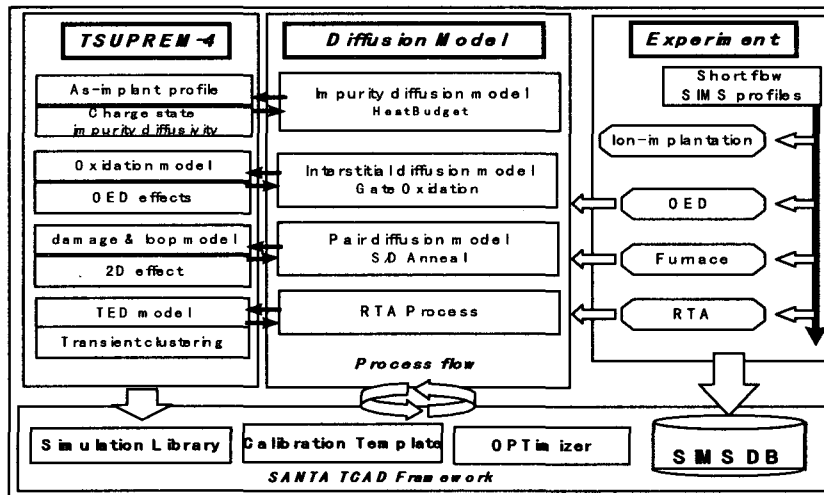### 2.1 Methodology

Fig. 1 Calibration Methodology for TCAD System.

We analyze the implantation, gate oxidation and annealing process conditions of each process technology generation to make the critical point of experiment window. Based on this experiment window, we process the short-loop experiment such as in the right box of figure 1. The SIMS data are stored as TCAD-DB (Data-Base) for efficient handing[2]. From the target SIMS data, we optimize the parameters which are previously determined for each

process condition by the sensitivity analysis. Such as the box diagram of center and left in figure 1, we sequentially extract the diffusion parameters starting from the intrinsic carrier concentration region with impurity diffusivity to TED (Transient Enhanced Diffusion) parameters. Then the set of the extracted parameters are validated by the device simulation in term of electrical characteristics.

2.2 Calibration

With 175 SIMS profiles which cover the whole range of conditions of implant and diffusion processes in the fabrication lines, the dominant diffusion phenomenon in each process temperature region has been determined. From the fully-coupled diffusion model [3], impurity diffusivities at the high temperature over 950℃ and interstitial-related parameters from the OED (Oxidation Enhanced Diffusion) phenomenon at 900℃ have been sequentially extracted. Then, the parameters for the impurity-defect pair movement have been extracted because the impurity redistribution and dopant activation are dominant below 850℃. In addition to implant and furnace diffusion calibration, the TED (Transient Enhanced Diffusion) parameters in RTA models including the silicidation process have been extracted at the final calibration step. The adjustment of parameters for the dose loss and snow plowing effects has been considered for the whole temperature region.

2.3 Results

Fig. 2 shows that the simulation results for ion-implantation with calibrated parameters are well matched to the peak and tail regions of as-implanted SIMS profiles for arsenic impurities. Fig. 3 shows the TED simulation results of high-dose RTA process. The simulation and SIMS data do not match perfectly, but can be a good inputs for device simulation and characterization. Also we calibrated that the fluorine effect on boron impurity diffusion which retarded the boron TED with modification of pair-reaction parameters.
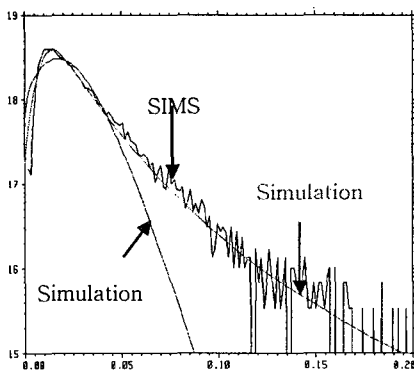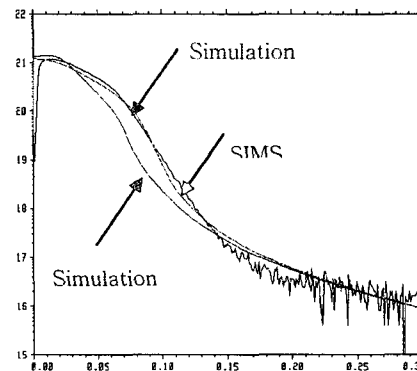

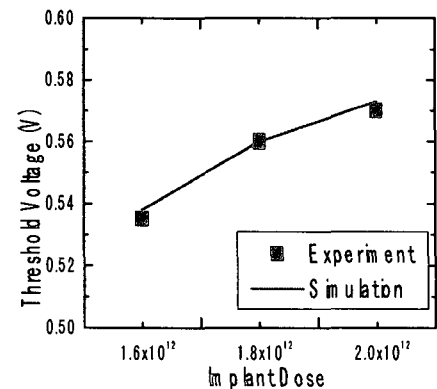Fig.2 Calibration of Implantation.   Fig 3. Calibration of RTP anneal   Fig 4. Simulation of Vth vs. Dose

2.4 Applications

We applied the globally calibrated process simulator parameters to memory and logic devices to predict the optimum process conditions for target device characteristics. Fig. 4 shows the DRAM NMOS threshold voltage simulation with the maximum 1% error to the experimental data for the various gate lengths and channel doping conditions. Based on the simulation, we can control the threshold voltage roll-off and the surface punch-through current in the n^- region.

3. Conclusions

We have constructed a systematic calibration methodology for the ion-implantation and diffusion process simulation. The accuracy and efficiency of the globally extracted parameters will be successfully validated in the process design of 1G-DRAM and 90nm logic transistors.

References

[1] T. Kunikiyo, K. Mitsui, M. Fujinaga, T. Uchida and N. Kotani, " Reverse short-channel effect due to lateral diffusion of point-defect induced by source/drain ion implantation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume: 134 , 507 - 514, April 1994.

[2] Jun-Ha Lee, Seung-Woo Lee, Jeong-Taek Kong and Young-Wug Kim, " Systematic Calibration for Transient Enhanced Diffusion of Indium and It's Application to 0.15um Logic Devices," 6th International Conference on VLSI and CAD (ICVC ' 99), 53-56, 1999

[3] M. Y. Kwong, C. H. Choi, R. Kasnavi, P. Griffin and R. Dutton., " Series Resistance Calculation for Source/Drain Extension Regions Using 2-D Device Simulation," IEEE Trans. ED, vol.49, No. 7, July 2002