A Dual-Level Knowledge-Based Synthesis System for Semiconductor Chip Encapsulation

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Abstract

Semiconductor chip encapsulation process is employed to protect the chip and to achieve optimal performance of the chip. Expert decision-making to obtain the appropriate package design or process conditions with high yields and high productivity is quite difficult. In this paper, an expert system for semiconductor chip encapsulation has been constructed which combines a knowledge-based system with CAE software.

1. Introduction

Knowledge-based systems have been proposed as tools for constructing a rational design system for injection molding.

Semiconductor chip encapsulation is employed to protect the chip and to achieve optimal performance of the chip. Transfer molding is currently the most popular process for encapsulating integrated circuits[1]. The design and manufacture of semiconductor chips with desired properties is a costly process dominated by empiricism, including the repeated modification of actual tooling. It is quite difficult to obtain package design or process conditions with high yields (i.e. with minimum encapsulation defects such as incomplete fill, part non-uniformity, wire sweep and voids) and high productivity.

Expert decision-making to determine the appropriate material, process conditions and package design requires an experienced designer's knowledge. The functions of evaluating the initial design and generating redesign recommendations are also needed to acquire a better design based on the design-evaluation criteria. In this paper, an expert system for semiconductor chip encapsulation has been constructed which combines a knowledge-based system with CAE software.

2. System Overview

The system used in this study is composed of two functional groups of software: a knowledge-base module and CAE programs. The overall control and user interface are

managed by an expert system (Fig. 1). The knowledge-base module includes heuristic and pre-analysis knowledge for evaluation and redesign. Evaluation of the initial design and generation of redesign recommendations can be developed from the rules as applied to a given chip package.

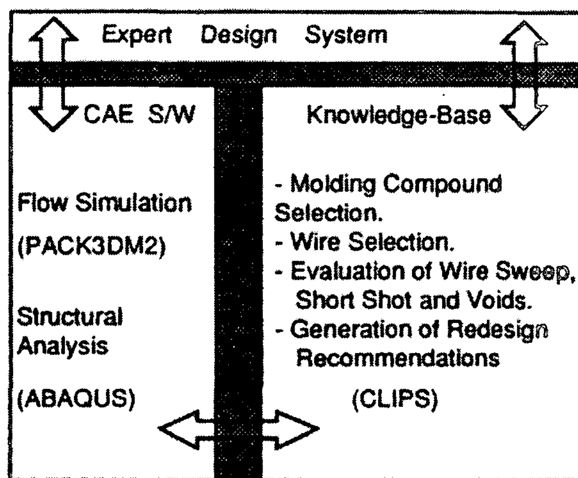


Fig. 1. A .Framework of Knowledge-based Synthesis System for Chip Encapsulation.

Table 1. Resulting Maximum Wire-Deflection Values for Original and Revised Process Conditions.

	Fill Time(s)	Mold T. (℃)	Wire Deflection(m)
Original	12	180	2.42e-4
Redesign 1	19	180	1.11e-4
Redesign 2	12	189	1.78e-4

The expert system can trigger necessary analysis modules, such as the flow-simulation program and the structural-analysis program. PACK3DM2[2)] has been developed to analyze the chip encapsulation process by the research group at CIMP (Cornell Injection Molding Program).

It can be used for simulating the filling and packing stage of encapsulation process. ABAQUS (a product of HKS Ins.) is used for structural analysis. These CAE programs perform analyses as requested, based upon decision made by the expert system.

3. Evaluation of the Process Condition

The semiconductor chip package is usually designed by an applications engineer to have the necessary functional requirements. Design tasks of chip encapsulation are composed of the selection of material, the decision of chip package geometry and the choice of process conditions for meeting the requirements of processability and performance of the package. In this study, the objective is to develop an expert system that can eventually perform these tasks. The first step in this regard has been to develop a module to evaluate the user-suggested process conditions. Specifically, this module checks whether the suggested process conditions will induce any processing problems such as wire sweep, incomplete filling of voids. This evaluation procedure has been divided into first- and second-level stages. The first-level evaluation stage is for a quick evaluation although its accuracy may not be adequate. The second-level evaluation uses CAE analysis and knowledge-base for more accurate evaluation. The flow charts for the first- and second-level evaluations are

shown in Fig. 2.

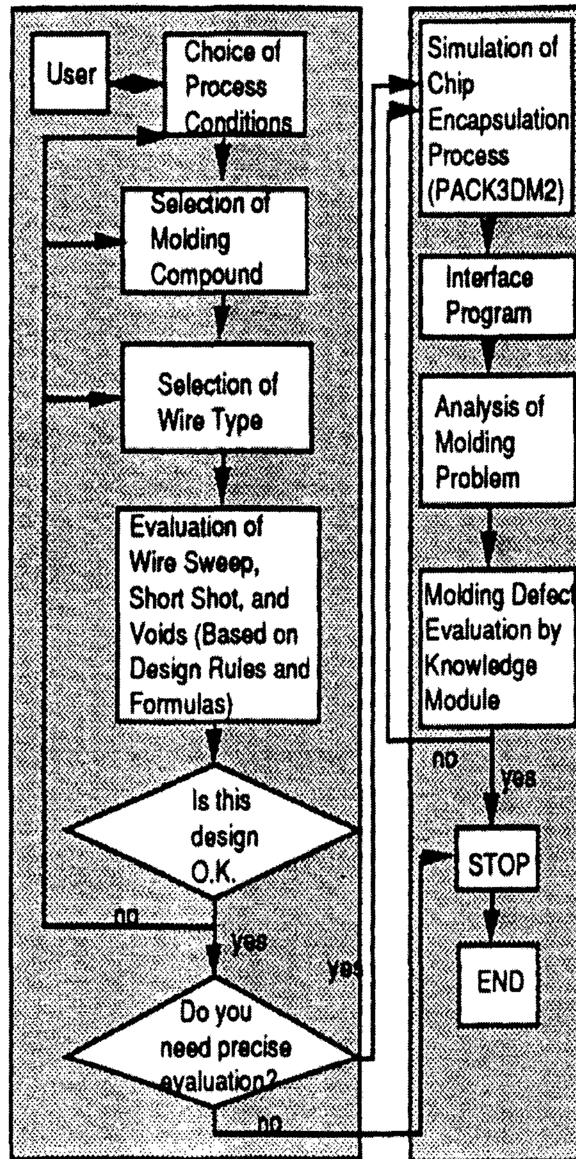


Fig. 2. Flow Chart of Knowledge-based Synthesis System for Chip Encapsulation.

3.1 First-Level Evaluation

The evaluation of wire sweep will be discussed first. In this regard, the behavior of a wirebond eformed by a moving front needs to be quantified. The use of a complicated CAE program for the wire-sweep analysis may take much time and so we suggest a different, more approximate, approach.

The following is an example of the rule used for wire sweep assessment in the case of a Nitto Denko molding compound.

IF: Molding compound is Nitto Denko [MP-180]
and Wire type is [SPM1]

and Wire sweep is bigger than [10percent]
THEN: Wire sweep problem is possible

The assessment of the possibility of wire sweep, short shot or voids is to be made through interactions between the designer and the expert system. The expert system may guide the designer to reach an acceptable selection of process conditions.

3.2 Second-Level Evaluation

In order to get a more precise evaluation of possible molding problems, a designer can trigger a second-level evaluation module. An example will be given for the wire-sweep problem evaluation.

To calculate the wire sweep, the drag force on the wire due to flow should be needed to know. This can be done by running PACK3DM2. First, the expert system requests the required input data to run the PACK3DM2 program. Then, the expert system triggers the PACK3DM2 program to get the maximum drag force on the wire during the filling and packing stage. For the wire-deformation calculation due to the given drag force, ABAQUS is used. The drag-force data obtained from the flow simulation is read by an interface program written in CLIPS to generate an ABAQUS input file automatically. The input data file includes the wire shape, the wire radius, the material properties of the wire, and the drag force. Using this input file, the wire deformation can be obtained by executing the ABAQUS structural-analysis program.

4. Generation of Redesign Recommendations

The expert system evaluates the molding process conditions. If a molding problem is not detected, then the procedure is completed. However, if any molding problem is indicated, then the expert system generates a redesign recommendation to eliminate the molding problem. In the case of wire sweep, the expert system searches the knowledge base for reducing the wire sweep. For example, it may recommend changing fill time, mold temperature and/or ram velocity profile.

An example of such an application will be given below. A schematic of the mold used for this study is shown in Fig. 3. Some of the results from the PACK3DM2 for the original process condition are shown in Fig. 4. The original processing conditions yield wire deflection of about 2.4×10^{-4} m for the wire in cavity 1(cavity at the leftmost side). The goal is to reduce the wire deflection value to 1.6×10^{-4} m(which is 2/3 of the original value). The original and expert-system suggested processing condition is shown in Table 1. The original new wire sweep values are given in the same table which shows that revised process condition give satisfactory wire sweep.

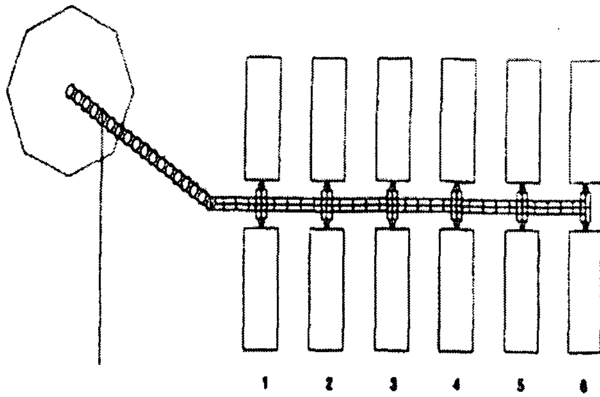
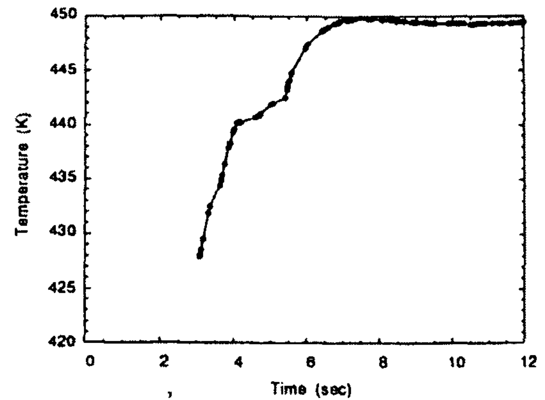
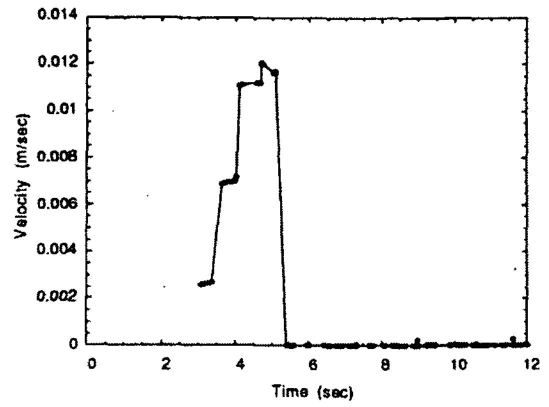


Fig. 3. A schematic of the mold for encapsulation.



(a)



(b)

Fig.4. (a) Temperature and (b) velocity change at the central point in cavity 1.

For the short-shot or void problem, no satisfactory quantitative redesign rules presently exist. We may, however, use qualitative redesign rules for the void problem as given below.

IF : The required pressure is smaller than the saturation pressure of the given molding compound and The required pressure is smaller than the allowable maximum pressure
THEN : Increase the pressure

New process conditions to improve the productivity of the process can also be recommended. For example, if the calculated wire sweep is smaller than the specification, the fill time can be reduced as long as the wire sweep is within specification.

5. Conclusions

At the present time, the expert system includes synthesis knowledge for evaluating and generating redesign alternatives to reduce wire sweep, short shot and voids. The expert system also includes material data for several molding compounds and wires. The modular

structure of the expert system allow expansion of the system to cover most attributes of the chip encapsulation by adding knowledge modules. For example, we can add design guide rules which is actually used by practitioner in the chip encapsulation field. Also we may add module to choose appropriate process condition if there is conflict between results obtained from different criterion.

References

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