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초미세 메모리 커패시터의 전극형성을 위한 식각 기술
Patterning issues for the fabrication of sub-micron memory capacitors' electrodes

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This paper describes some of the key issues associated with the patterning of metal electrodes of sub-micron (especially at the critical dimension (CD) of 0.15 μm) dynamic random access memory (DRAM) devices. Due to reactive ion etching (RIE) lag, the Pt etch rate decreased drastically below the CD of 0.20 μm and thus the storage node electrode with the CD of 0.15 μm could not be fabricated using the Pt electrodes. Accordingly, we have proposed novel techniques to surmount the above difficulties. The Ru electrode for the stack-type structure is introduced and alternative schemes based on the introduction of the concave-type structure using Pt or Ru as an electrode material are outlined.