Low Temperature Flip Chip Bonding Process

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Abstract

The low temperature flip chip technique is applied to the package of the temperature-sensitive devices for LCD systems and image sensors since the high temperature process degrades the polymer materials in their devices. We will introduce the various low temperature flip chip bonding techniques; a conventional flip chip technique using eutectic Bi-Sn (mp: 138℃) or eutectic In-Ag (mp: 141℃) solders, a direct bump-to-bump bonding technique using solder bumps, and a low temperature bonding technique using low temperature solder pads.

I. Introduction

Flip chip technology has been increasingly used due to its high packaging density, good electrical performance, and excellent reliability in many applications since it was introduced by IBM in the early sixties[1]. The conventional flip chip technique using Pb-5Sn or eutectic Pb-Sn solders requires the high temperature above 200℃ during process. The packaging of temperature-sensitive electronic systems such as liquid crystal display (LCD) and image sensor should be processed below 160℃ since the polymer materials may be degraded at high temperature[2-4]. In this paper, we introduce three kinds of flip chip bonding techniques which can be processed below 160℃. First, the low temperature alloy solders were substituted for Pb-Sn solders used in a conventional flip chip technique. Eutectic Bi-Sn (mp: 138℃) and In-Ag (mp: 141℃) were selected. Second, a direct bump-to-bump bonding technique using solder materials was developed. Next, two kinds of solder bumps were formed on the chip and the substrate and metallurgically bonded below the melting temperatures of two solders. Finally, a flip chip technique using low temperature solder pad on the substrate was developed. In this technique, a high temperature solder bump was formed on the chip, and a low temperature solder pad was formed on the substrate. The low temperature solder pad melted and wetted to the high temperature solder bump during joining process.

II. Experimental procedures

A. Conventional flip chip technique using low temperature solders

Cr(0.05 ㎛), Cu(1 ㎛), and Au(0.1 ㎛) thin films were deposited on Si wafers for under bump metallurgy (UBM) using DC magnetron sputtering system. Octagonal shaped UBMs were fabricated by photolithography and wet chemical etching. Eutectic 58wt%Bi-42wt%Sn and 97wt%In-3wt%Ag solders were evaporated on the UBM and solder bumps were patterned by lift-off process. Then, reflow process was performed in N_2 by rapid thermal annealing.

The solder bumped chip was aligned to the corresponding pads of the glass substrate and all solder joints were made simultaneously at 160℃ using a flip chip bonder. The underfill process was performed to improve the reliability of solder joints. During curing the epoxy resin at 160℃ for 5 minutes, the solder joints were reflowed again.

For the electrical test of solder joints, multi-layered metal films were deposited to form daisy chain links on SiO_2/Si wafer. The daisy chains have a total of 112 links. The electrical resistance (R_c) of samples with Bi-Sn solder joints was measured by four point probing.

B. A Direct Bump-to-bump bonding

The procedure for fabricating the solder joints with 40 ㎛ pitch is shown in Fig. 1. Au/Cu/Ti thin film was deposited for metal pads using DC magnetron sputtering on Si wafer. The rectangular-shaped metal pads of 40 ㎛ pitch were fabricated through the photolithographic process and the wet chemical etching. The solder bumps were formed on the metal pads using evaporation method and lifted off process. The dimension of the solder bumps was 25 × 50 ㎛. The In solder bumps on the test chip and Sn solder bumps on the glass substrate were formed. Flux was dispensed on the surface of each bump and then the solder bumps on the chip were aligned to the corresponding solder bumps of glass substrate using flip chip bonder at 125℃ for 1 min and all solder bumps were jointed simultaneously. The load of 2 N per chip was applied during the bonding. Since the test chip and glass substrate had 676 bumps, the load per bump was 3 mN.

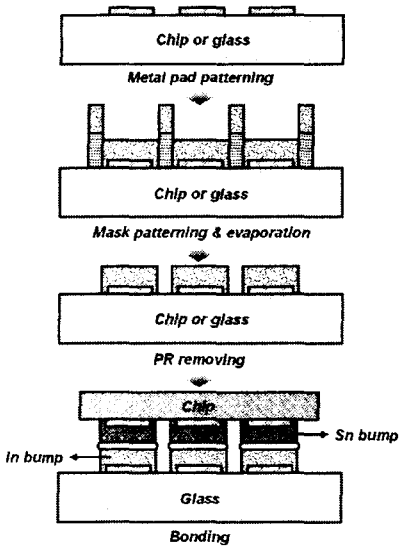

Fig. 1. Schematic view of solder joint formation.

C. Bonding using low temperature solder pads

An UBMs used in this experiment is Au/Ni/Cu with a diameter of 380 ㎛ on PCB. Sn-4.0wt%Ag-0.5wt%Cu solder balls of 350 ㎛ or 475 ㎛ diameters were attached on UBM and reflowed at 260℃ for 90 sec in the convection oven. 52wt%In-48wt%Sn solder pad was deposited on Cu/Ti/Si substrate using thermal evaporation. Sn-4.0Ag-0.5Cu solder bumps were aligned to the 52wt%In-48wt%Sn solder pad and joined at 140℃ for 10 min under 12 mN/bump on hot plate.

III. Results and Discussion

A. Conventional flip chip technique using low temperature solders

In Fig. 2, eutectic Bi-Sn and In-Ag solder bumps with two different pitches are shown after the reflow at 160℃. The bumps are uniform and smooth. The height and diameter of Bi-Sn solder bumps are about 40 ㎛ and 46 ㎛ in the 80 ㎛ pitch arrays, while they are about 24 ㎛ and 27 ㎛ in the 50 ㎛ pitch arrays.

The solder bumps of the test chip were aligned to the metal pads of the glass substrate and then heated to 160°C for joining. A no-clean type flux was applied prior to the joining. Figure 3 shows a cross-sectional SEM micrograph of a 50 ㎛ pitch Bi-Sn solder joint assembled at 160° C. The spherical-shaped solder joint was successfully connected to the metallization between Si and glass substrate. This demonstrates that ultra-fine interconnections with pitches of 50 ㎛ can easily be formed using this technique due to the self-alignment characteristic of the joints due to the surface tension of liquid solder.

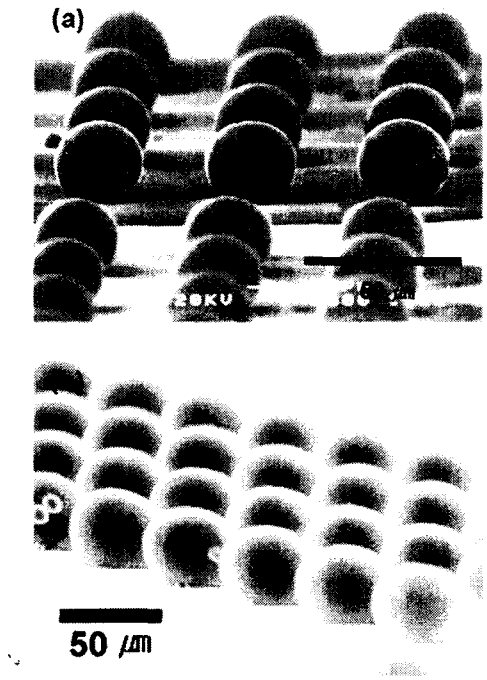

Fig. 2. SEM images of solder bump arrays; (a) eutectic Bi-Sn and (b) eutectic In-Ag.

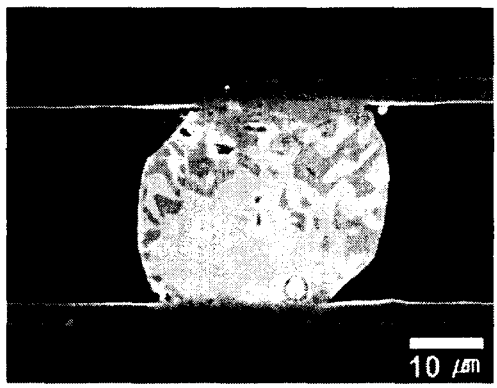

Fig. 3. Cross-sectional SEM images of eutectic Bi-Sn solder joint.

Table I lists the average contact resistances (R_c) per link of daisy chain. The metallization of chip and substrate was Au/Cu/Ti. These measured values include the contact resistance of one solder joint and a conductor line. The contact resistance of Bi-Sn solder joint increased with the decrease of the solder size while that of In-Ag solder joint little changed.

Calculating the resistances of conductor lines on substrate and subtracting them from measured R_c, the corrected contact resistances of Bi-Sn and In-Ag solder joints are from 13.9 to 39.3 mΩ.

Table II shows the R_cs before and after the underfill process. The solder joints were additionally reflowed at 160℃ for 15 minutes because the epoxy resin required a curing. After this process, the contact resistance of the Bi-Sn solder joint slightly increased while that of the In-Ag solder joint decreased from the initial value. The R_cs of the In-Ag solder joints with underfill have been measured after a temperature cycling test (-55℃-125℃ with a cycle duration of 30 min). The results are shown in Table. III. The R_c of the In-Ag solder joint with underfill remained almost completely unchanged.

In the conventional flip chip technique using low temperature solder bumps, the growth of intermetallic compounds can be a serious problem because the extensive reaction of the liquid solder with the UBM occurs.

Table I. Contact resistances of solder joints before underfill process.

Solder	Pitch (㎛)	Measured R_c (mΩ)	Standard deviation (mΩ)	Corrected R_c (mΩ)
Bi-Sn	80	18.6	3.0	13.9
	50	46.8	2.8	39.3
In-Ag	50	24.4	1.6	14.8
	50	28.2	1.0	16.4

Table II. Contact resistances of solder joints before and after underfill process.

Solder	Underfill	R_c (mΩ)	Standard deviation (mΩ)
80 ㎛ pitch Bi-Sn	no	19.5	4.1
	yes	23.4	6.7
80 ㎛ pitch In-Ag	no	24.4	1.6
	yes	21.1	1.8

Table III. Contact resistances of 80 ㎛ pitch In-Ag solder joints after the temperature cycling.

Temperature cycling	R_c (mΩ)	Standard deviation (mΩ)
before	22.6	0.7
1018 cycles	22.7	0.8

B. A Direct Bump-to-bump bonding

When the In and Sn solder are in contact together, the interdiffusion occurs between two solders. As shown in Fig. 4, the melting temperature of In-Sn alloy decreases from that of each solder due to intermixing. Therefore, the In-Sn solder joint may melt partially in the interface and bond at the lower temperature than the melting temperature of either In (157℃) or Sn (232℃).

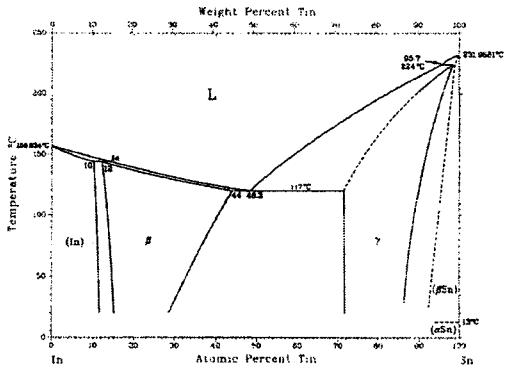

Fig. 4. In-Sn phase diagram[5].

Figure 5 is the SEM images showing the metal pads and the In bumps formed on the metal pads of 40 ㎛ pitch uniformly. The 20 × 45 ㎛ rectanglar-shaped metal pads were used, which were slightly smaller than those of solder bumps to cover solder bumps entirely. The solder bumps were successfully fabricated using evaporation method and lifted off process and the average height of the solder bumps was 10 ㎛.

Figure 6 is the SEM image of the cross-sectional In/Sn solder joints. This image demonstrates the solder bumps with 40 ㎛ pitch were successfully connected at the bonding pressure as low as 3 mN per bump.

The electrical assessment is done using four-point probing technique to address the electrical resistance of the daisy chain running through the chip and the glass substrate with 204 bumps. The average of contact resistance per solder joint was 65 mΩ.

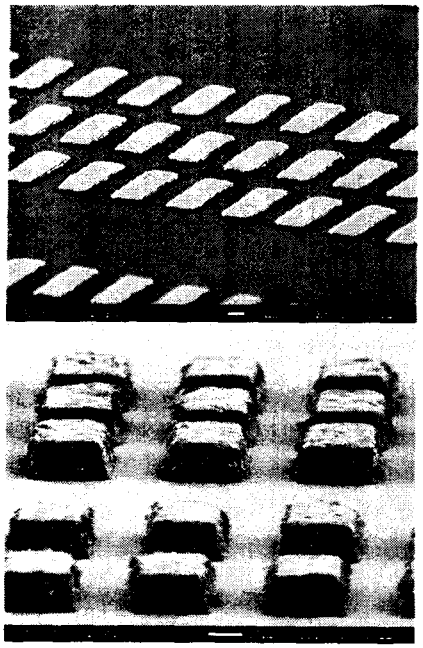

Fig. 5. SEM images showing (a) the metal pads and (b) the In solder bumps.

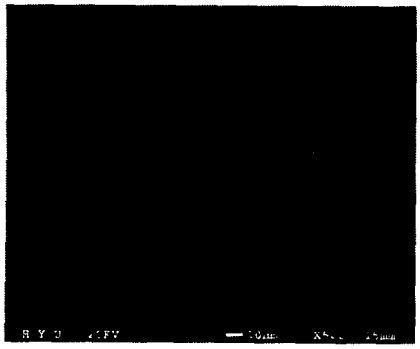

Fig. 6. Cross-sectional SEM image of 40 ㎛ pitch In/Sn solder joint.

C. Bonding using low temperature solder pads

Figure 7 shows a optical microscopy showing the cross-section of Sn-Ag-Cu solder ball bonded on In-Sn solder layer after reflow. As shown in Fig. 7, the low temperature solder wetted to the high termperature solder and the mixed layer was observed between the Sn-Ag-Cu solder and In-48Sn solder layer. The cross-section image of the solder joint after aging at room temperature for 76 days is shown in Fig. 8. It was found that the low temperature solder was diffused to the Sn-Ag-Cu solder bump. It is expected that the composition of low temperature solder changed because the interdiffusion of solder components. This technique proved to be a very promising method for the low temperature bonding.

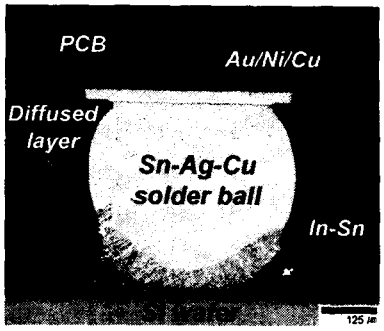

Fig. 7. Cross-sectional optical microscopy of Sn-Ag-Cu/In-Sn solder joint.

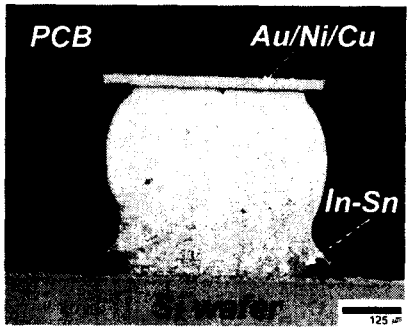

Fig. 8. Cross-sectional optical microscopy of Sn-Ag-Cu/In-Sn solder joint after aging at room temperature for 76 days.

IV. Summary

We developed the various low temperature flip chip bonding techniques; a conventional flip chip technique using eutectic Bi-Sn (mp: 138℃) or eutectic In-Ag (mp: 141℃) solders, a direct bump-to-bump bonding technique using solder bumps, and a low temperature bonding technique using low temperature solder pad. It is believed that these flip chip techniques can be used to the package of the temperature-sensitive systems such as LCD and image sensor.

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