Unique New Packaging Technology of Semiconductor by High Performance Encapsulation Expoxy Resin and VPES (Vacuum Printing Encapusulation Systems)

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(Sanyu Rec Co., Ltd. / Korea)

Unique New packaging of Semiconductor Packaging Technology High performance by Encapsulation Epoxy Resin and VPES(Vacuum Printing Encapsulation Systems)

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1. Process of PES and VPES

2. Comparing with Conventional Technology

3. Component technologies of PES and VPES
3-1. Special Stencil
3-2. Equipment
3-3. Liquid Encapsulation Resin

4. Applications of PES and VPES

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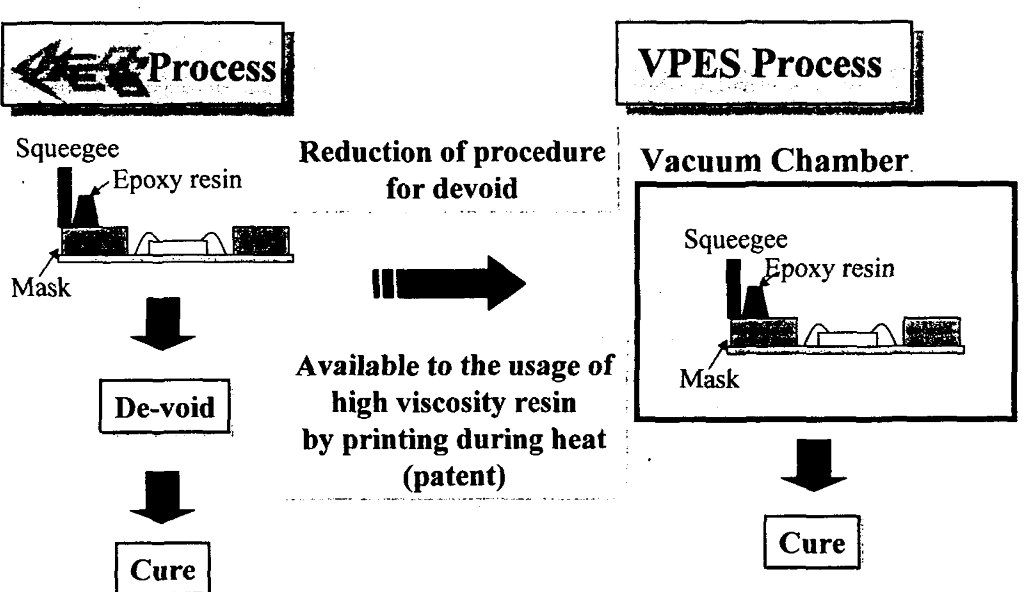
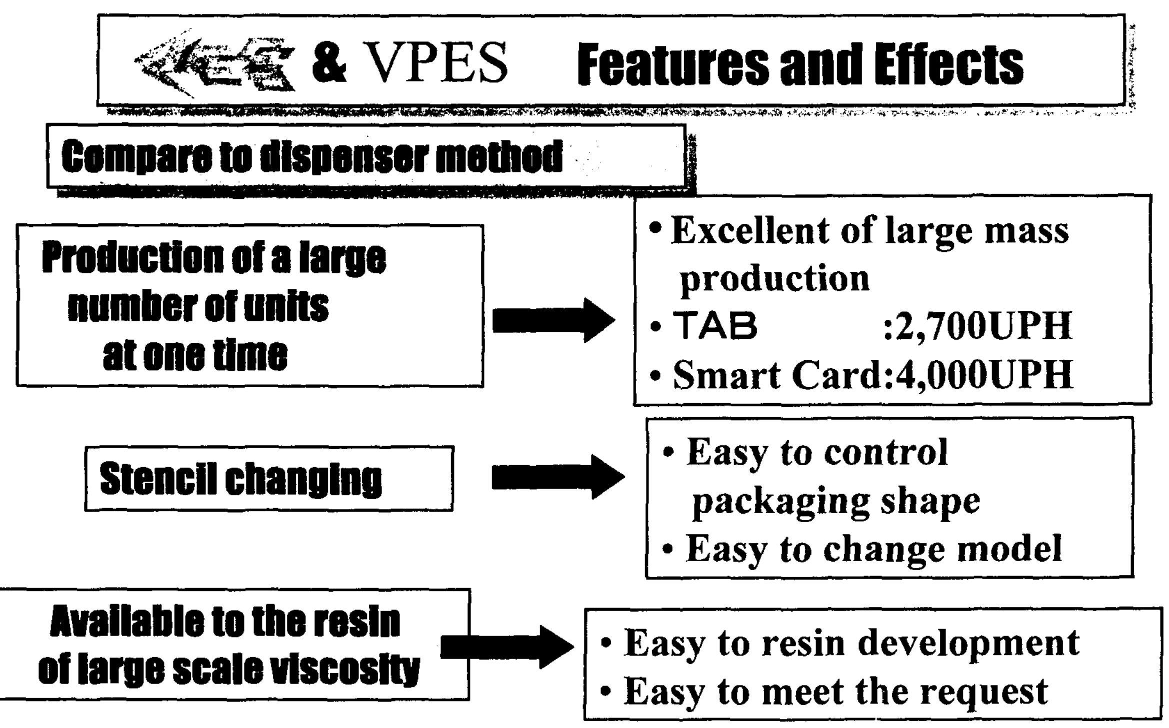
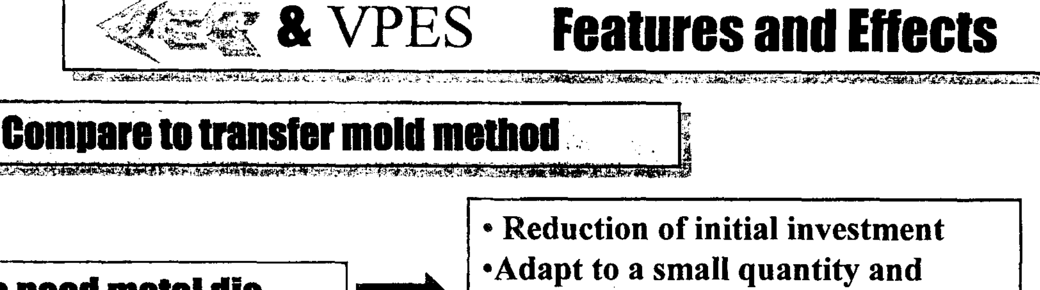
Process Comparison of & VPES







No need metal die →

- Reduction of initial investment
- Adapt to a small quantity and a large number types
- Short delivery time

No need heat and pressure process →

- Without restriction of interposer
- Low cost

Low resin loss →

- Low cost
- Without environment problem

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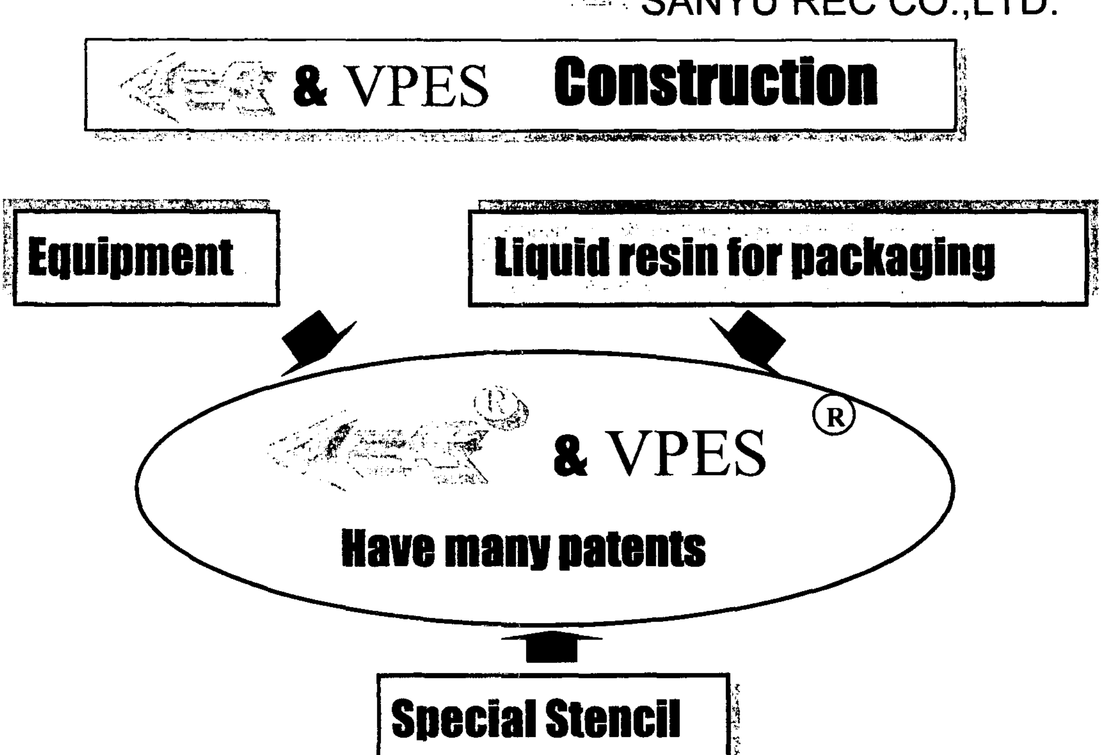
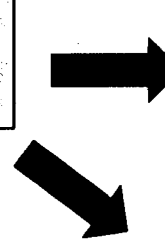


& VPES **Special Stencil**

Special structure (Our patents)



Continuous printing
No need the sweeping bottom of Stencil

Easy control of packaging shape

Easy control of packaging thickness
Getting smooth surface

Off-Contact Construction

Heated printing

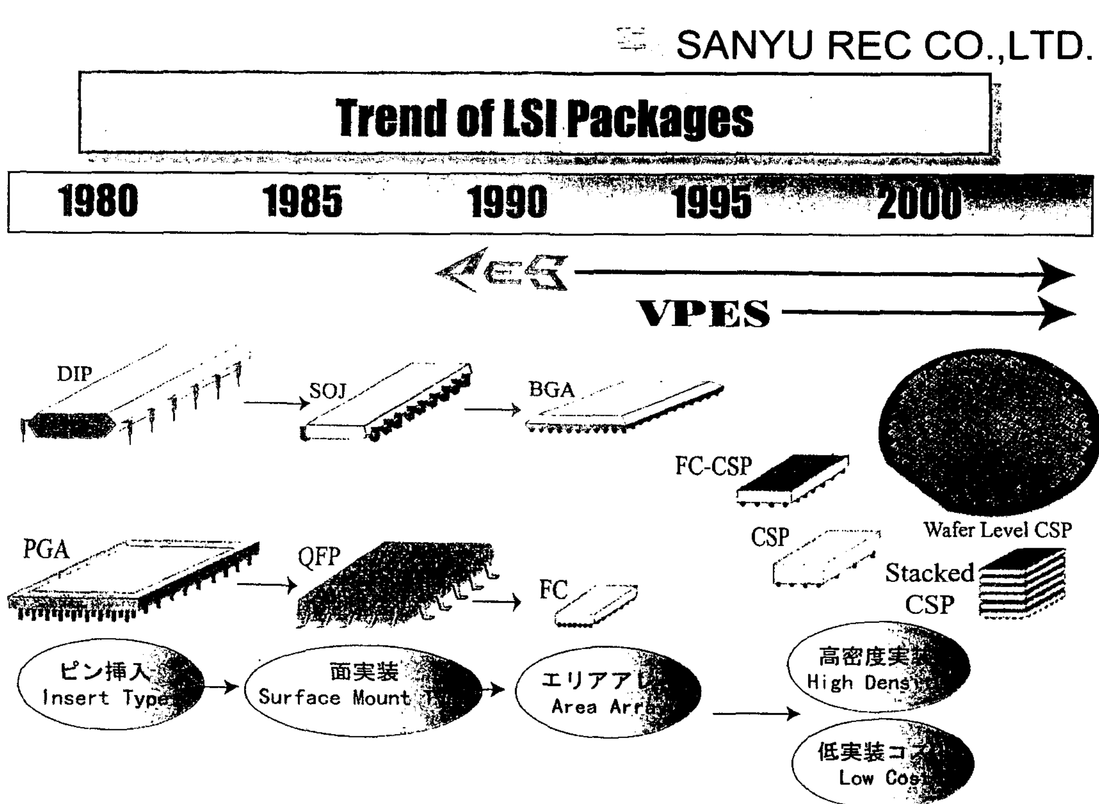
Available in all kinds of packaging

Vacuum printing

Loading System

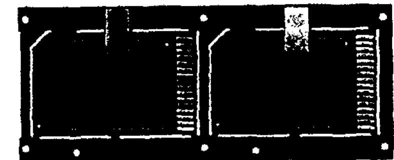
& VPES Liquid resin for packaging

NPR-100 series	General grade	COB、Smart Card etc.
NRT series NUV series	Quick cure High adhesion UV cure style	TAB、thin thickness packaging etc. Smart Card etc.
NPR-700 series	Low warpage High reliability	BGA、CSP、MCM etc.
ES series	Low warpage For ceramic	BGA、CSP、MCM etc. Module for ceramic board
NF series	High underfill	Flip Chip underfill
NLD series	High transparent	LED、others

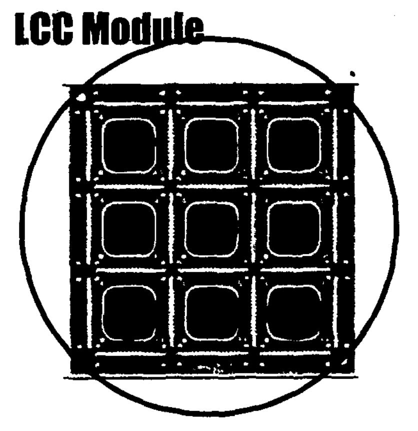


LCD Driver Module

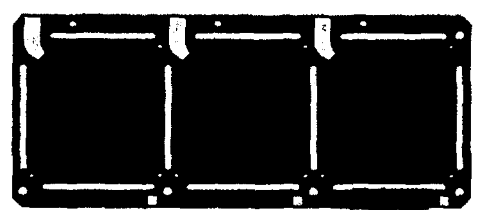
SD Card Module



LCC Module



P-BGA



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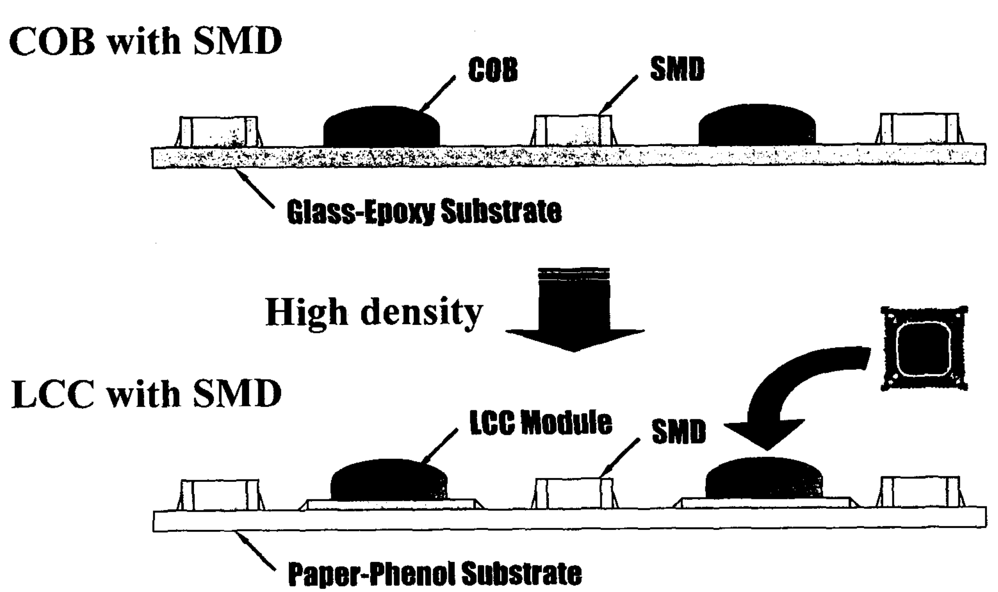
Used for LCC assembling



Merit for LCC assembling

1. Suitable for SMT and reflow soldering with SMD at onetime

2. Failure IC can be repair after inspection

   ⇨ Reduction of percent defective

3. Paper phenol substrate can be used for mother board

   ⇨ Reduction of total cost

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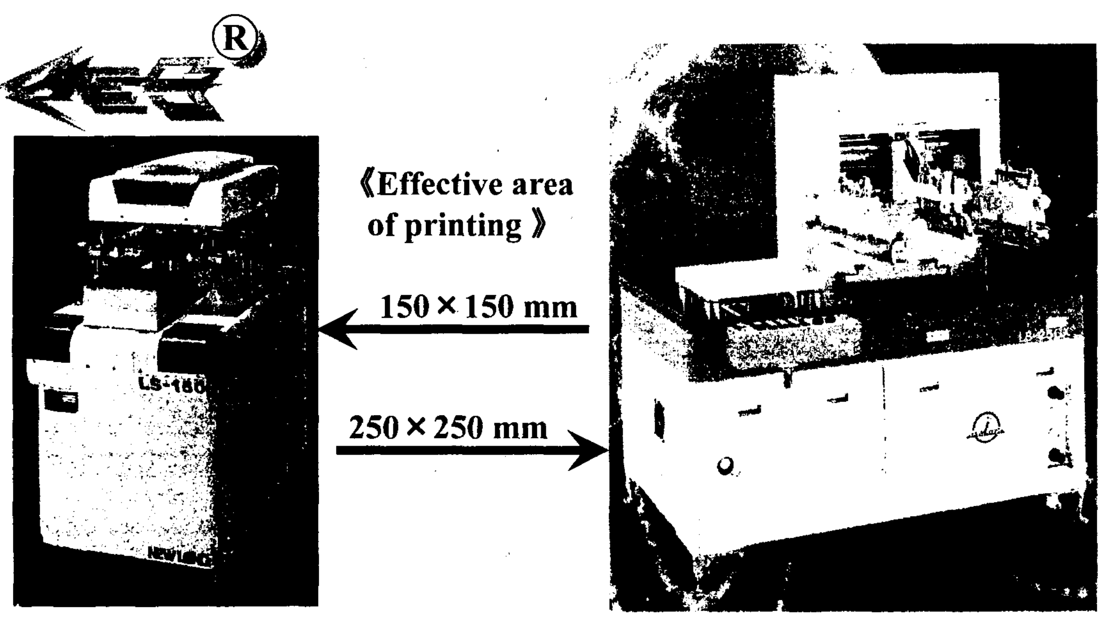
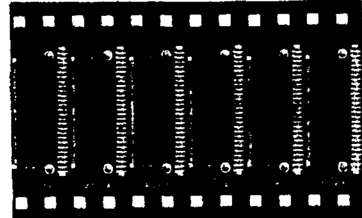
Table type LS-20GX-B type

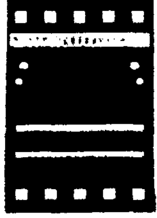
Semi-auto Printing Encapsulation System (Standard)

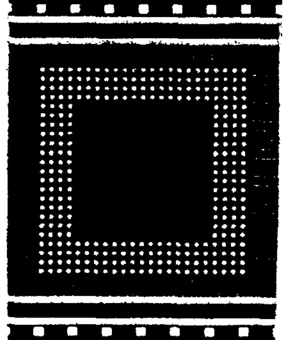


LCD Driver

T-BGA







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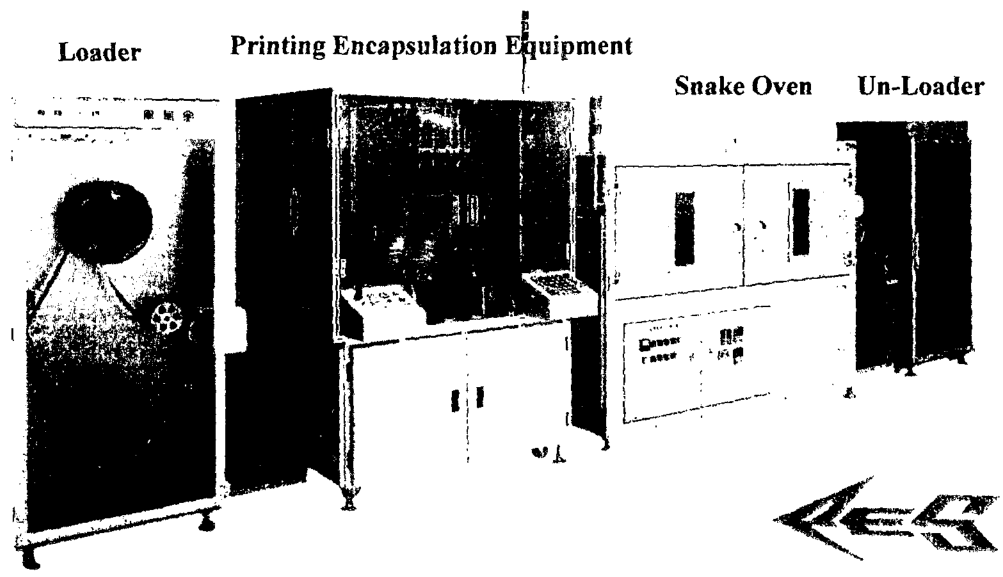

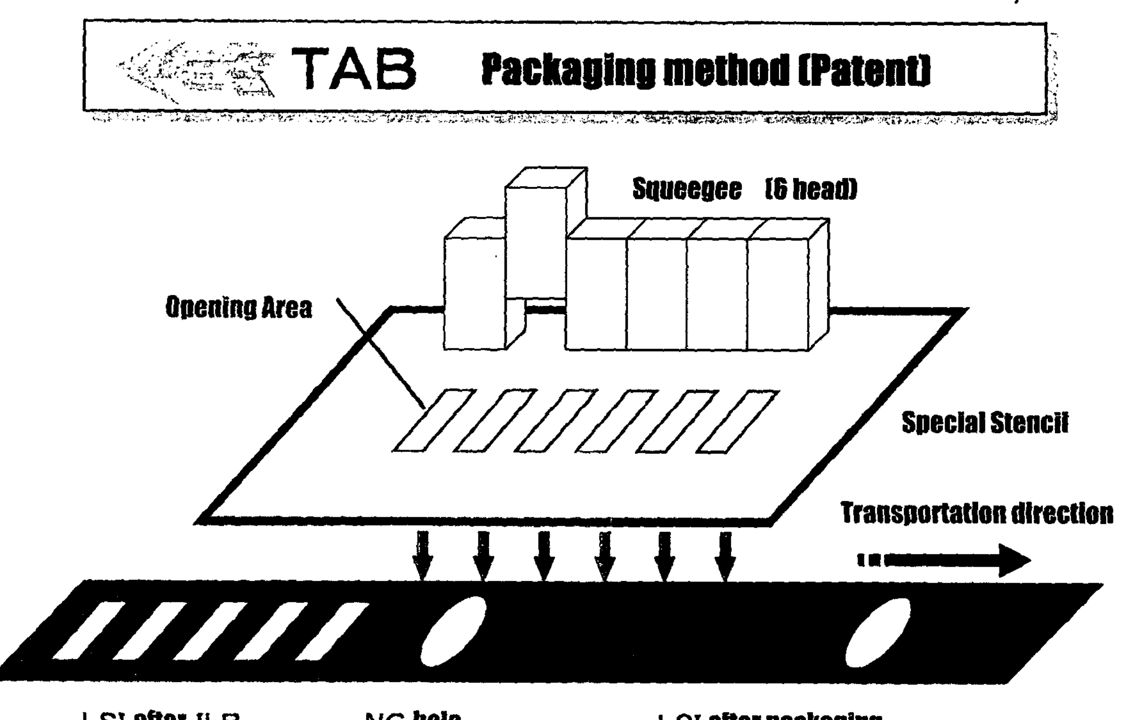

Presupposition

Capacity	6IC/7S	(transportation 2.5 S + Printing 4.5 S)
Operation time	30days × 24h/month	

Productivity ≒

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Product	NRT-930 Series	Remark
Advantage	Snap Curing Type	
Viscosity	50 Pa.s	B type (23℃)
TI	1.0	2rpm./20rpm.
Gelation Time	30 sec.	150℃
Curing Condition	120℃/10 min. + 150℃/1.5 hr.	
Pot Life	3 month	At 5℃
Tg	100℃	TMA
Hardness	> 80	Rockwell M
CTE	33 ppm	TMA
Modulus	900 kg/mm²	JIS K6911
Strength	> 200 g/cm	For Upilex

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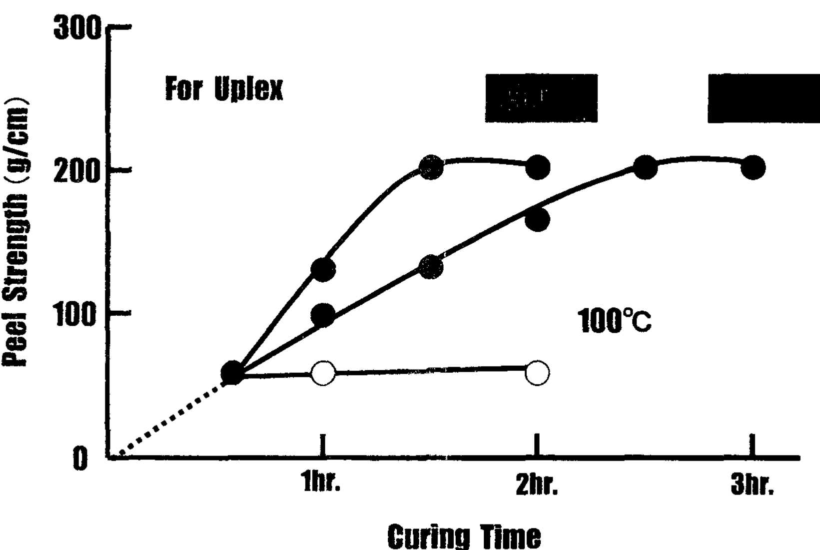
NRT-930 Peel Strength



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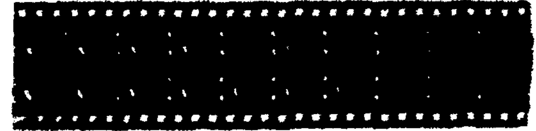
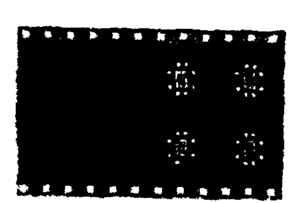
TAB Reliability Test Result

Item	A	B	C
Mechanical Strength	Pass	Pass	Pass
Temp. Cycle	-65℃∞150℃ 500cycle	-40℃∞125℃ 300cycle	-50℃∞150℃ 200cycle
TB	125℃/1000hr.		
THB	85℃-85%RH 1000hr.	85℃-85%RH 1000hr.	85℃-85%RH 1000hr.
USPBT			131℃-2atm 40hr.
PCT	125℃-100%RH 96hr.	125℃-2atm. 300hr.	125℃-2atm. 100hr.

Smart Card Module





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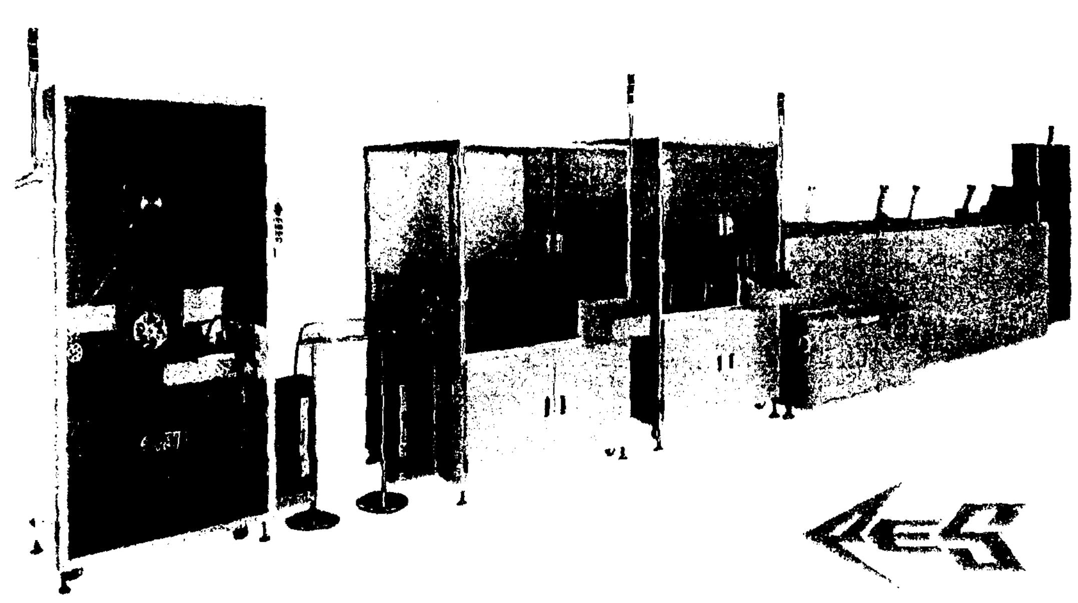
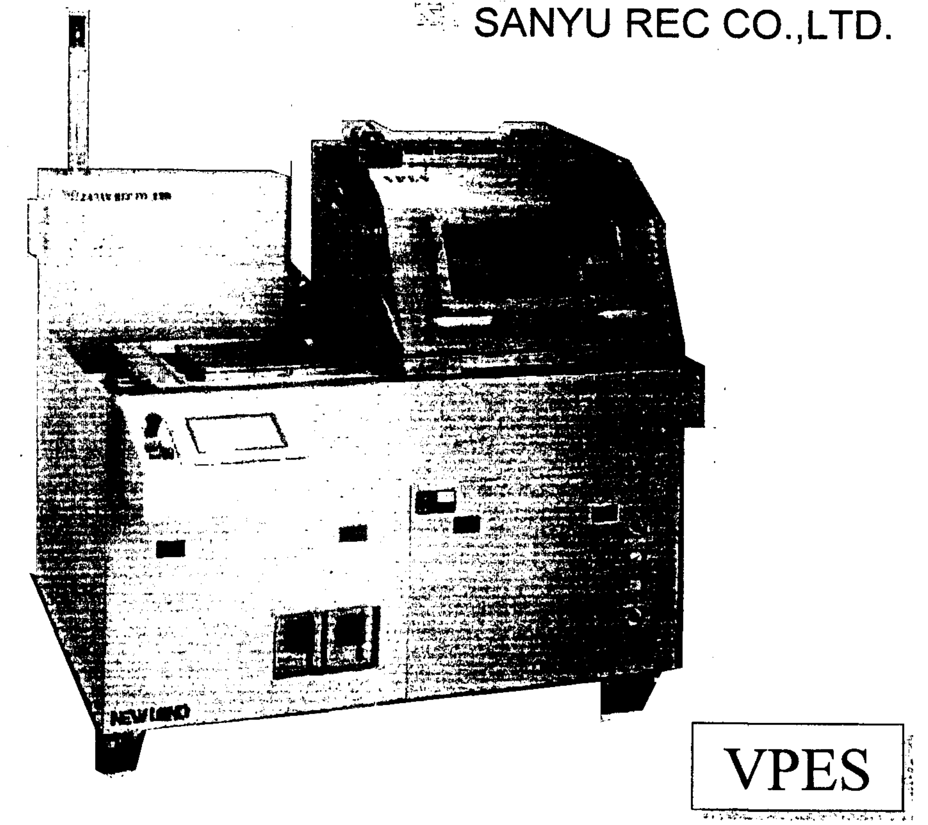


Smart Card PES Line



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Full Auto
VPES®

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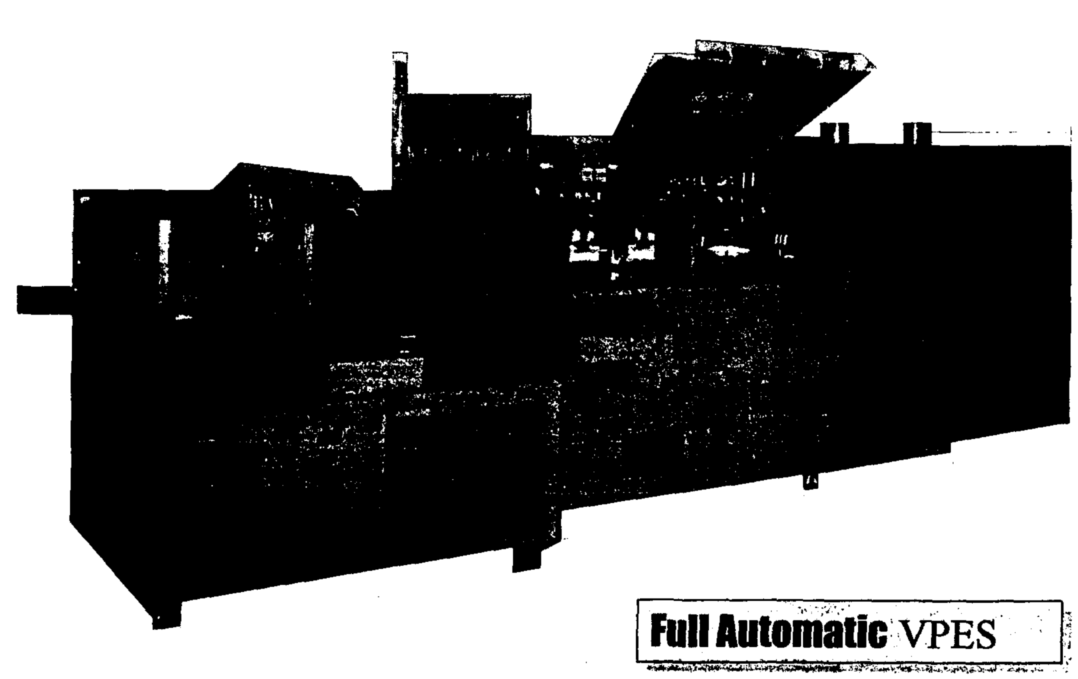

Full Automatic VPES

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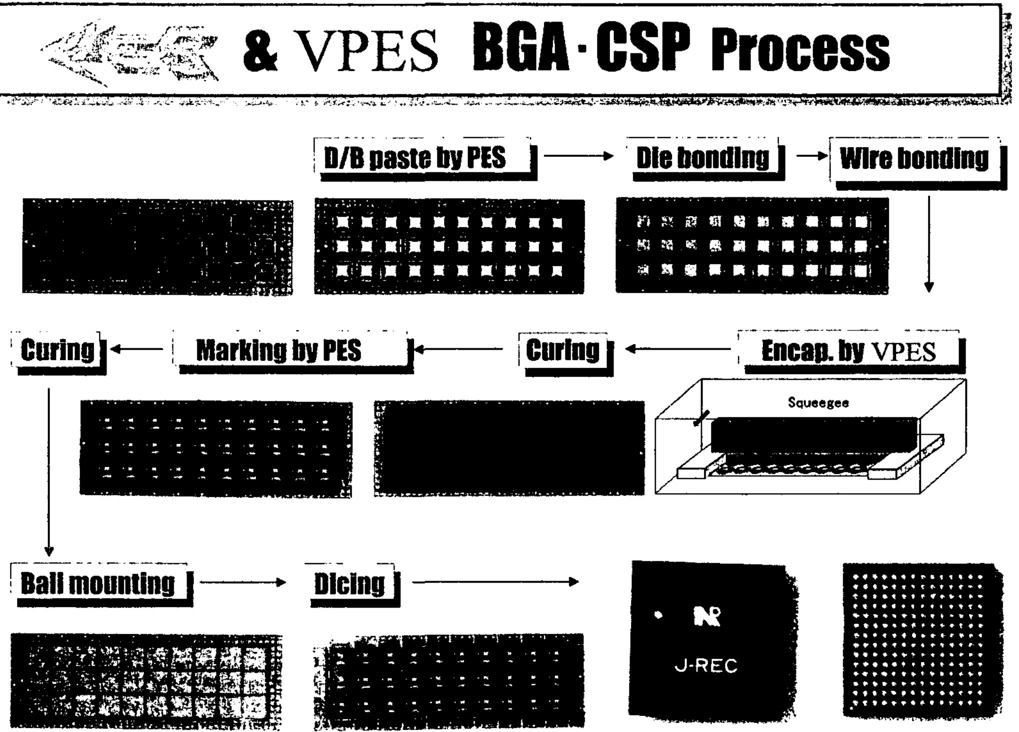
Encapsulation Resin for CSP

Advantage	Low CTE	Low Modulus	Remark
Product	NPR-700 series	ES series	Low Warpage
Viscosity	700 Pa.s	240 Pa.s	B type (23 ℃)
TI	1.0	1.2	2 rpm./20 rpm.
Curing Condition	100 ℃/1 hr. + 150 ℃/3 hr.		
Tg	105 ℃	130 ℃	TMA
Shear Strength	>100 kg/cm²		Al Al
Hardness	>100	>80	Rockwell M
Water Absorption	0.9 %	0.5 %	PCT 2 atm./100 hr.
CTE	10 ppm	25 ppm	TMA
Modulus	2300 kg/mm²	300 kg/mm²	JIS K6911
Ionic Impurity (Cl)	<1 ppm		100 ℃/20 hr.



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VPES BGA Package Reliability Test Result

Test Item		Result
Wire Damage X-Ray		0/20
Voiding C-SAM Through scan		0/50
Peel test SPS intemal. Hand peel encap		0%
Moisture sensitivity	JEDEC A-112 Level1	18/22
	JEDEC A-112 Level2	0/22

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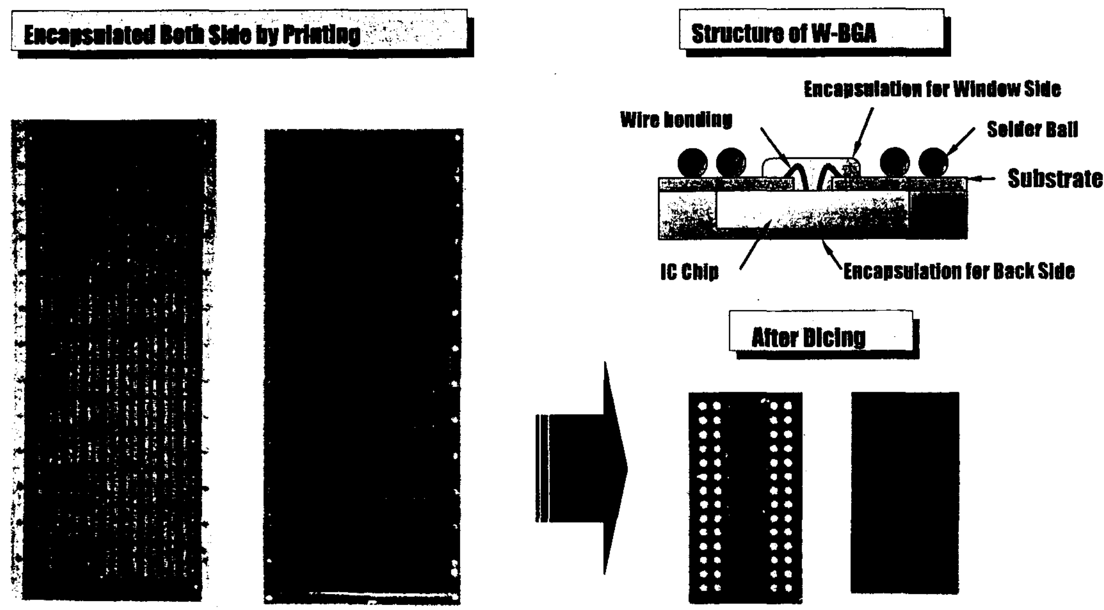
& VPES W-BGA Process



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VPES DRAM Package Reliability Test Result

(JEDEC STD Test Method A113-B)

Eiectrical DC Functional test

↓

Bake@125℃,24hr

↓

Pre-conditioning LevelⅢ
30℃/60%RH/192hr

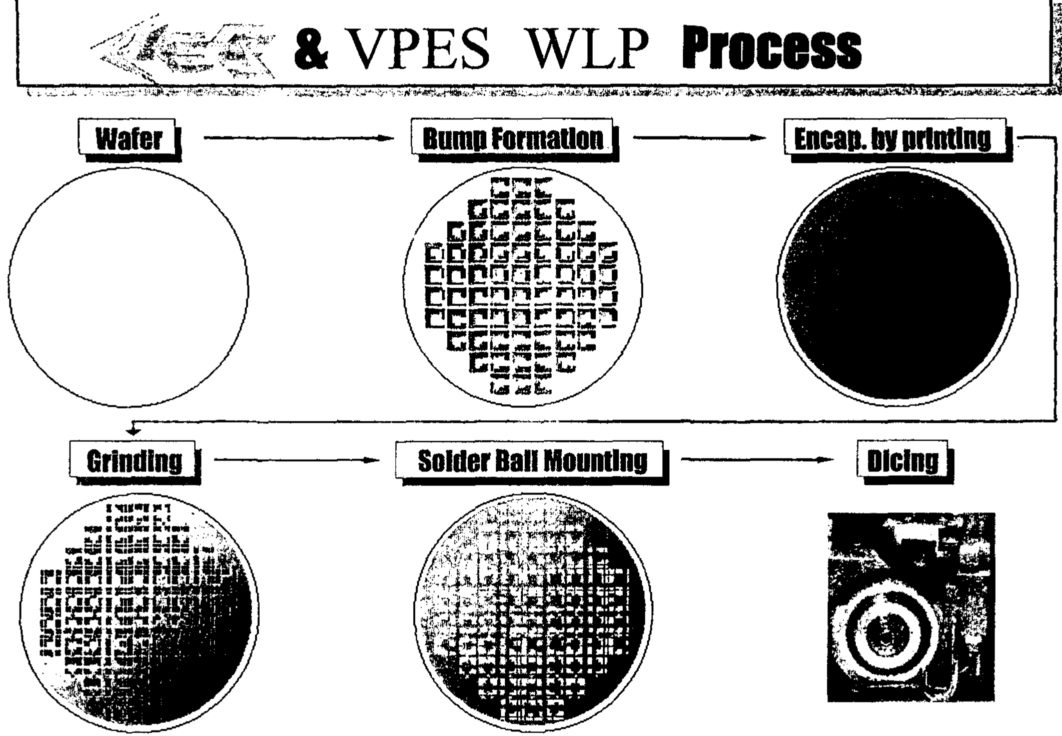
↓

Reflow@220℃ 4times

↓

Eiectrical DC Functional test

Test Item	Result
PCT 121℃/100%RH/2atm /168hr JEDEC A102-B,Cond.D	Pass
Heat cycle test -55℃to125℃(air to air) 500cycle JEDEC A104-A,Cond.B	Pass
Thermal shock test -55℃to125℃(liq to liq) 500cycle JEDEC A106-A,Cond.C	Pass
High temp storage test 150℃/ 500hr JEDEC A103-A	Pass



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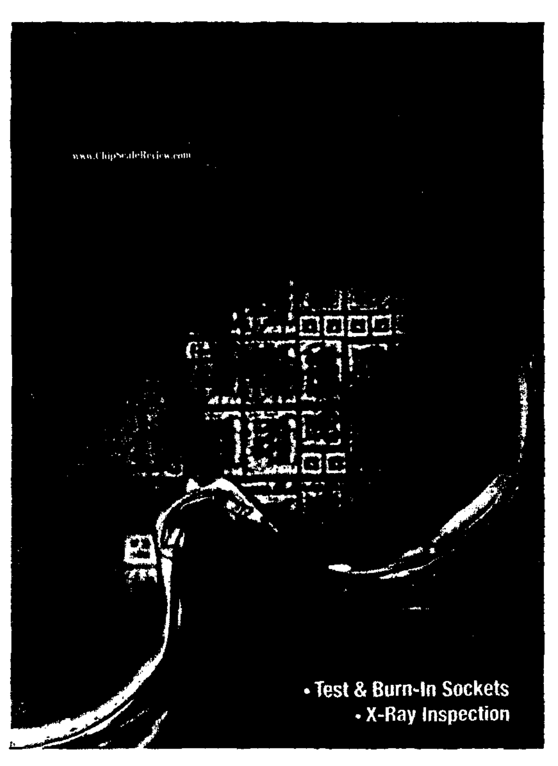

A Critical Review of the Top CSP Patents

By David Francis and Linda Jardine, Contributing Editors

Last year, the U.S. Patent Office issued about 350 patents that could be classified as either ball grid array, chip scale or wafer level. After a careful review, we believe the 10 that follow were among the best.

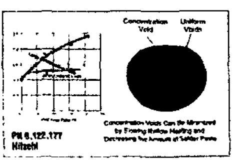

Figure 1. The effect of void size on solder joint strain

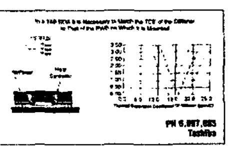

Figure 2. Selecting stiffener TCE to minimize solder strain

How did we determine which patents out of 350 were best? Our selection was largely subjective based on our experience and our knowledge of the literature and the industry. The primary reason for the selection of each patent, however, is indicated at the front of that patent. The patents are presented in no special order.

1. Understanding the Causes of Voids in Solder Joints

This patent (Figure 1) was selected because it discusses a general problem that can be encountered by anyone in this industry, and because it indicates how the effect can be reduced or eliminated. The package manufacturer can make a package with perfect joints yet this same package can fail prematurely due to poor assembly practices.

A standard way of joining solder bumped devices to PWBs is to screen-print solder paste on the pads, place the device and reflow it. When heated, the flux in the solder paste volatilizes forming bubbles that escape mostly into the atmosphere.

Some of these bubbles, however, remain in the molten solder. Since these bubbles weigh less than the solder, they tend to move up through the molten solder and collect in the region where the solder is bonded to the package substrate or chip.

If the solder does not adhere well to the substrate or chip pad, these small bubbles can collect and create a large void.

In this patent, the company studied the effect of these voids on solder joint strain. The results are shown in the accompanying graph. Researchers found that small uniform voids have little impact on strain for modest amounts of void area. As shown in the accompanying chart, a void area as large as 15-20% of the total solder area had about the same strain as a 2% void area. The strain produced by large concentration voids increased at a much faster rate.

The solution provided in this patent was to prevent the formation of concentration voids by first decreasing the heating rate for reflow soldering, which allows more time for the flux vapors to escape, and then decreasing the amount of solder paste to the minimum needed for a good bond.

2. Understanding the Role of the Stiffener Used in a TAB Ball Grid Array Package

We selected this patent (Figure 2), again, because it addresses a specific industry problem, it was well investigated and the solution was clearly presented.

It is also an example of how the package designer must understand where and how the packages are to be used to properly select the correct materials.

To be able to handle the TAB BGA throughout its processing, a stiffener plate is usually attached to the TAB frame or vice versa. This stiffener can be made of a laminate or metal, and it is chosen

Last year, the U.S. Patent Office issued about 350 patents that could be classified as either ball grid array, chip scale or wafer level. After a careful review, we believe the 10 that follow were among the best.

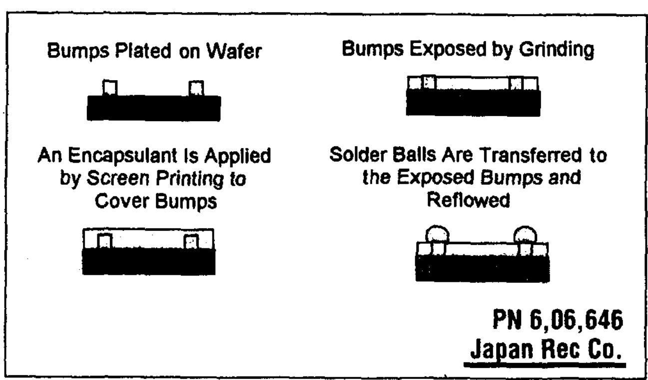

Figure 5. Wafer-scale package using double bumps

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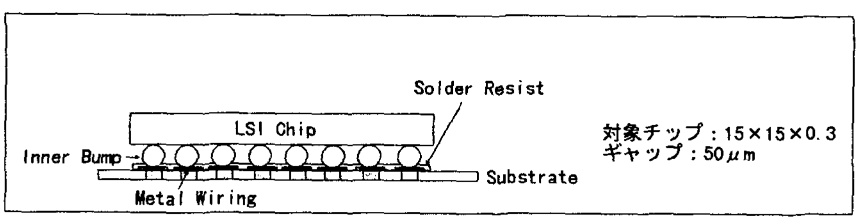
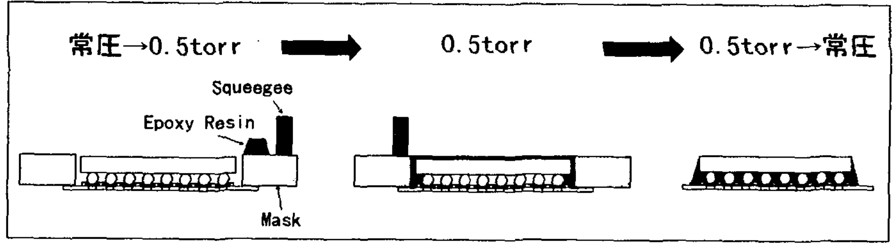
VPES Flip Chip **Process**





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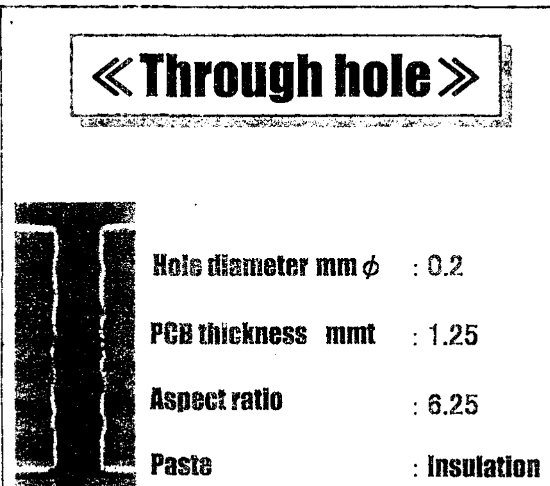
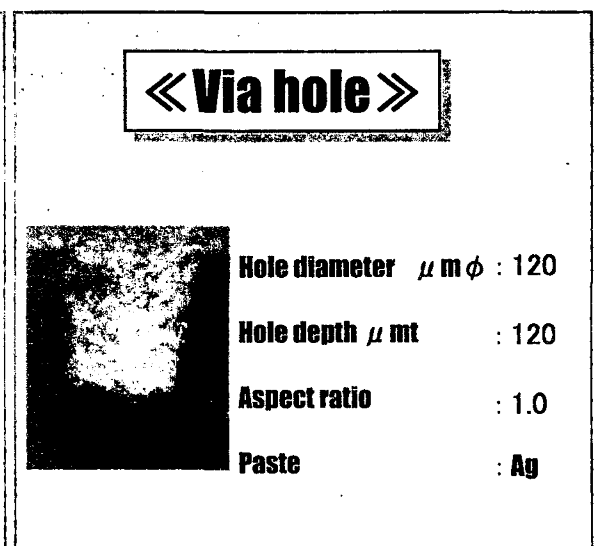
Fill in through hole by VPES





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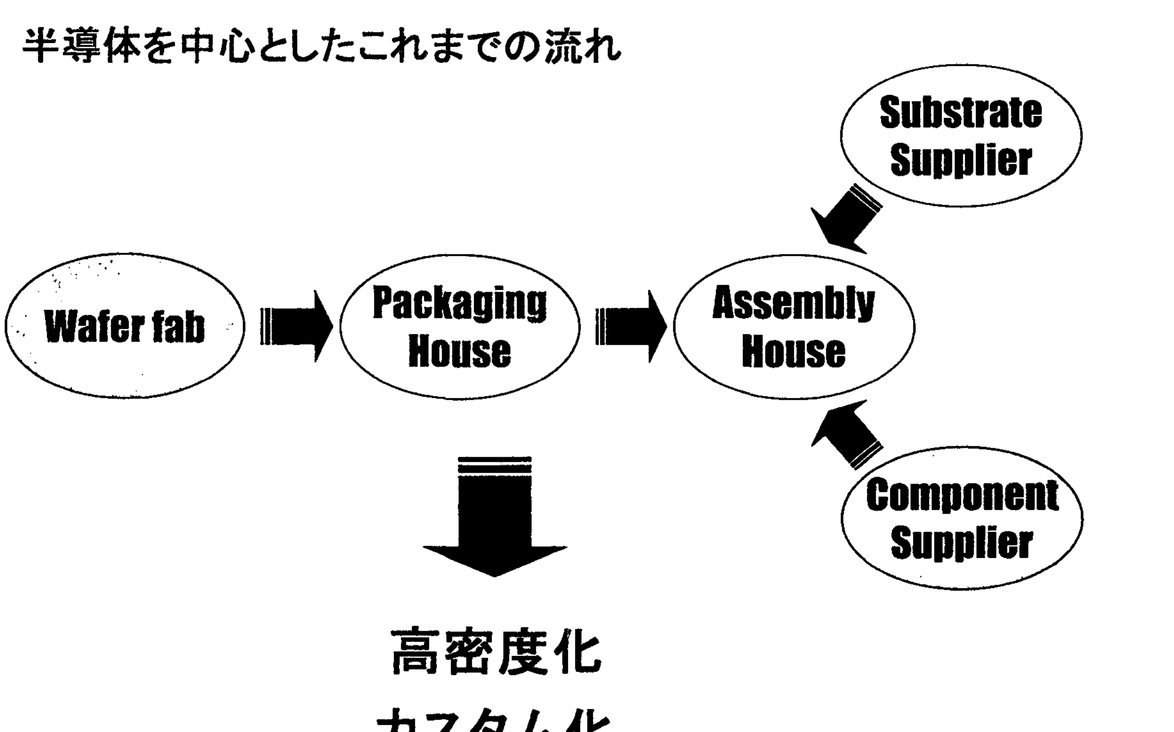
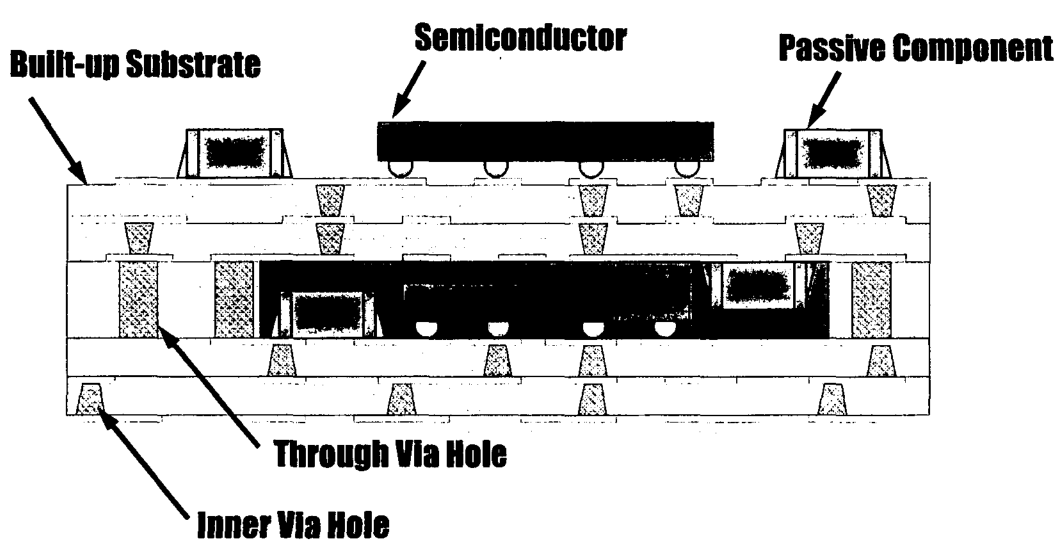


SIP (System in Package) への流れ



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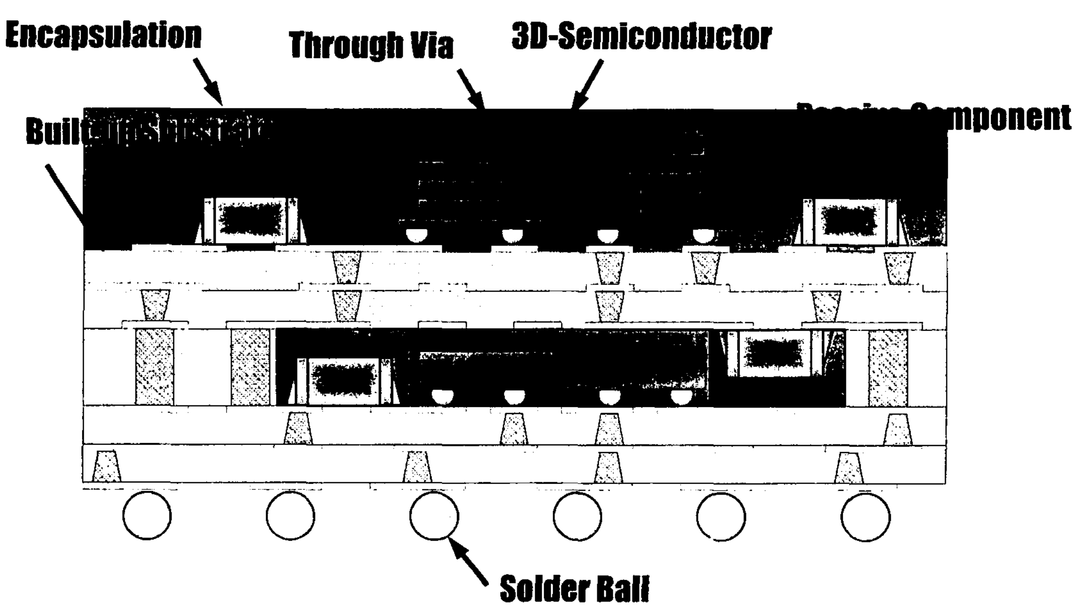
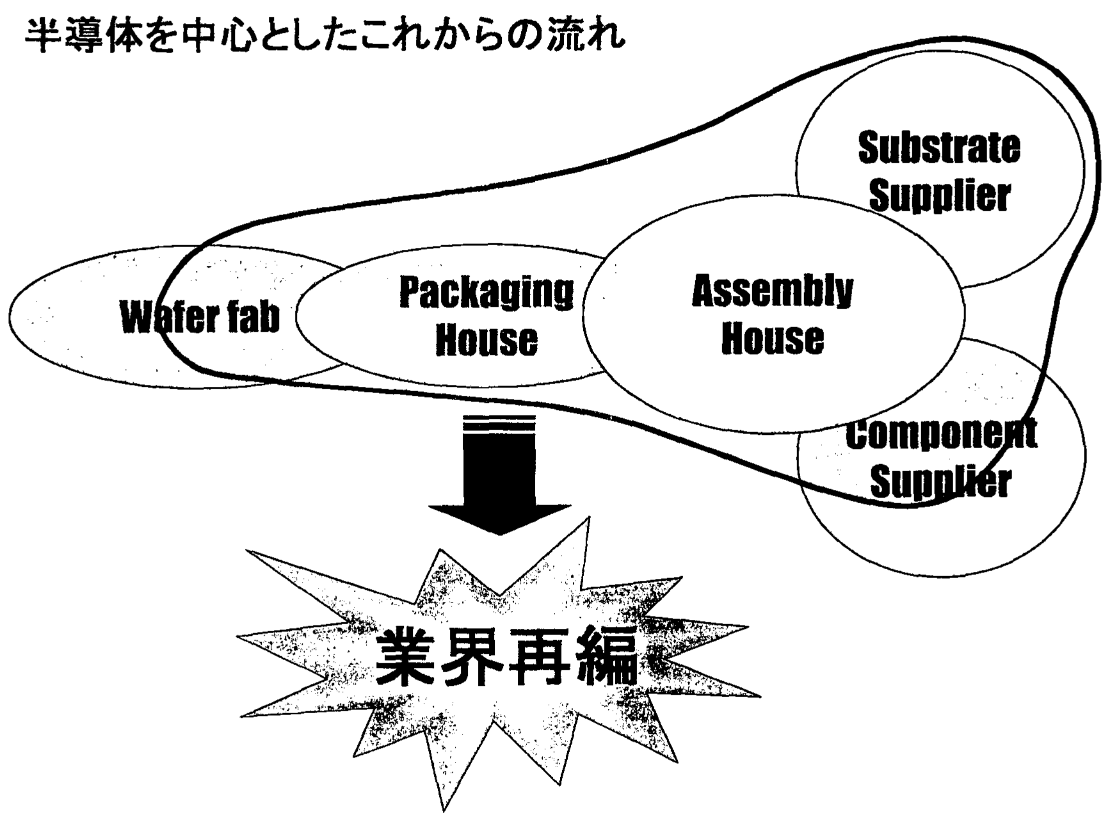
3DP (Cube Package) への流れ



半導体を中心としたこれからの流れ



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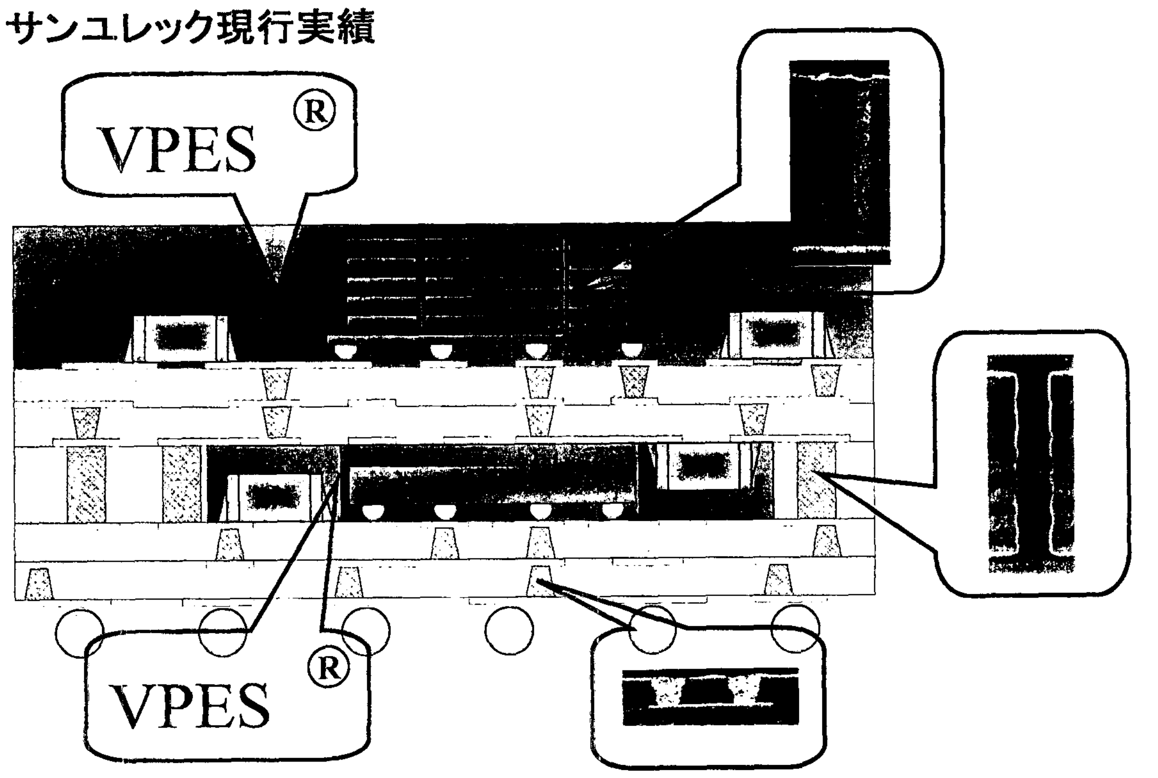
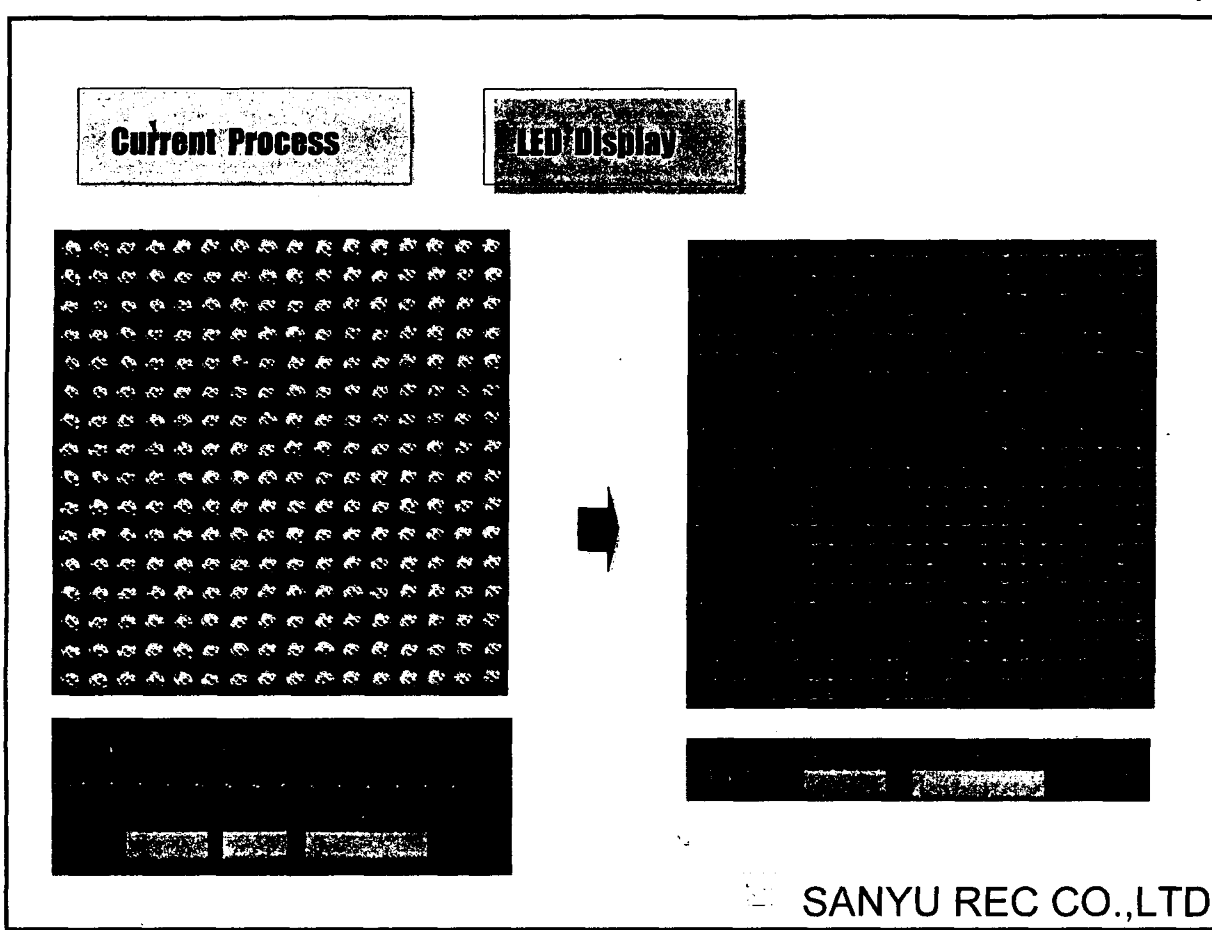
サンユレック現行実績





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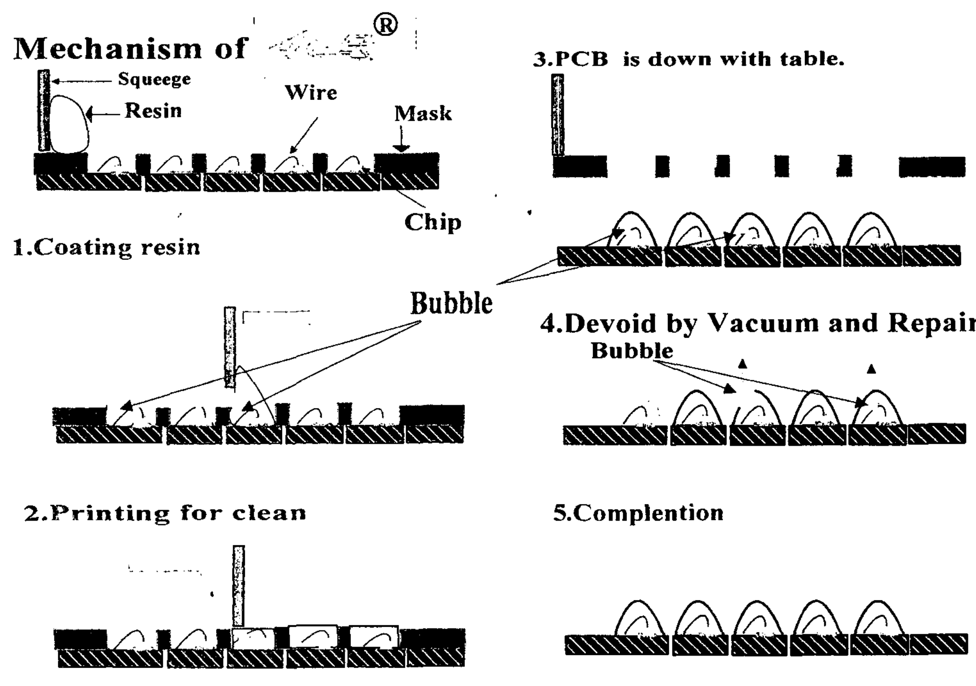
& VPES LED Process

Comparison of LED dot matrix display between conventional method and & VPES	LED lamp ① Lead insert ② Solder joint	LED COB Squeegee Resin Mask
Display size	96 mm□	96 mm□
Display thickness	31 mm	12 mm
Display weight	160 g	80 g
Dot number	256 dot	576 dot
Viewing angle	70 °	160 °



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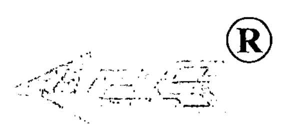
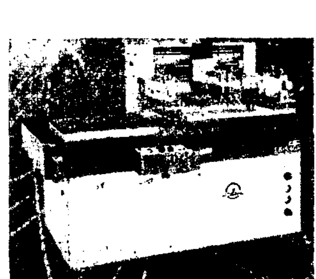
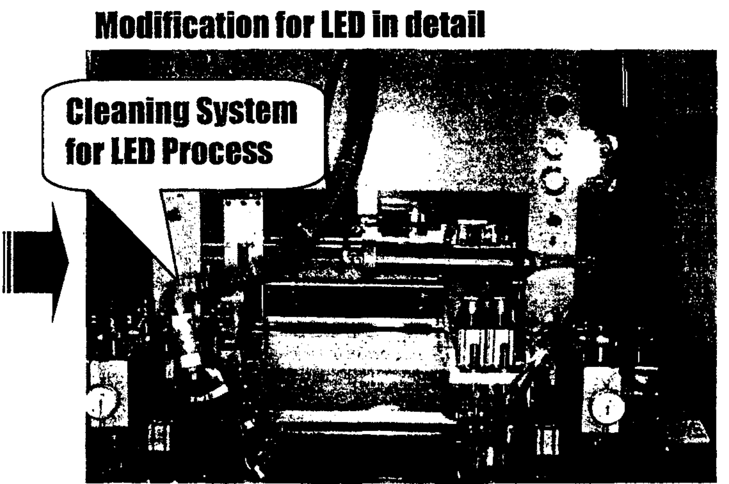


Semi-automatic type Printer for PES

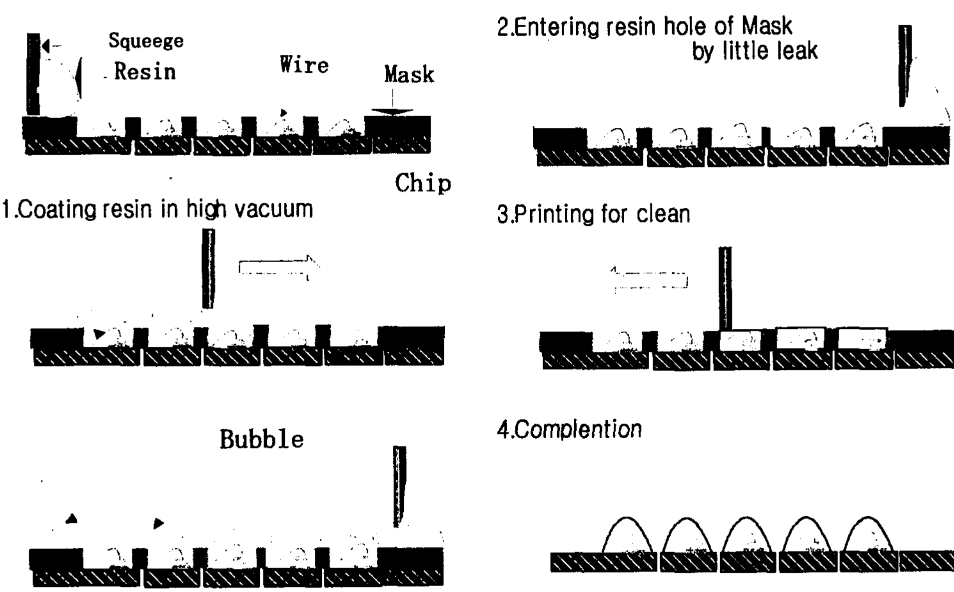
LS-34GX-PES



Modification for LED in detail



Mechanism of VPES®



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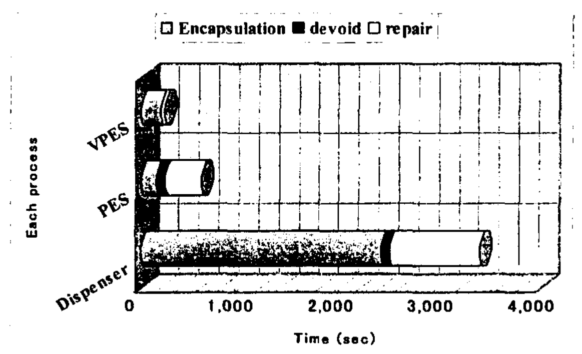
工法別封止作業時間比較（顧客データ）

※直径3mmピッチ幅4mmドット数16×16ドットマトリックスタイプの場合

	ﾃﾞｨｽﾍﾟﾝｻｰ法	PES	VPES
樹脂封止	2,400.0(S)	150.0(S)	200.0(S)
脱泡	90.0(S)	90.0(S)	0.0(S)
検査修正	900.0(S)	360.0(S)	30.0(S)
Total	3,390.0(S)	600.0(S)	230.0(S)



3. LED分野への展開及び実績

実用例1;案内板

羽田空港バス案内所

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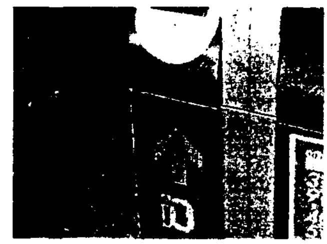
3. LED分野への展開及び実績

実用例2;自動改札口



JR東京駅在来線自動改札

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3. LED分野への展開及び実績

実用例3;メッセージボード

自動販売機

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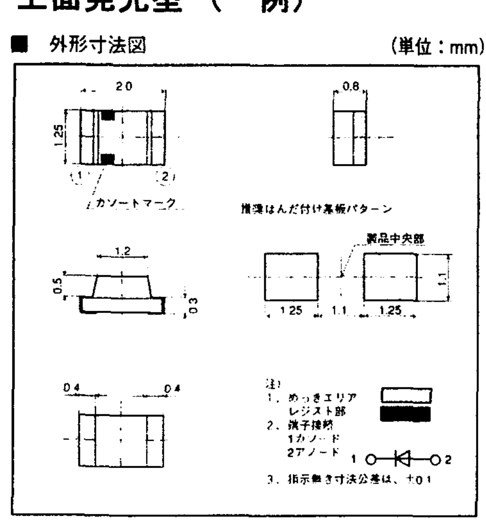
チップ部品型LEDランプ標準外形寸法

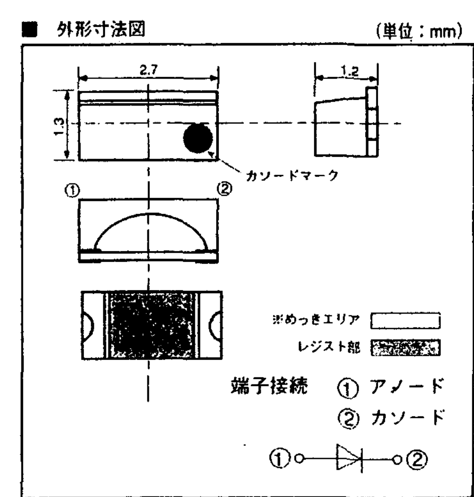
上面発光型（一例）

■ 外形寸法図　(単位：mm)



側面発光型

■ 外形寸法図　(単位：mm)



VPES® を用いたチップ部品型LEDランプ生産実績

発光方向	構　　造	需要家
上 面	1. リードフレーム反射板一帯成型 2. 基板＋反射板　貼付け 3. キャビティ基板（反射板不要） 4. 基板のみ（広角発光）	オプトレックス他 シチズン他 日亜化学他 光波他
側 面	サイド発光チップLED 半田付け用電極部 光 LED 裏面	シャープ他

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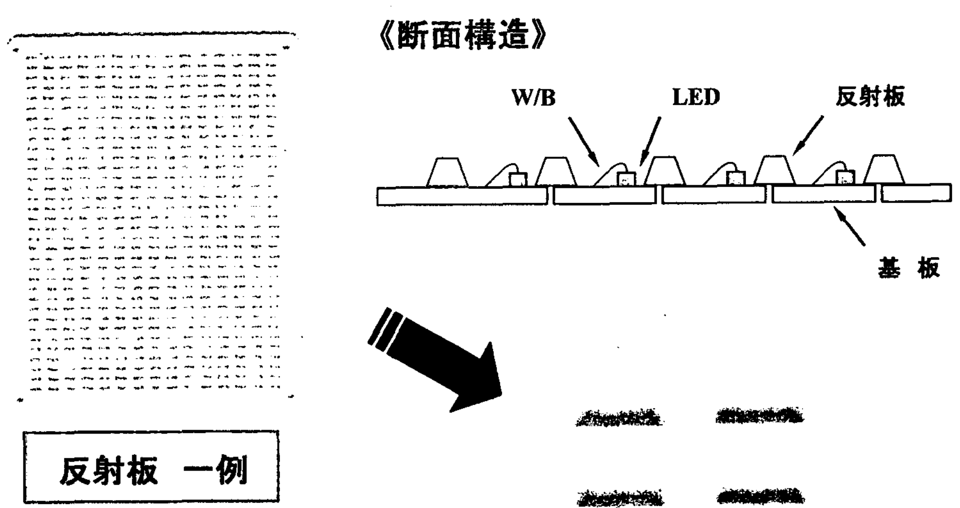
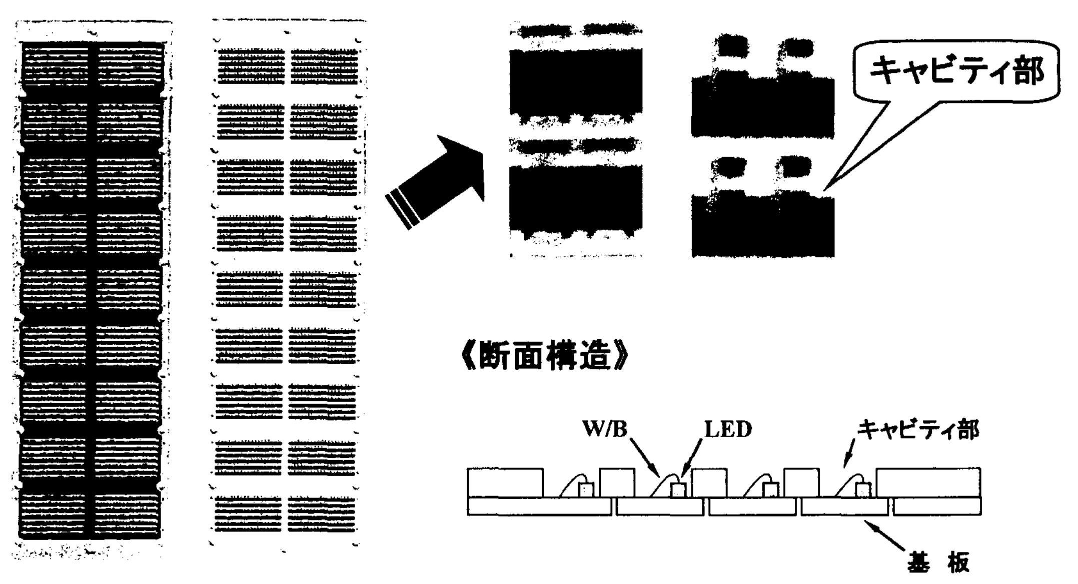
上面発光型構造　　基板＋反射板　貼付け



反射板 一例

上面発光型構造　キャビティ基板（反射板不要）



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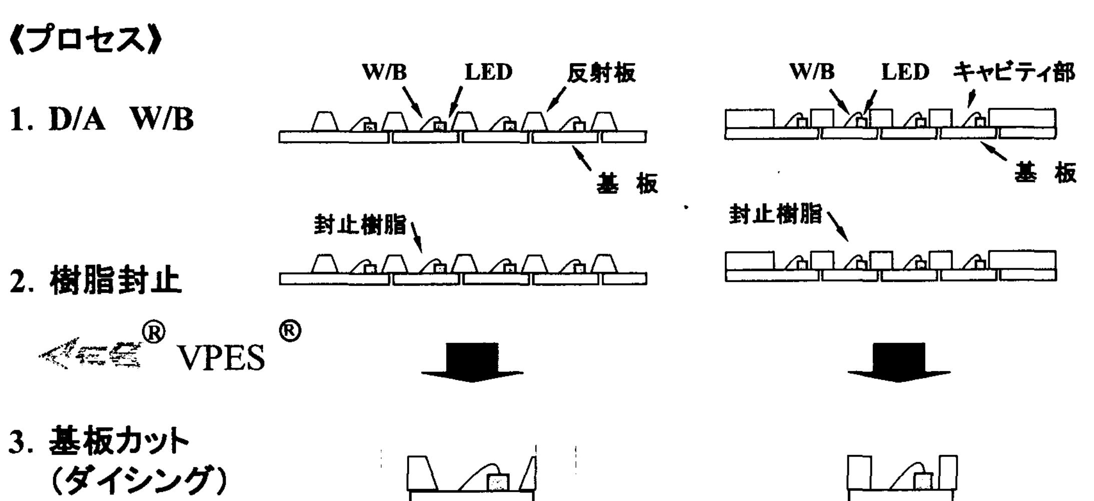
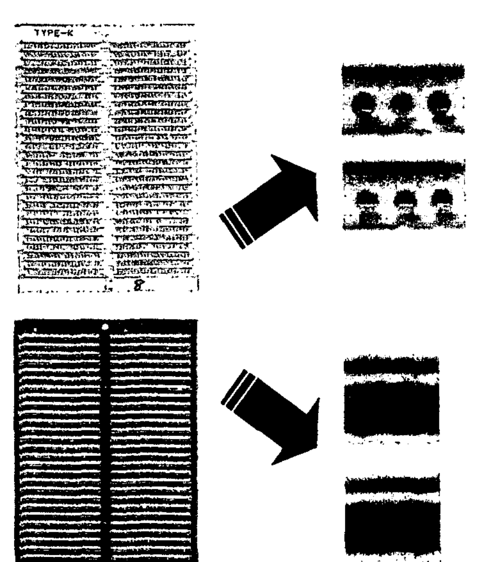
上面発光型構造　基板+反射板、キャビティ基板

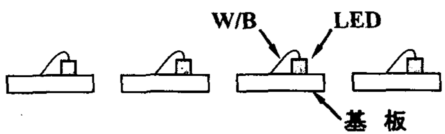


上面発光型構造　基板のみ（広角発光）



《断面構造及びプロセス》

1. D/A　W/B



2. 樹脂封止 ® VPES ®

封止樹脂

3. カット（かまぼこ型チップLED）

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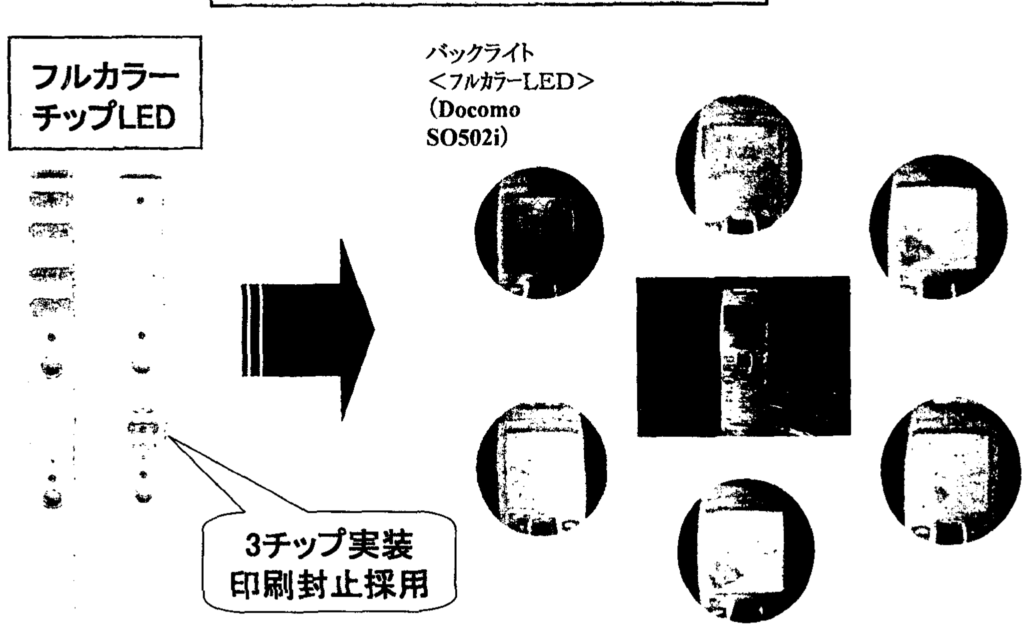
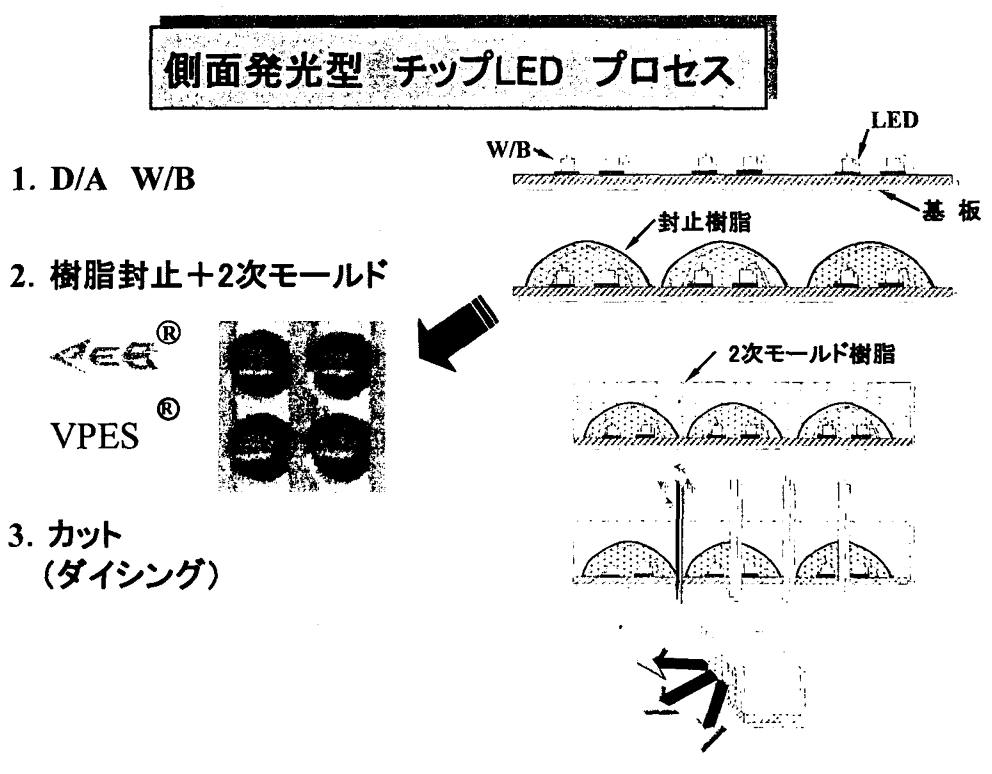
上面発光型構造　実用例





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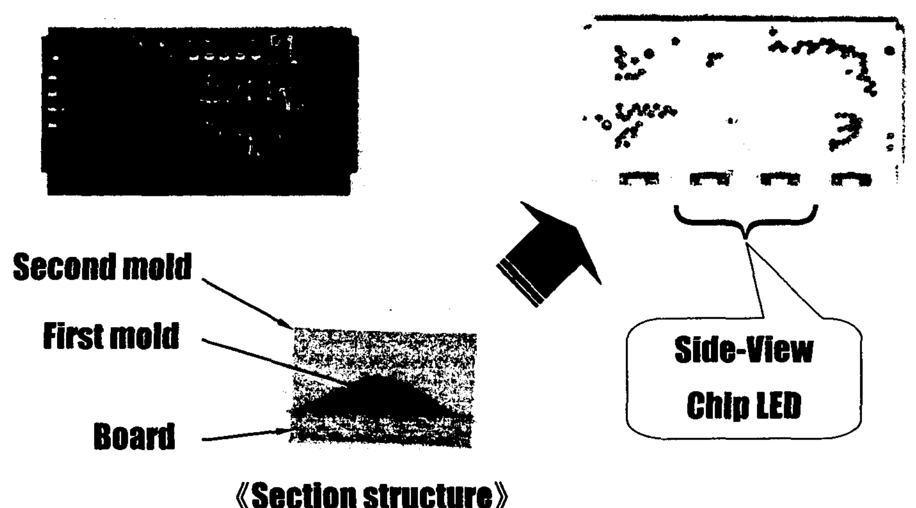

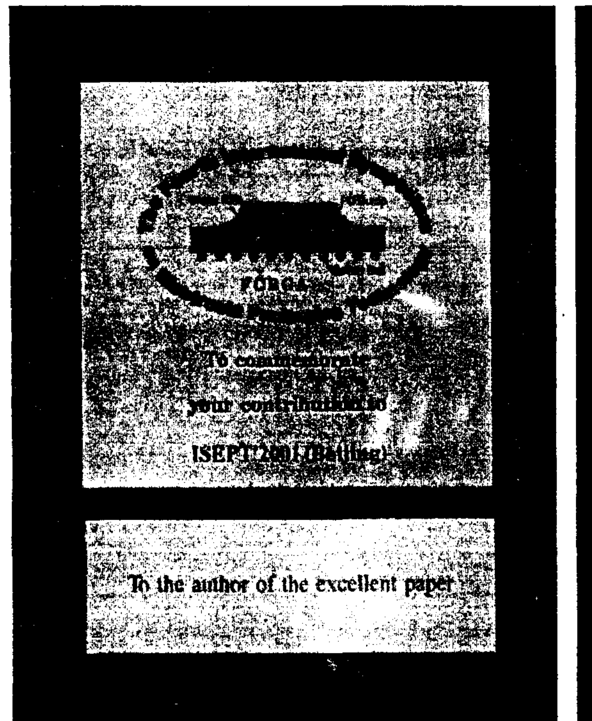

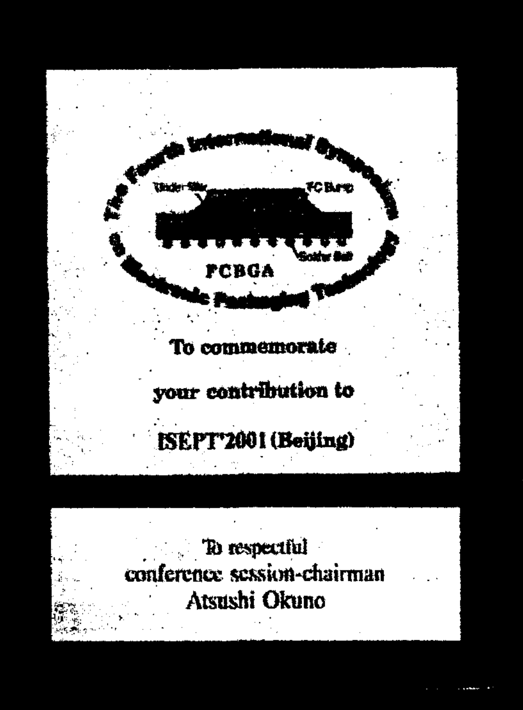

ISEPT'2001: The Fourth International Symposium on Electronic Packaging Technology
Aug., 2001 in Bejing
Excellent paper: High Density Semiconductor Packaging with PES&VPES