# High-density Through-Hole Interconnection in a Silicon Substrate

**Nobuyuki Sadakata**
(Fujikura Ltd. / Japan)

# WAFER LEVEL PACKAGE AND LEAD-FREE SOLDER JOINT RELIABILITY

Nobuyuki Sadakata
Electron Device Laboratory, Fujikura Ltd.
1440 Mutsuzaki, Sakura, Chiba 285-8550, Japan
E-mail nsadakat@fujikura.co.jp

## ABSTRACT

**Wafer-level packaging technology has become established with increase of demands for miniaturizing and realizing lightweight electronic devices evolution. This packaging technology enables the smallest footprint of packaged chip. Various structures and processes has been proposed and manufactured currently, and products taking advantages of wafer-level package come onto the market. The package enables mounting semiconductor chip on print circuit board as is a case with conventional die-level CSP's with BGA solder bumps. Bumping technology is also advancing in both lead-free solder alternative and wafer-level processing such as stencil printing using solder paste. It is known lead-free solder bump formation by stencil printing process tend to form voids in the re-flowed bump. From the result of FEM analysis, it has been found that the strain in solder joints with voids are not always larger than those of without voids. In this paper, characteristics of wafer-level package and effect of void in solder bump on its reliability will be discussed.**

## INTRODUCTION

Advanced new electronic devices, for instance, cellular-phone, personal digital assistants, digital still camera, have now come into our popular life. In keeping with the current trend towards of downsizing, miniaturizing components with packaged IC, new technologies are urgent necessity such as wafer-level package and system in package. Conventional IC package has structure interconnected by wire bonding between metal pad on a die and electrode. "Dual Inline Package" or "Quad Flat Package" is a common structure. Die-level chip scale package is widely used lately with "Ball Grid Array; BGA" solder bump structure enabling compact electrode re-arrangement. Chip scale package with BGA realizes compact packaged IC compared to conventional structure.

"Wafer-Level Chip Scale Packaging; WL-CSP" adopt a method of building up packaging components of resin insulation layer, copper reroute, resin overcoat and solder bump on a whole wafer. Therefore, a chip cut from the wafer is a complete packaged IC with minimized size in area and weight. In the case of a wafer containing smaller die size with lower number of I/O, corresponding to larger number of chips in a wafer, yields lower packaging cost per one chip.

"Metal-Covered Resin-Core Structure" has been developed for a production of wafer-level package, building up with a copper re-route from the contact holes on the chip toward metal-covered post consist of copper cap and resin core.[1] The existence of the elastic resin core enables to reduce total post height and copper thickness for effective stress relaxation without losing mechanical and electrical reliability. Bumping technology is also advancing in both lead-free solder alternative and wafer-level processing such as stencil printing of solder paste. In this process, lead-free solder bumps are formed by stencil printing on a wafer, then being reflowed in a furnace to form solder balls. Stencil printing is favorable process because of its mass-productivity.

It is known lead-free solder bump formation from solder paste tend to form voids in the reflowed bump. Failure mode of board-level reliability evaluation under heat-cycle test was practically crack formation in solder joint. Therefore, it is anticipated that existence of voids in lead-free bump degrade its solder joint or not. In this paper, the relationship between formation of solder joints were examined by finite element method analysis and mechanical shear fatigue test.

## FATIGUE STRENGTH OF EUTICTIC SOLDER AND LEAD-FREE SOLDER

To compare the thermal fatigue strength of conventional Sn-37Pb eutectic solder and lead-free solder, isothermal mechanical fatigue test of the BGA package was carried out. The isothermal cycle test has been proposed by the group at Yokohama National University. The consistency of these two tests has sufficiently been accepted [2]-[4]. Figure 1 shows the schematic illustrations of the isothermal mechanical fatigue test equipment used in this study. The specimen was fixed to the jigs to which both its upper and lower surfaces were bonded; and a prescribed shear displacement was applied repeatedly to the upper jig. The displacement controlled fatigue test was carried out by applying triangular waves with a constant displacement rate. The part of the solder joint was observed throughout the fatigue test, through a microscope of high magnifying power and the relative displacement on the upper and lower surfaces of the solder ball was measured directly through the observation images. In this study, the failure number was defined as the number of cycles that pass before the load drops about 10% from the initial load. And in order to investigate the stress and strain behavior in the solder joint, elasto-plastic analyses were carried out using FEM.

The fatigue lives of each solder joint are shown in Figures 2 and 3. Axis of ordinate is the equivalent inelastic strain range of each solder joint which was calculated by FEM analysis and axis of abscissa is the cycles to failure of each solder joint given by isothermal mechanical fatigue test. The fatigue life of each solder joint was evaluated from equivalent inelastic strain range of the solder joint by Manson-Coffn's law [5]

## EFFECT OF VOIDS ON RELIABILITY OF LEAD-FREE SOLDER JOINTS

In the mechanical fatigue test, it was found that the thermal fatigue strength of lead-free solder joints is almost equivalent to that of Sn-37Pb eutectic solder joints. Equivalent plastic strain and x-z shear strain of solder joints with voids were calculated using FEM analysis, and the effect of voids on thermal fatigue strength of lead solder joints based on the results was examined[6]. Six types of models were analyzed models included 6 types in all. Models without void and in which position and size of the void were changed were prepared. The analysis model with a void was considered for two cases. One is the case that the void is formed on the central axis of the BGA solder joint and the other is the case that the void was generated in the corner of the solder joint. Figure 4 shows dimensions of models. Table 1 and Figure 5 show the position and size of the void in each model and the analysis model of each type, respectively. The properties of the solder joint materials are shown in Table 2. The analysis was carried out by fixing the lower surface of the solder joint and by applying shear displacement to the upper surface of the solder joint as shown in Figure 6. Table 3 shows that the maximum value of x-z shear strain and equivalent plastic strain in each solder joint, and ratio to base model (no-void model). In the case of Types 1, 2 and 3, void exists at the central axis of the solder joint, and x-z shear strain and equivalent plastic strain are larger than that of the base model without a void. On the other hand, in the case of Types 4 and 5, there exists a void at the corner of the solder joint. x-z shear strain and equivalent plastic strain are smaller than that of the base model, while the difference of the result is fairly small.

From the results of analysis, x-z shear strain and equivalent plastic strain of solder joints where a void exists are not always larger than those of solder joints without a void. This is related to the size and location of the void. The formation of a void does not always adversely affect the thermal fatigue strength of solder joints. In the extent examined this time, the difference of x-z shear strain and equivalent plastic strain of the solder joint between the Base model with no void and Types 1, 2, 3, 4 and 5 was so small. It was found that the thermal fatigue strength of the solder joint was not affected strongly by the formation of a void.

## FRACTURE MODES OF SOLDER JOINTS WITH LARGE VOIDS

In this study, the mechanical fatigue tests of CSP solder joints are used to compare the fatigue strength of solder joints in which voids exist and solder joints without voids. Figure 7 show the schematic illustrations of CSP specimens used in this study. The specimens are classified into 2 types by solder material. One is Sn-37Pb/Sn-37Pb that is combined with Sn-37Pb bump and Sn-37Pb paste. The other is Sn-3Ag-0.5Cu/Sn-37Pb that is combined with Sn-37Pb ball and Sn-3Ag-0.5Cu solder paste. In the Sn-37Pb/Sn-37Pb specimen, the void is not formed like with conventional eutectic solder. On the contrary, obvious voids are observed in the Sn-3Ag-0.5Cu/Sn-37Pb specimen.

Figure 8 shows the results of the mechanical fatigue tests of the solder joints. The relative displacement of ordinate is the mismatch of displacement on the upper and lower surface of the solder bump, which is measured directly through the microscope images during the fatigue test. The cycles till failure is the number of cycles that pass before the load drops about 10% from the initial load. The figure shows that fatigue strength of Sn-3Ag-0.5Cu/Sn-37Pb specimens in which voids exist and Sn-37Pb/Sn-37Pb specimens without voids is almost equivalent. The figure shows even if a void exists in the solder joint, cracks initiated and were propagated in places away from the void, It means that the fatigue strength is not affected by voids, because the void does not participate in initiation and propagation of cracks. The fatigue strength of the Sn-3Ag-0.5Cu/Sn-37Pb specimen and Sn-37Pb/Sn-37Pb specimen is almost equivalent.

## CONCLUSION

In this study, the fatigue strength of eutectic solder joints and lead-free solder joints were examined using isothermal mechanical fatigue test, and it has been found lead-free solder joints have almost identical fatigue strength as Sn-37Pb eutectic solder joints. The FEM analysis of solder joints was carried out to examine the effect of voids on thermal fatigue strength of lead-free solder joints. From the results of FEM analysis, it has been found that the equivalent plastic strain and shear strain of a solder joint with a void is not always larger than that of a solder joint without a void. And in the extent examined in this study, the difference of the strain was not so large as to affect the fatigue strength of the solder joint. In conclusion, the effect of void formation on fatigue strength of solder joint is small that it may be neglected.

## ACKNOWLEDGMENT

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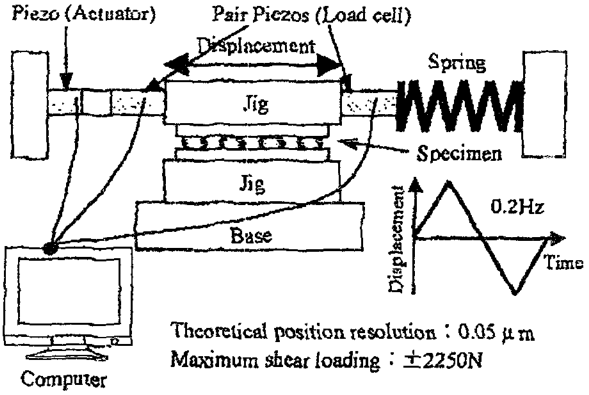


Fig.1. Schematic drawing of the isothermal mechanical fatigue test equipment.

Table 1. Position and size of the void.

| Model type | $d$ | $h$ | $r$ |
|---|---|---|---|
| Base | 0 | 0 | 0 |
| Type-1 | 80 | 80 | 0 |
| Type-2 | 80 | 60 | 0 |
| Type-3 | 120 | 80 | 0 |
| Type-4 | 80 | 80 | 87.5 |
| Type-5 | 120 | 80 | 87.5 |

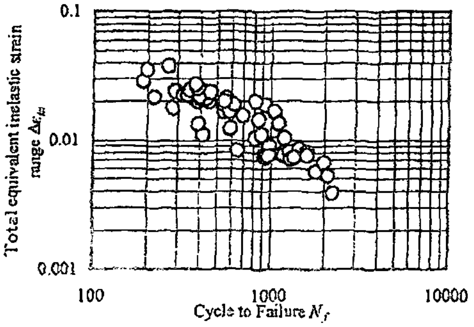


Fig. 2. S-N curves of Sn-37Pb solder joints.

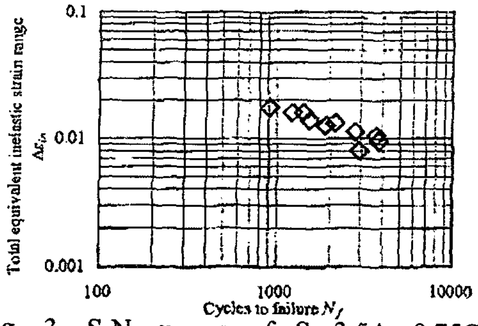


Fig. 3. S-N curves of Sn-3.5Ag-0.75Cu solder joints.

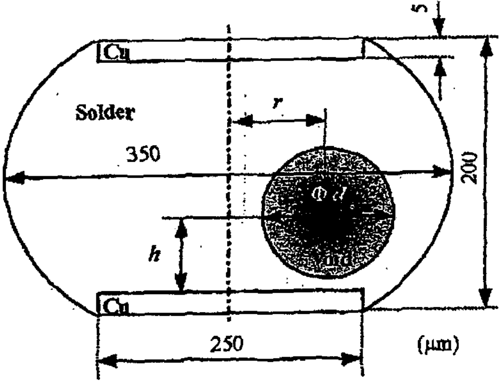
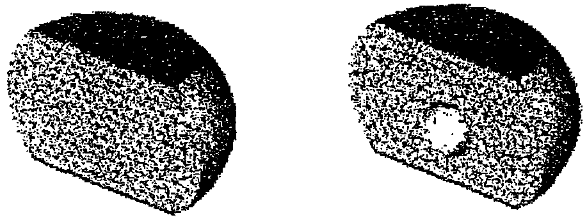
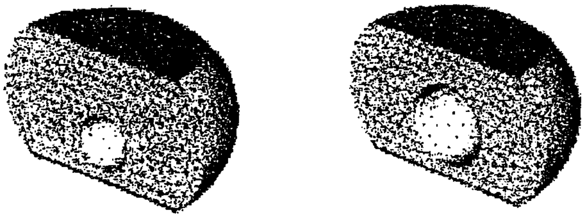


Fig.4. Dimension of analysis model.

Table 2. Position and size of the void

| Material | Elastic modulus (MPa) | Yield stress (MPa) | Poisson's ratio |
|---|---|---|---|
| Cu | 123500 | - | 0.345 |
| Solder | 20000 | 29.1 | 0.388 |


(a) Base (b) Type-1


(c) Type-2 (d) Type-3

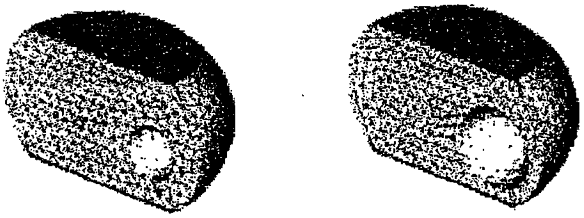
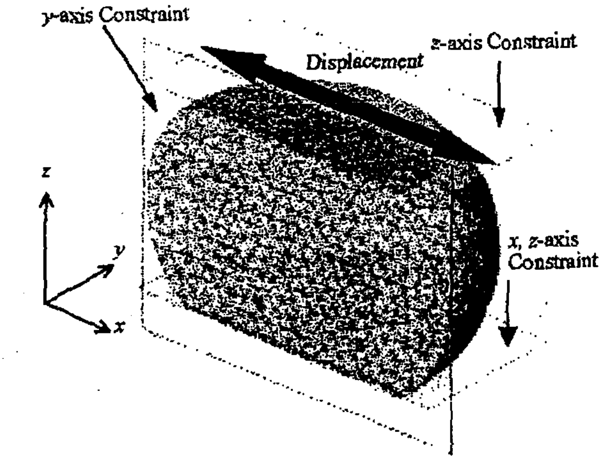
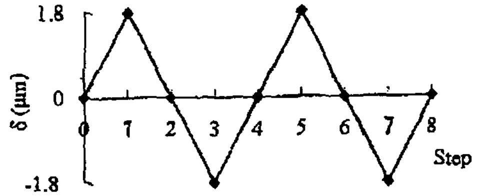

(e) Type-4 (f) Type-5

Fig. 5. Analysis model of bump type



(a) Boundary condition



(b) Displacement

Fig. 6 Boundary condition and displacement in analysis.

Table 3. Results of analysis

| Type of model | x-z shear strain | | Equivalent plastic strain | |
|---|---|---|---|---|
| | STEP 7 | Ratio to Base | STEP 8 | Ratio to Base |
| Base | 2.14E-02 | 1.00 | 1.03E-01 | 1.00 |
| Type-1 | 2.19E-02 | 1.02 | 1.04E-01 | 1.01 |
| Type2 | 2.28E-02 | 1.06 | 1.05E-01 | 1.01 |
| Type-3 | 2.36E-02 | 1.10 | 1.04E-01 | 1.01 |
| Type-4 | 1.92E-02 | 0.90 | 9.78E-02 | 0.95 |
| Type-5 | 2.01E-02 | 0.94 | 9.89E-02 | 0.96 |

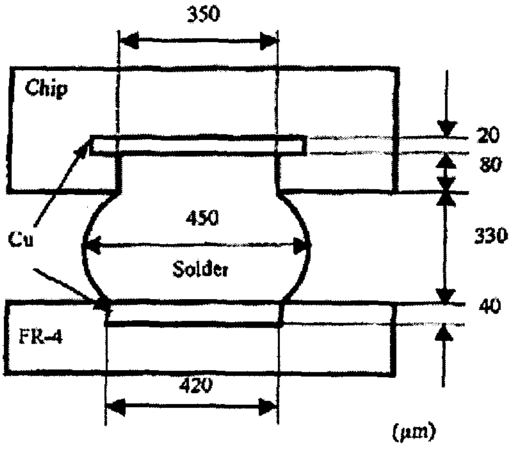


Fig. 7 Schematic drawing of specimen.

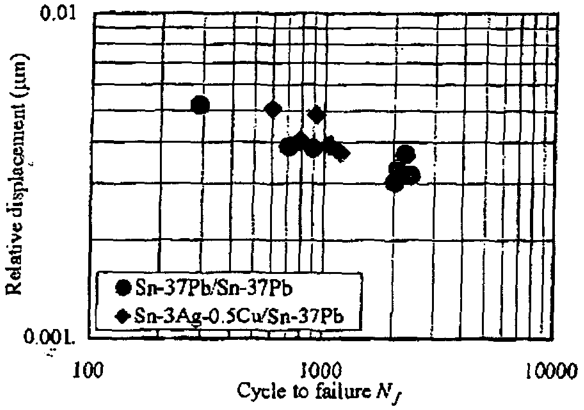


Fig. 8. S-N cureve of eutictic solder joint and lead-free solder joint.